FOREIGN PATENT

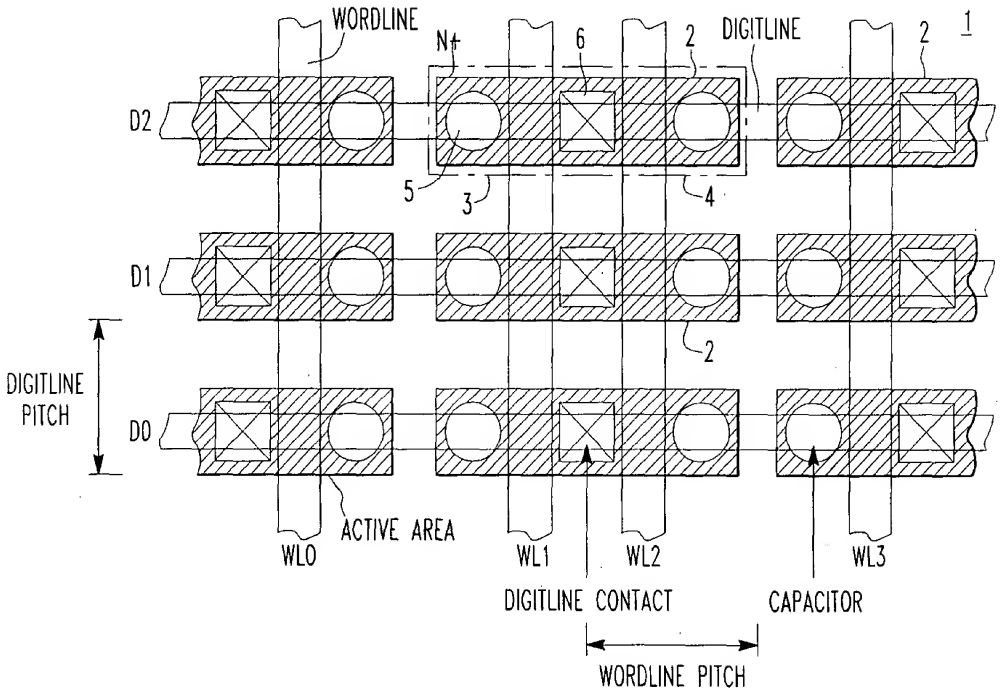
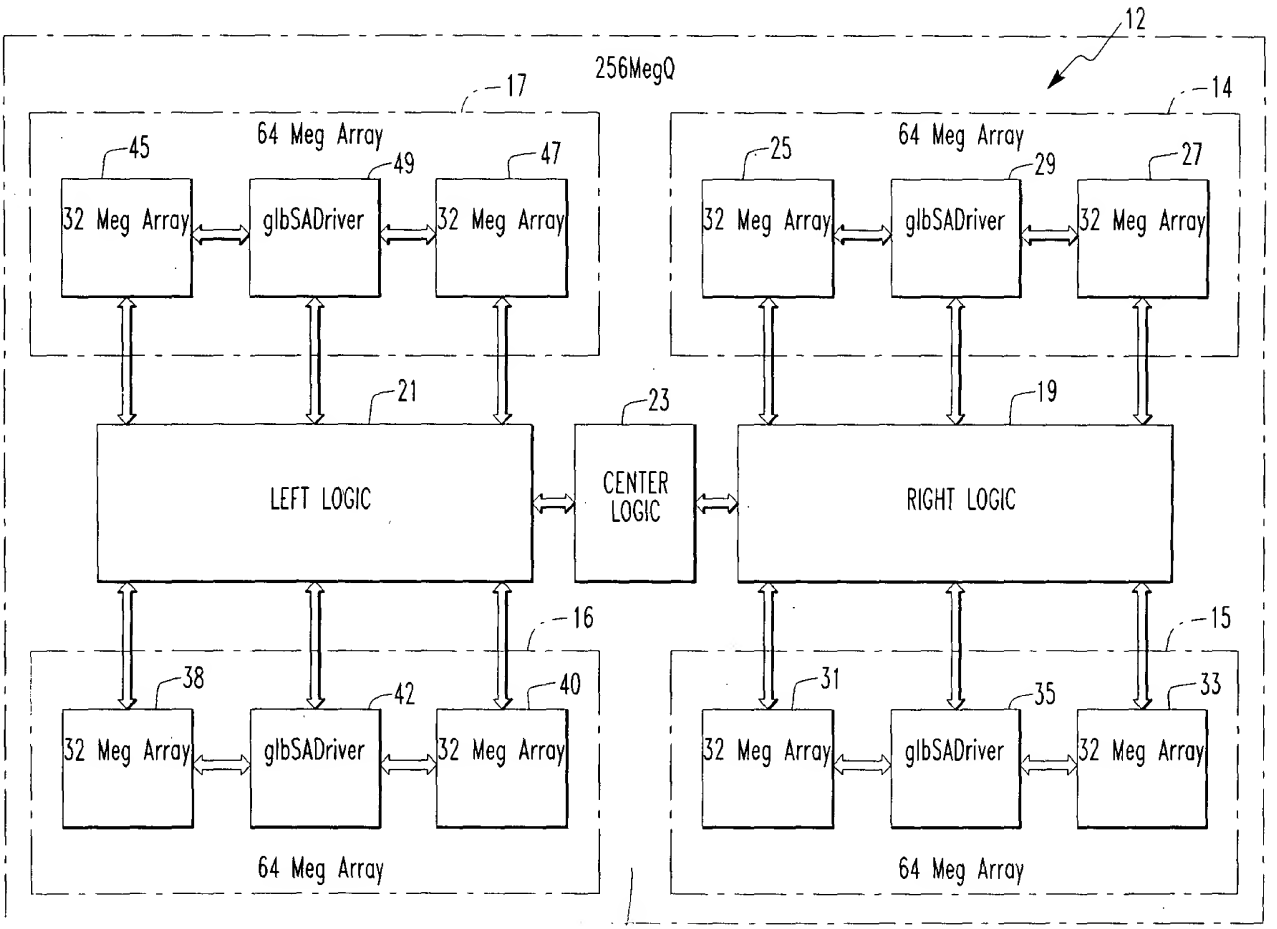


FIG. 1

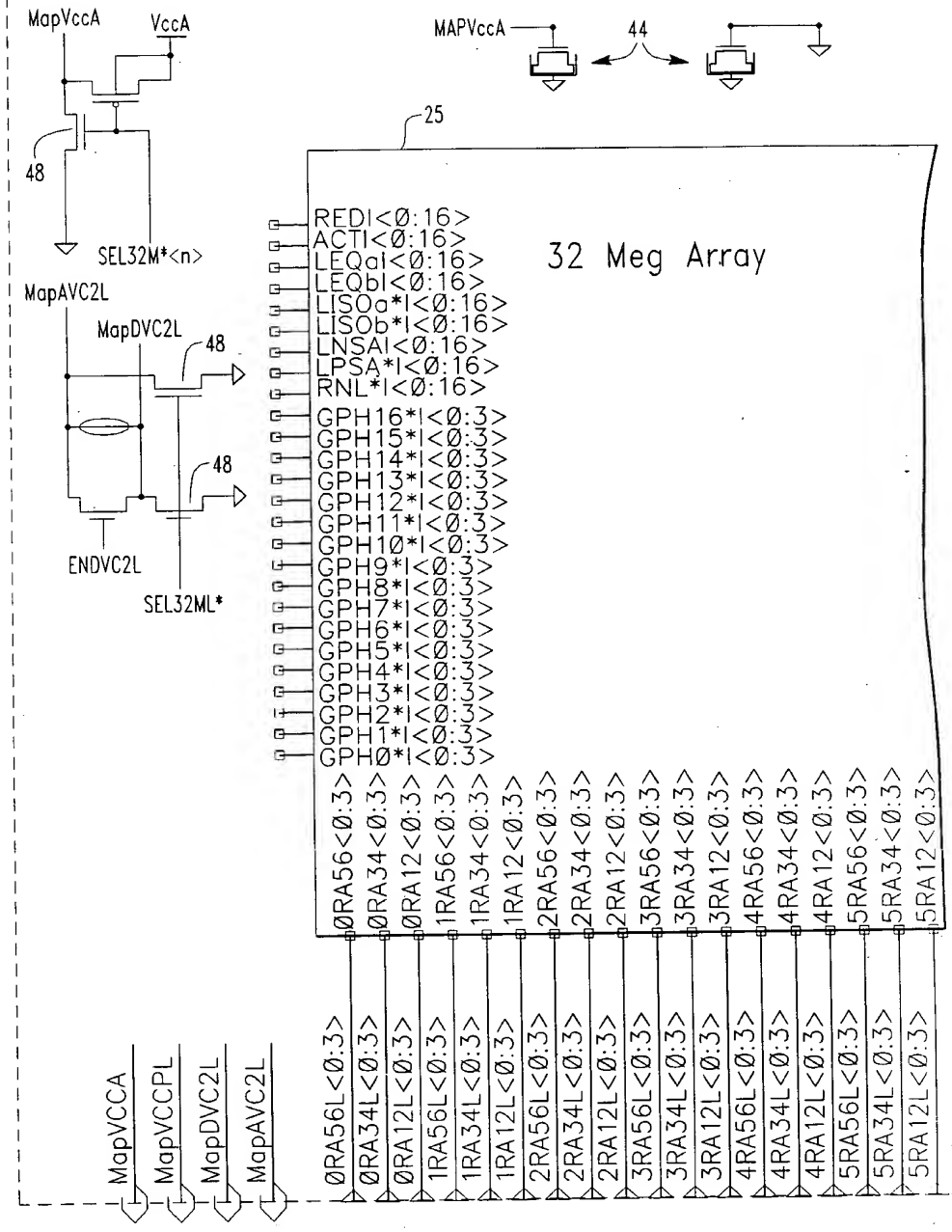
1/367


12
256MegQ
17
64 Meg Array
45
49
47
32 Meg Array
glbSADriver
32 Meg Array
14
64 Meg Array
25
29
27
32 Meg Array
glbSADriver
32 Meg Array
21
23
19
LEFT LOGIC
CENTER LOGIC
RIGHT LOGIC
16
15
38
42
40
31
35
33
32 Meg Array
glbSADriver
32 Meg Array
64 Meg Array
64 Meg Array

10

FIG. 2

FIG. 3A



Docket: 95-0250

FIG. 3B

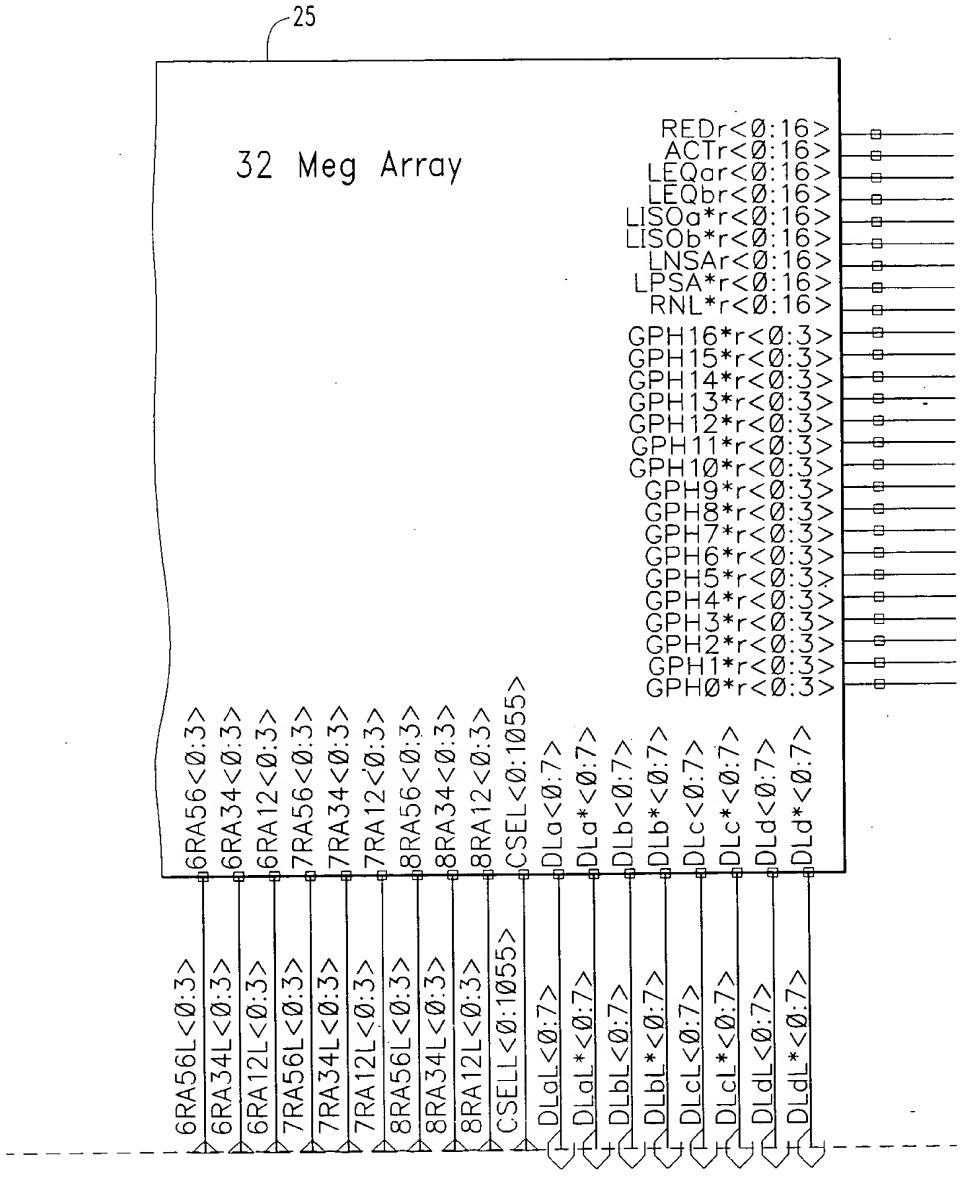

25
32 Meg Array
REDr<0:16>
ACTr<0:16>
LEQar<0:16>
LEQbr<0:16>
LISOa*r<0:16>
LISOb*r<0:16>
LNSAr<0:16>
LPSA*r<0:16>
RNL*r<0:16>
GPH16*r<0:3>
GPH15*r<0:3>
GPH14*r<0:3>
GPH13*r<0:3>
GPH12*r<0:3>
GPH11*r<0:3>
GPH10*r<0:3>
GPH9*r<0:3>
GPH8*r<0:3>
GPH7*r<0:3>
GPH6*r<0:3>
GPH5*r<0:3>
GPH4*r<0:3>
GPH3*r<0:3>
GPH2*r<0:3>
GPH1*r<0:3>
GPH0*r<0:3>
6RA56<0:3>
6RA34<0:3>
6RA12<0:3>
7RA56<0:3>
7RA34<0:3>
7RA12<0:3>
8RA56<0:3>
8RA34<0:3>
8RA12<0:3>
CSEL<0:1055>
DLa<0:7>
DLa*<0:7>
DLb<0:7>
DLb*<0:7>
DLc<0:7>
DLc*<0:7>
DLd<0:7>
DLd*<0:7>
6RA56L<0:3>
6RA34L<0:3>
6RA12L<0:3>
7RA56L<0:3>
7RA34L<0:3>
7RA12L<0:3>
8RA56L<0:3>
8RA34L<0:3>
8RA12L<0:3>
CSELL<0:1055>
DLaL<0:7>
DLaL*<0:7>
DLbL<0:7>
DLbL*<0:7>
DLcL<0:7>
DLcL*<0:7>
DLdL<0:7>
DLdL*<0:7>

FIG. 3C

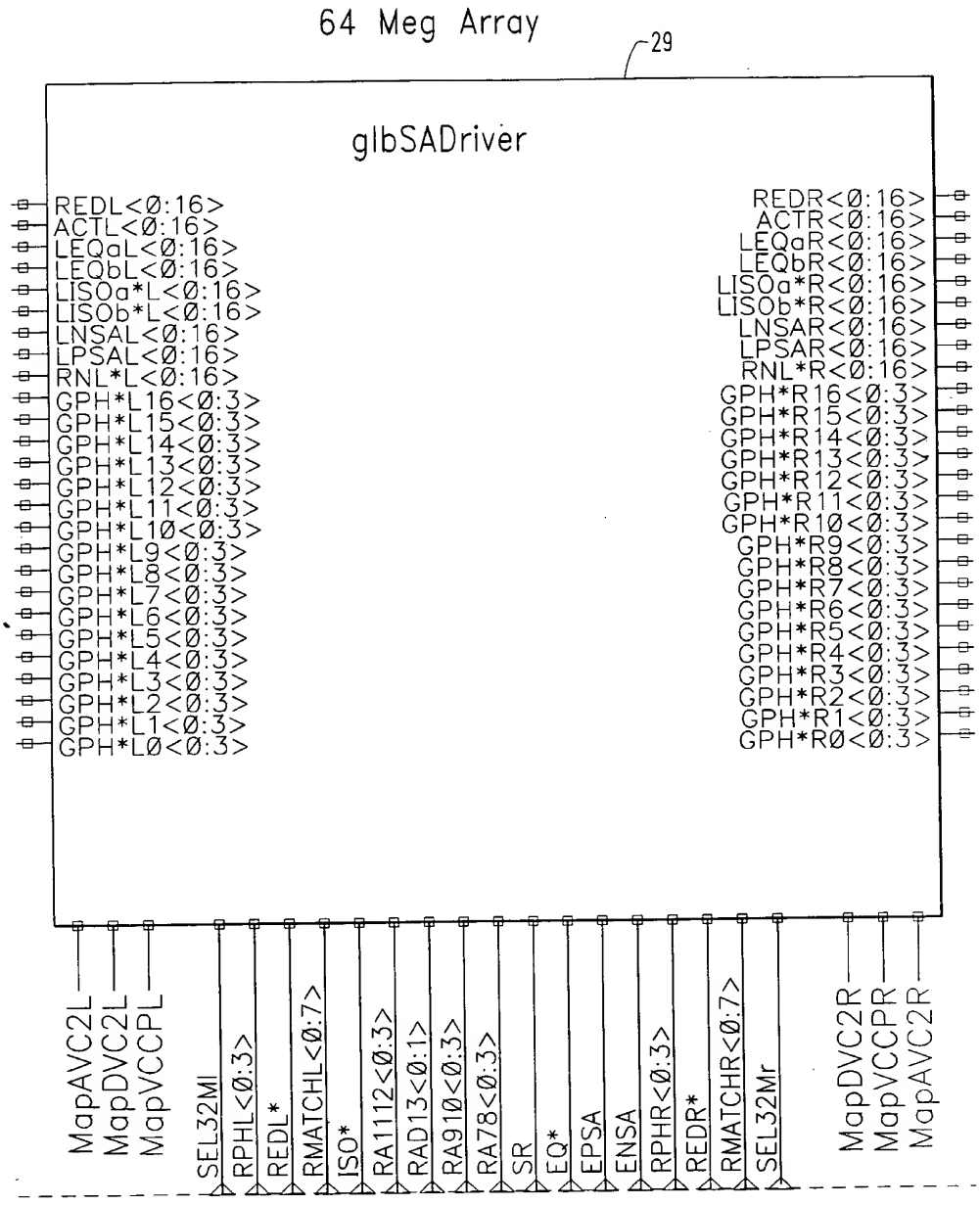

64 Meg Array
29
glbSADriver
REDL<0:16>
ACTL<0:16>
LEQaL<0:16>
LEQbL<0:16>
LISOa*L<0:16>
LISOb*L<0:16>
LNSAL<0:16>
LPSAL<0:16>
RNL*L<0:16>
GPH*L16<0:3>
GPH*L15<0:3>
GPH*L14<0:3>
GPH*L13<0:3>
GPH*L12<0:3>
GPH*L11<0:3>
GPH*L10<0:3>
GPH*L9<0:3>
GPH*L8<0:3>
GPH*L7<0:3>
GPH*L6<0:3>
GPH*L5<0:3>
GPH*L4<0:3>
GPH*L3<0:3>
GPH*L2<0:3>
GPH*L1<0:3>
GPH*L0<0:3>
REDR<0:16>
ACTR<0:16>
LEQaR<0:16>
LEQbR<0:16>
LISOa*R<0:16>
LISOb*R<0:16>
LNSAR<0:16>
LPSAR<0:16>
RNL*R<0:16>
GPH*R16<0:3>
GPH*R15<0:3>
GPH*R14<0:3>
GPH*R13<0:3>
GPH*R12<0:3>
GPH*R11<0:3>
GPH*R10<0:3>
GPH*R9<0:3>
GPH*R8<0:3>
GPH*R7<0:3>
GPH*R6<0:3>
GPH*R5<0:3>
GPH*R4<0:3>
GPH*R3<0:3>
GPH*R2<0:3>
GPH*R1<0:3>
GPH*R0<0:3>
MapAVC2L
MapDVC2L
MapVCCPL
SEL32MI
RPHL<0:3>
REDL*
RMATCHL<0:7>
ISO*
RA1112<0:3>
RAD13<0:1>
RA910<0:3>
RA78<0:3>
SR
EQ*
EPSA
ENSA
RPHR<0:3>
REDR*
RMATCHR<0:7>
SEL32Mr
MapDVC2R
MapVCCPR
MapAVC2R

FIG. 3D

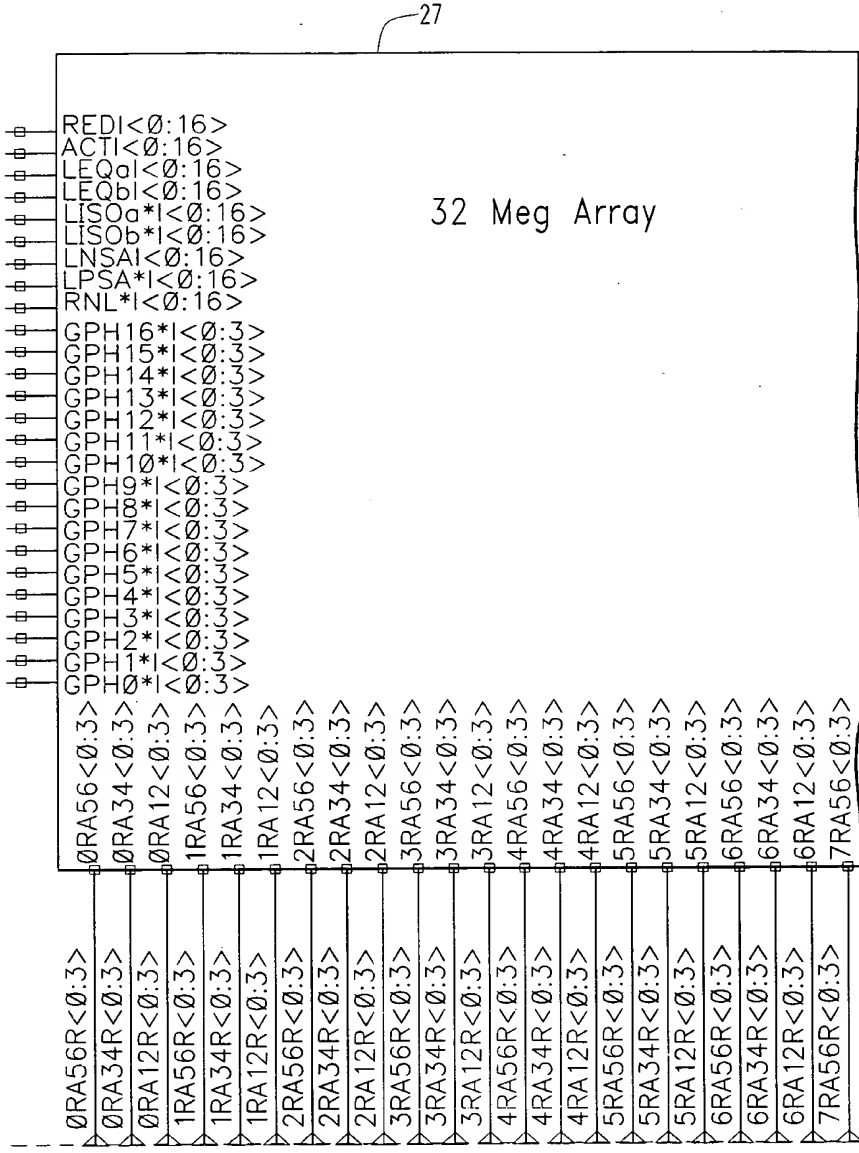
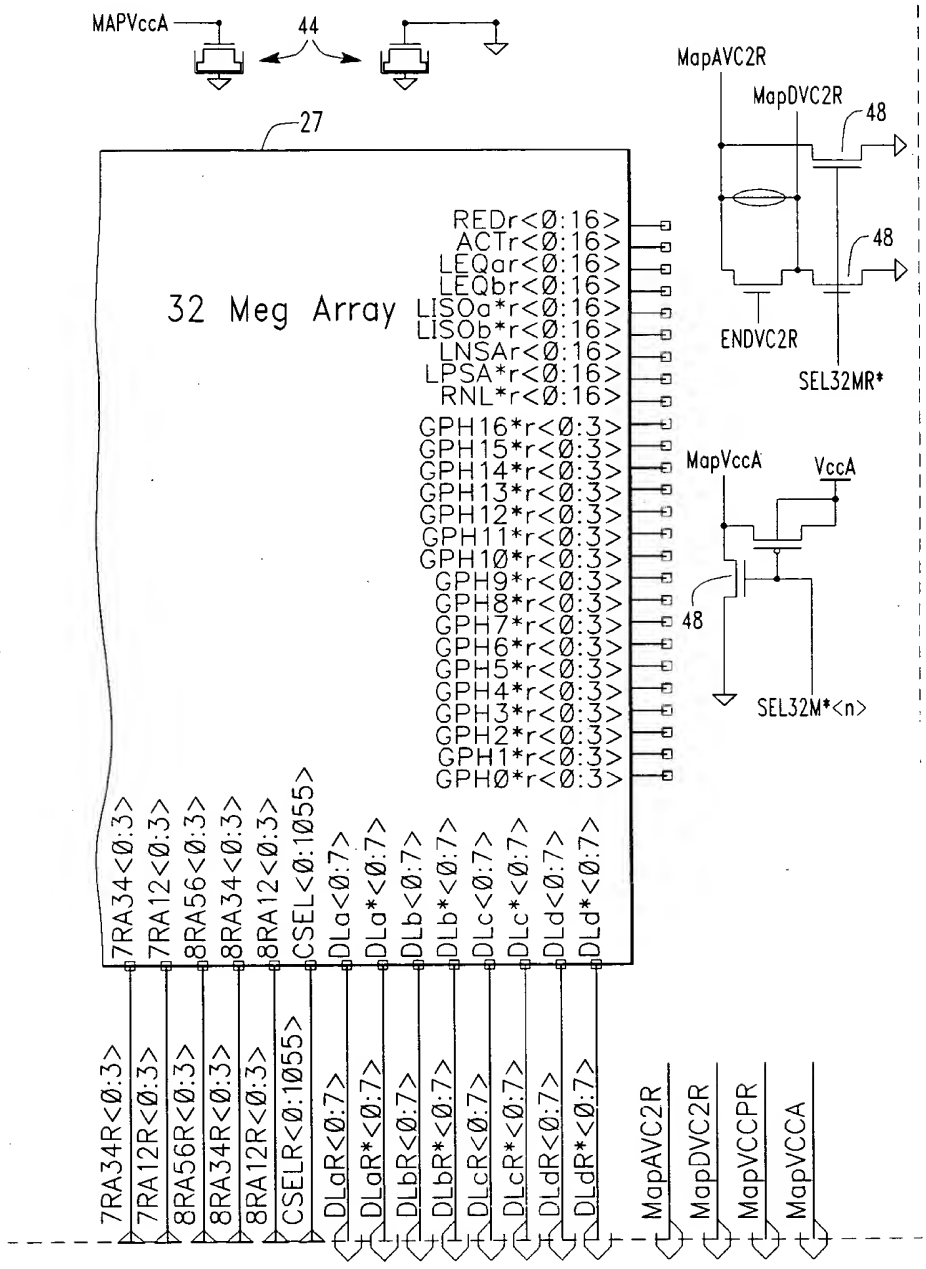

27
32 Meg Array
REDI<Ø:16>
ACTI<Ø:16>
LEQaI<Ø:16>
LEQbI<Ø:16>
LISOa*I<Ø:16>
LISOb*I<Ø:16>
LNSAI<Ø:16>
LPSA*I<Ø:16>
RNL*I<Ø:16>
GPII16*I<Ø:3>
GPII15*I<Ø:3>
GPII14*I<Ø:3>
GPII13*I<Ø:3>
GPII12*I<Ø:3>
GPII11*I<Ø:3>
GPII10*I<Ø:3>
GPII9*I<Ø:3>
GPII8*I<Ø:3>
GPII7*I<Ø:3>
GPII6*I<Ø:3>
GPII5*I<Ø:3>
GPII4*I<Ø:3>
GPII3*I<Ø:3>
GPII2*I<Ø:3>
GPII1*I<Ø:3>
GPII0*I<Ø:3>
ØRA56<Ø:3>
ØRA34<Ø:3>
ØRA12<Ø:3>
1RA56<Ø:3>
1RA34<Ø:3>
1RA12<Ø:3>
2RA56<Ø:3>
2RA34<Ø:3>
2RA12<Ø:3>
3RA56<Ø:3>
3RA34<Ø:3>
3RA12<Ø:3>
4RA56<Ø:3>
4RA34<Ø:3>
4RA12<Ø:3>
5RA56<Ø:3>
5RA34<Ø:3>
5RA12<Ø:3>
6RA56<Ø:3>
6RA34<Ø:3>
6RA12<Ø:3>
7RA56<Ø:3>
ØRA56R<Ø:3>
ØRA34R<Ø:3>
ØRA12R<Ø:3>
1RA56R<Ø:3>
1RA34R<Ø:3>
1RA12R<Ø:3>
2RA56R<Ø:3>
2RA34R<Ø:3>
2RA12R<Ø:3>
3RA56R<Ø:3>
3RA34R<Ø:3>
3RA12R<Ø:3>
4RA56R<Ø:3>
4RA34R<Ø:3>
4RA12R<Ø:3>
5RA56R<Ø:3>
5RA34R<Ø:3>
5RA12R<Ø:3>
6RA56R<Ø:3>
6RA34R<Ø:3>
6RA12R<Ø:3>
7RA56R<Ø:3>

FIG. 3E


MAPVccA
44
27
32 Meg Array
REDr<0:16>
ACTr<0:16>
LEQar<0:16>
LEQbr<0:16>
LISOa*r<0:16>
LISOb*r<0:16>
LNSAr<0:16>
LPSA*r<0:16>
RNL*r<0:16>
GPH16*r<0:3>
GPH15*r<0:3>
GPH14*r<0:3>
GPH13*r<0:3>
GPH12*r<0:3>
GPH11*r<0:3>
GPH10*r<0:3>
GPH9*r<0:3>
GPH8*r<0:3>
GPH7*r<0:3>
GPH6*r<0:3>
GPH5*r<0:3>
GPH4*r<0:3>
GPH3*r<0:3>
GPH2*r<0:3>
GPH1*r<0:3>
GPH0*r<0:3>
7RA34<0:3>
7RA12<0:3>
8RA56<0:3>
8RA34<0:3>
8RA12<0:3>
CSEL<0:1055>
DLa<0:7>
DLa*<0:7>
DLb<0:7>
DLb*<0:7>
DLc<0:7>
DLc*<0:7>
DLd<0:7>
DLd*<0:7>
7RA34R<0:3>
7RA12R<0:3>
8RA56R<0:3>
8RA34R<0:3>
8RA12R<0:3>
CSELR<0:1055>
DLaR<0:7>
DLaR*<0:7>
DLbR<0:7>
DLbR*<0:7>
DLcR<0:7>
DLcR*<0:7>
DLdR<0:7>
DLdR*<0:7>
MapAVC2R
MapDVC2R
MapVCCPR
MapVCCA
MapAVC2R
MapDVC2R
48
48
ENDVC2R
SEL32MR*
MapVccA
VccA
48
SEL32M*<n>

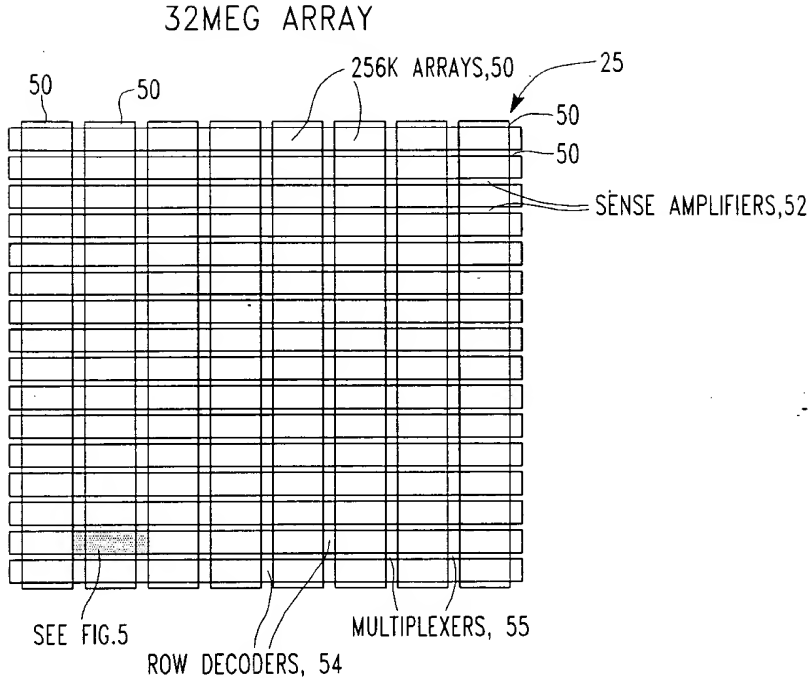

32MEG ARRAY
50
50
256K ARRAYS,50
25
50
50
SENSE AMPLIFIERS,52
SEE FIG.5
ROW DECODERS, 54
MULTIPLEXERS, 55

FIG. 4

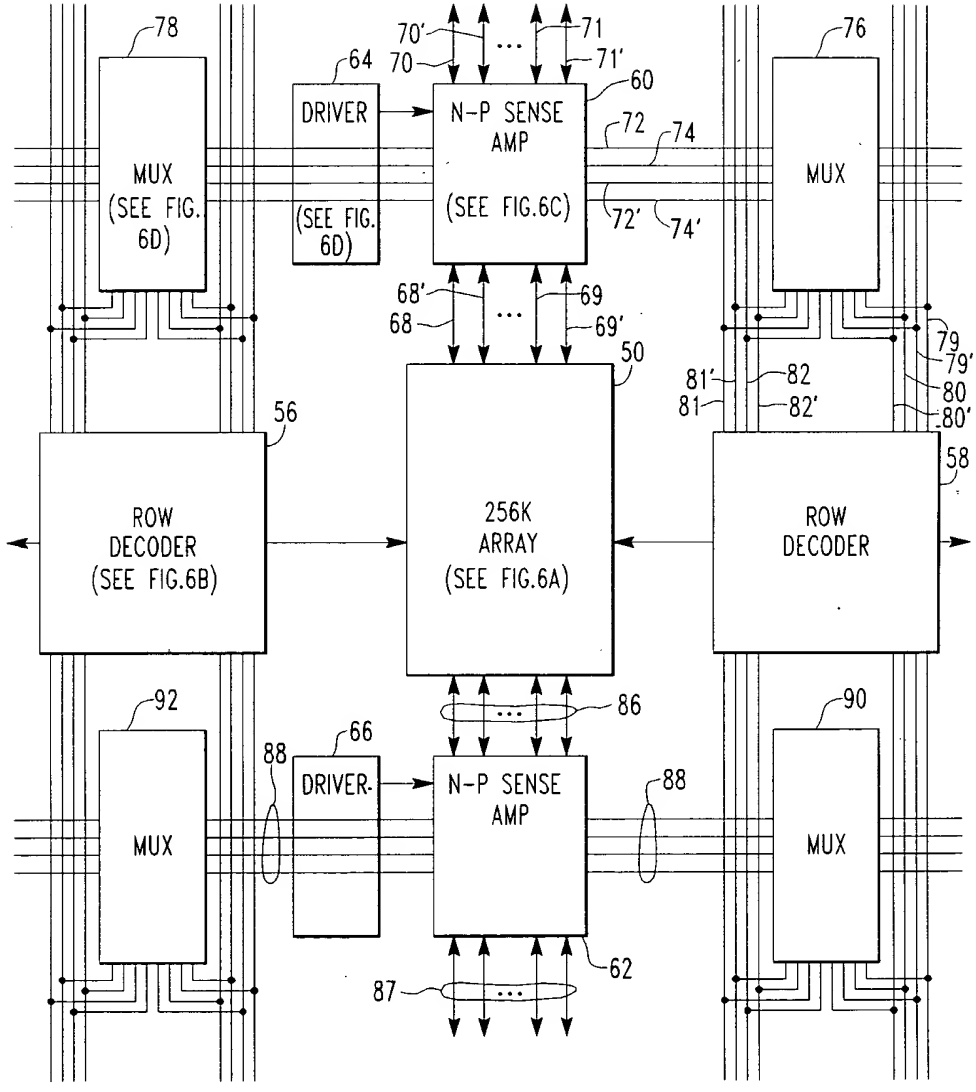

78
MUX
(SEE FIG.
6D)
64
DRIVER
(SEE FIG.
6D)
70'
70
71
71'
60
N-P SENSE
AMP
(SEE FIG.6C)
72
74
72'
74'
76
MUX
68'
68
69
69'
50
79
79'
80
80'
81'
81
82
82'
56
ROW
DECODER
(SEE FIG.6B)
256K
ARRAY
(SEE FIG.6A)
ROW
DECODER
58
92
MUX
88
66
DRIVER
N-P SENSE
AMP
88
86
90
MUX
87
62

FIG. 5

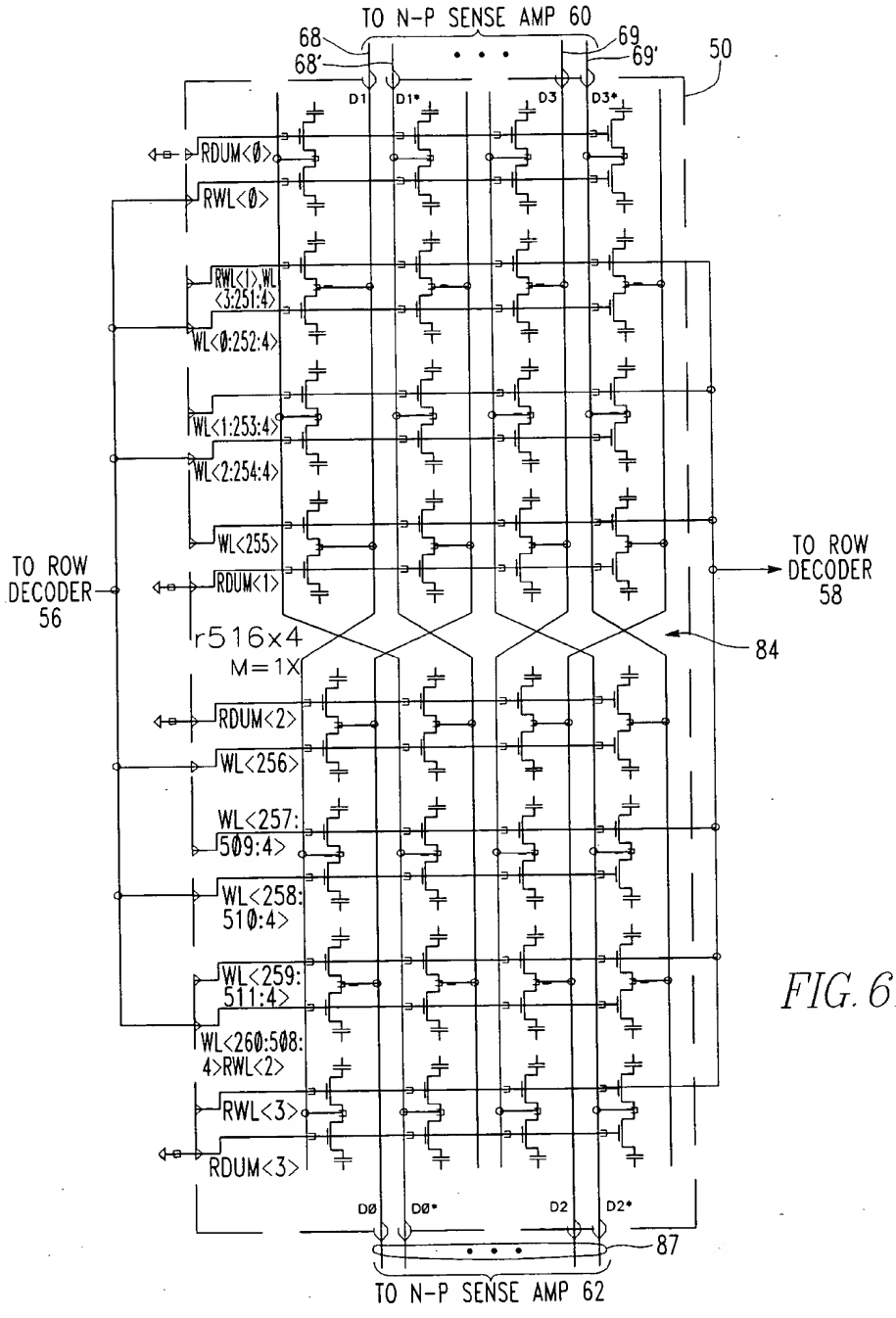

TO N-P SENSE AMP 60
68
68'
69
69'
50
D1
D1*
D3
D3*
RDUM<Ø>
RWL<Ø>
RWL<1>,WL<3:251:4>
WL<Ø:252:4>
WL<1:253:4>
WL<2:254:4>
WL<255>
RDUM<1>
TO ROW DECODER 56
TO ROW DECODER 58
r516x4
M=1X
84
RDUM<2>
WL<256>
WL<257:509:4>
WL<258:510:4>
WL<259:511:4>
WL<260:508:4>RWL<2>
RWL<3>
RDUM<3>
DØ
DØ*
D2
D2*
87
TO N-P SENSE AMP 62

FIG. 6A

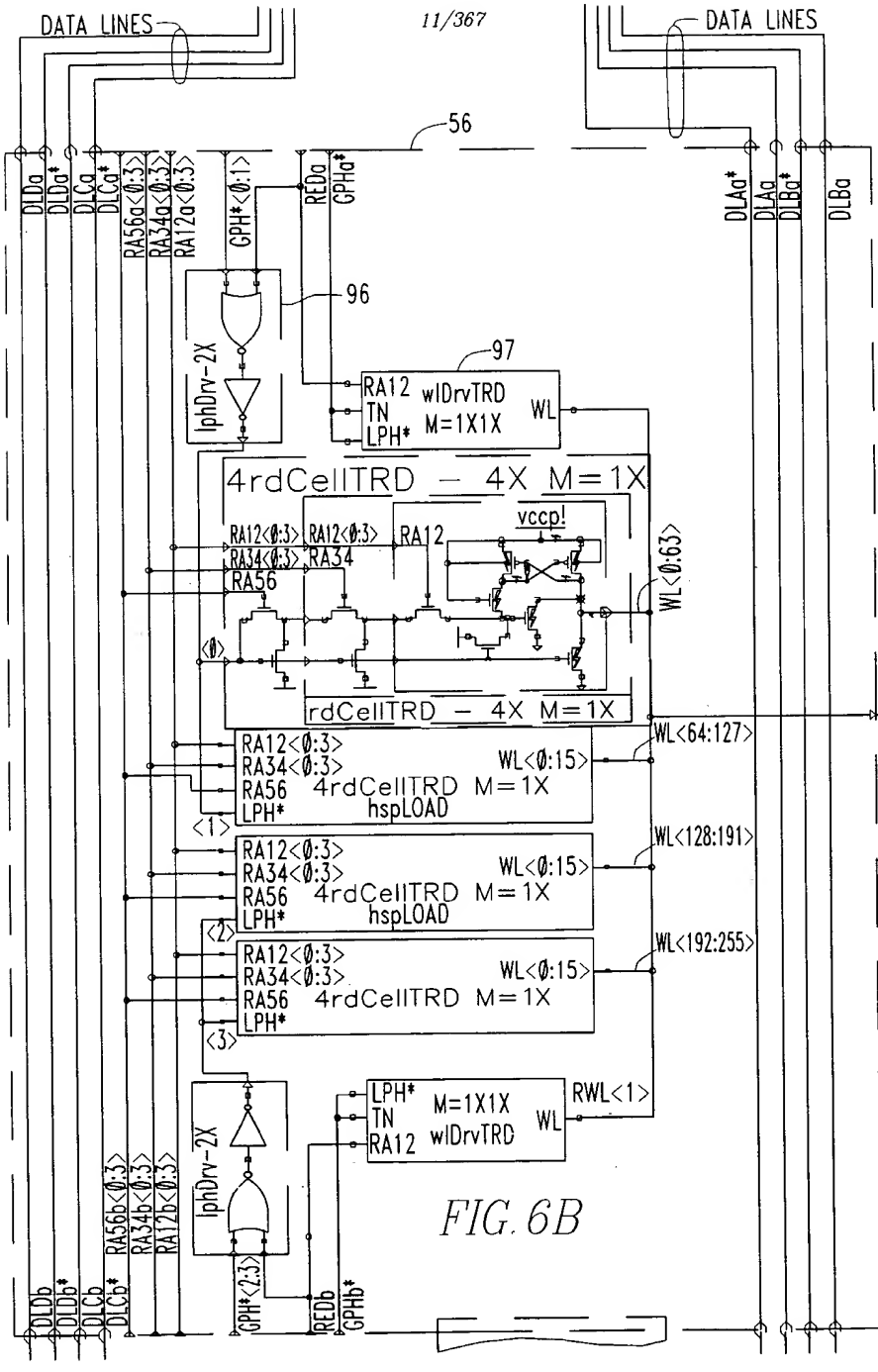

DATA LINES
DATA LINES
56
DLDa
DLDa*
DLCa
DLCa*
RA56a<0:3>
RA34a<0:3>
RA12a<0:3>
GPH*<0:1>
REDa
GPHa*
DLAa*
DLAa
DLBa*
DLBa
96
97
IphDrv-2X
RA12
TN
LPH*
wlDrvTRD
M=1X1X
WL
4rdCellTRD – 4X M=1X
vccp!
RA12<0:3>
RA34<0:3>
RA56
RA12<0:3>
RA12
RA34
WL<0:63>
<0>
rdCellTRD – 4X M=1X
WL<64:127>
RA12<0:3>
RA34<0:3>
RA56
LPH*
4rdCellTRD M=1X
hspLOAD
WL<0:15>
<1>
WL<128:191>
<2>
WL<192:255>
<3>
RWL<1>
DLDb
DLDb*
DLCb
DLCb*
RA56b<0:3>
RA34b<0:3>
RA12b<0:3>
GPH*<2:3>
REDb
GPHb*

FIG. 6B

Connections of odd/even columns to IOa and IOb alternates with odd/even column select lines:

CAØ1*	D1(even)	D2(odd)
Ø	IOa	IOb
1	IOb	IOa
2	IOa	IOb
3	IOb	IOa

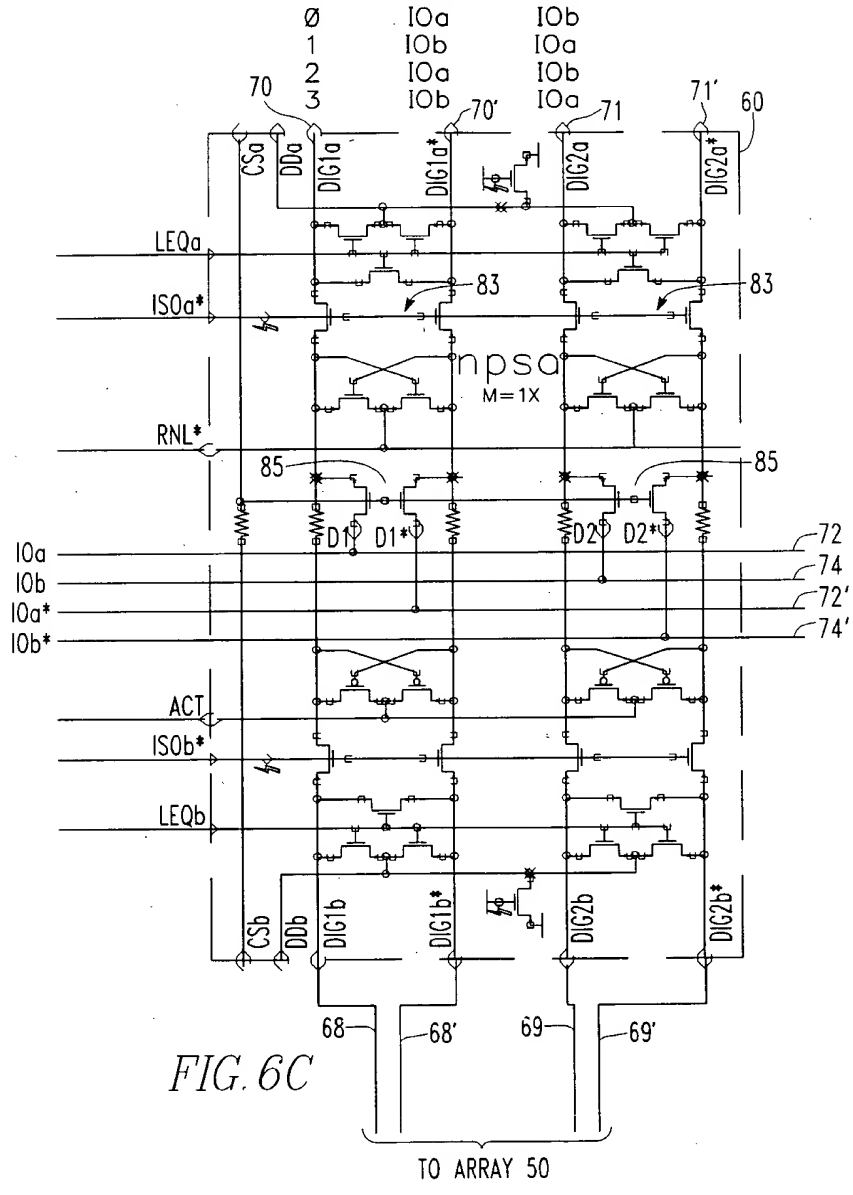


FIG. 6C

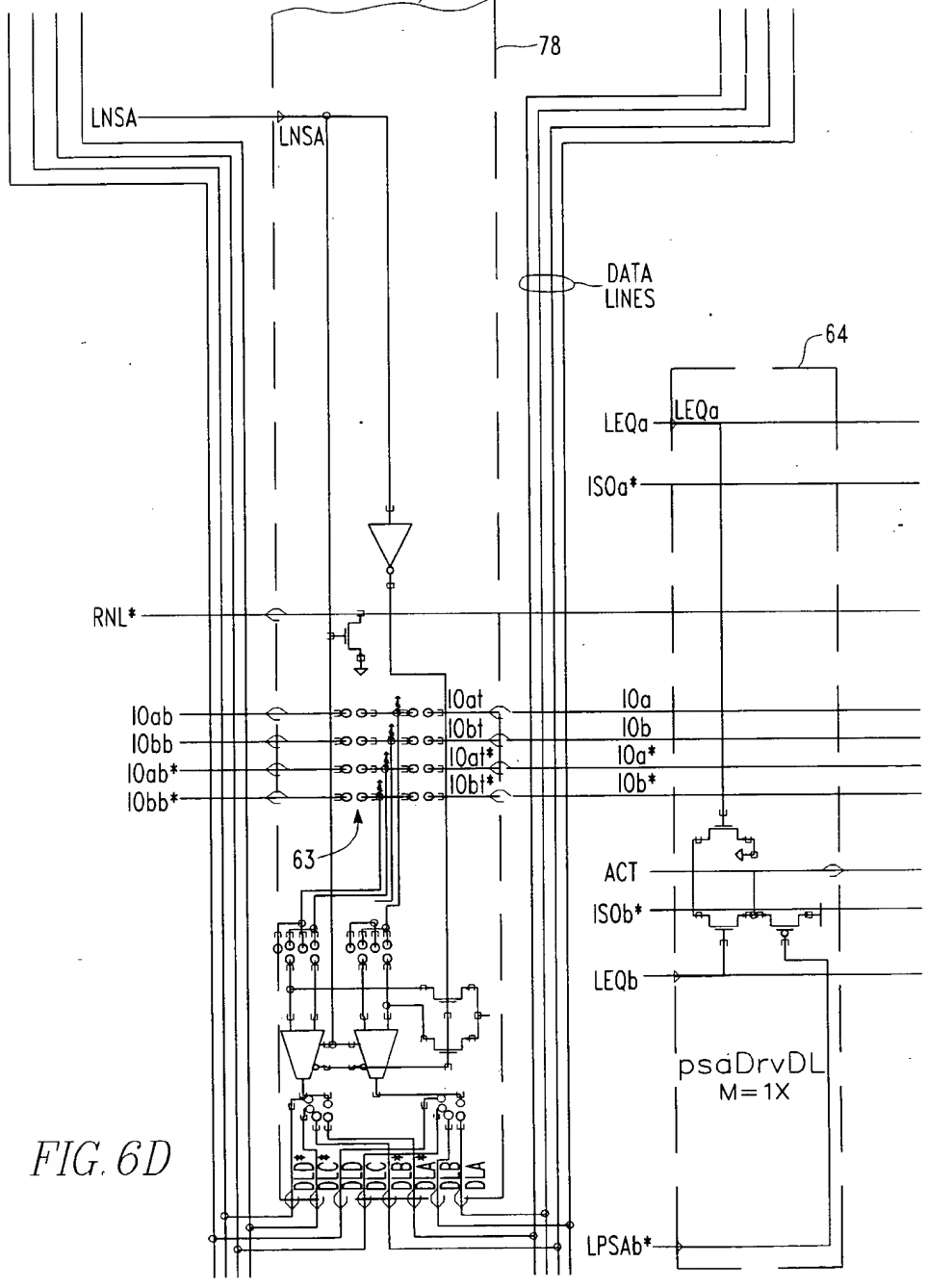

78
LNSA
LNSA
DATA LINES
64
LEQa
LEQa
ISOa*
RNL*
IOab
IObb
IOab*
IObb*
IOat
IObt
IOat*
IObt*
IOa
IOb
IOa*
IOb*
63
ACT
ISOb*
LEQb
psaDrvDL
M=1X
DLD*
DLC*
DLD
DLC
DLB*
DLA*
DLB
DLA
LPSAb*

FIG. 6D

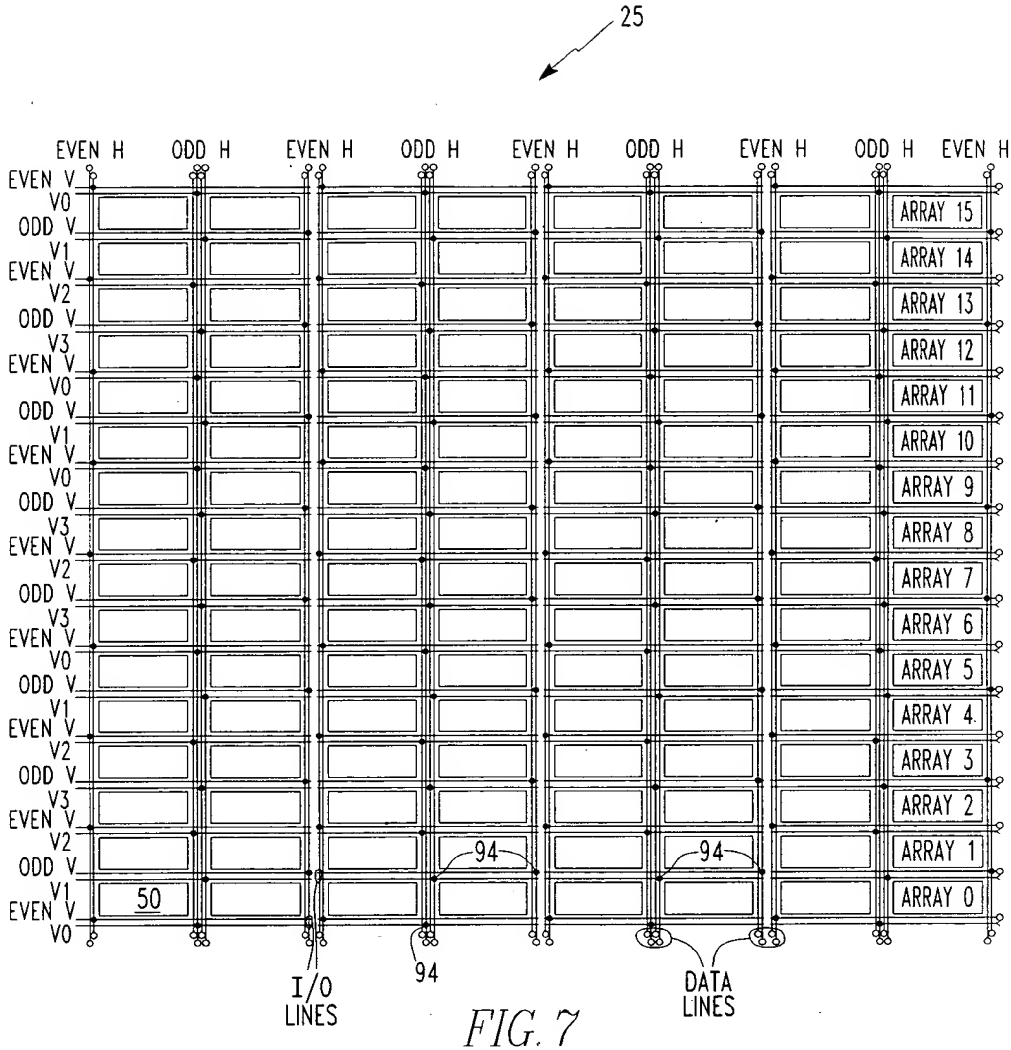

25
EVEN H
ODD H
EVEN H
ODD H
EVEN H
ODD H
EVEN H
ODD H
EVEN H
EVEN V
V0
ODD V
V1
EVEN V
V2
ODD V
V3
EVEN V
V0
ODD V
V1
EVEN V
V0
ODD V
V3
EVEN V
V2
ODD V
V3
EVEN V
V0
ODD V
V1
EVEN V
V2
ODD V
V3
EVEN V
V2
ODD V
V1
EVEN V
V0
50
94
94
94
I/O LINES
DATA LINES
ARRAY 15
ARRAY 14
ARRAY 13
ARRAY 12
ARRAY 11
ARRAY 10
ARRAY 9
ARRAY 8
ARRAY 7
ARRAY 6
ARRAY 5
ARRAY 4
ARRAY 3
ARRAY 2
ARRAY 1
ARRAY 0

FIG. 7

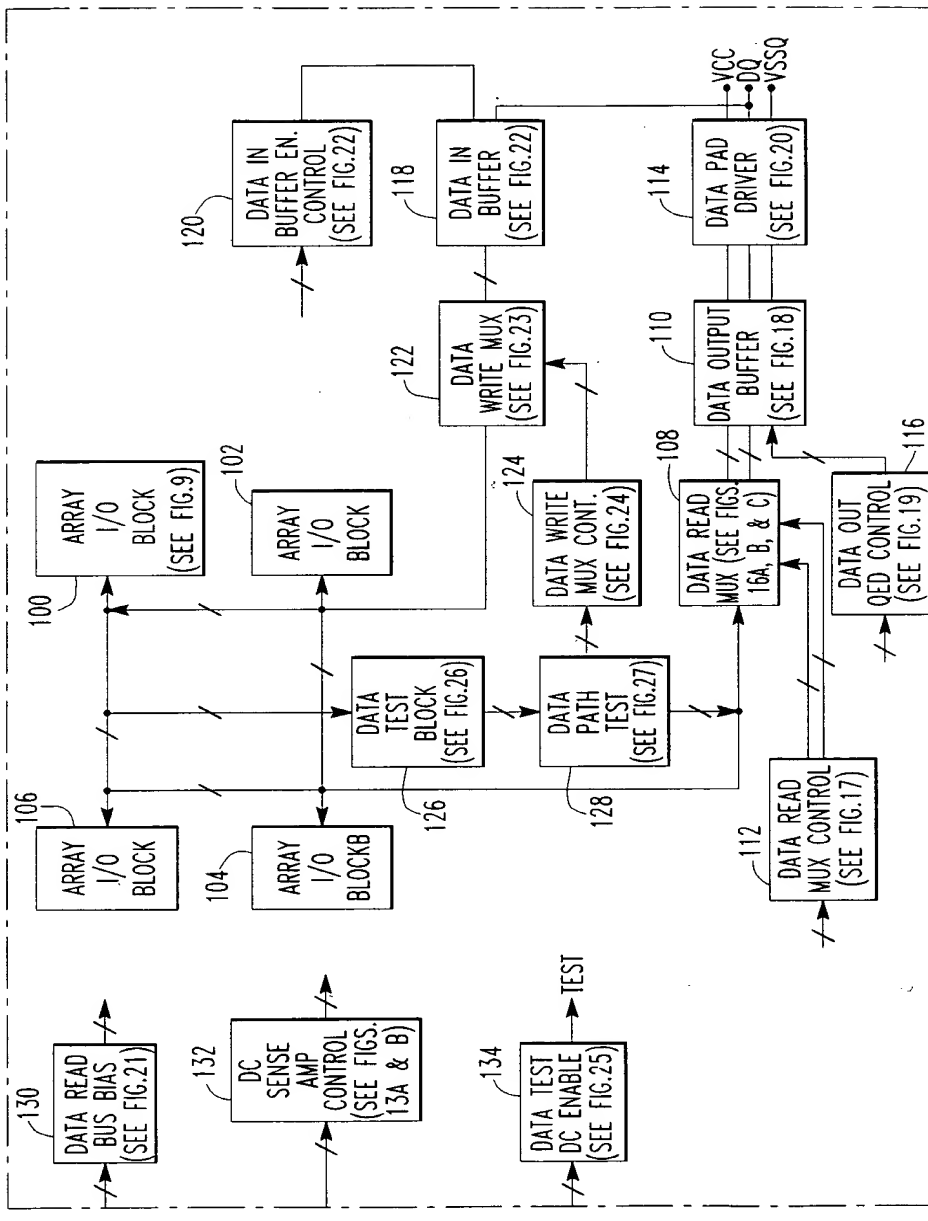

ARRAY I/O BLOCK (SEE FIG.9)
100
ARRAY I/O BLOCK
102
ARRAY I/O BLOCK
106
ARRAY I/O BLOCKB
104
DATA TEST BLOCK (SEE FIG.26)
126
DATA PATH TEST (SEE FIG.27)
128
DATA WRITE MUX CONT. (SEE FIG.24)
124
DATA WRITE MUX (SEE FIG.23)
122
DATA IN BUFFER EN. CONTROL (SEE FIG.22)
120
DATA IN BUFFER (SEE FIG.22)
118
DATA READ MUX (SEE FIGS. 16A, B, & C)
108
DATA OUTPUT BUFFER (SEE FIG.18)
110
DATA PAD DRIVER (SEE FIG.20)
114
VCC
DQ
VSSQ
DATA READ MUX CONTROL (SEE FIG.17)
112
DATA OUT QED CONTROL (SEE FIG.19)
116
DATA READ BUS BIAS (SEE FIG.21)
130
DC SENSE AMP CONTROL (SEE FIGS. 13A & B)
132
DATA TEST DC ENABLE (SEE FIG.25)
134
TEST

FIG. 8

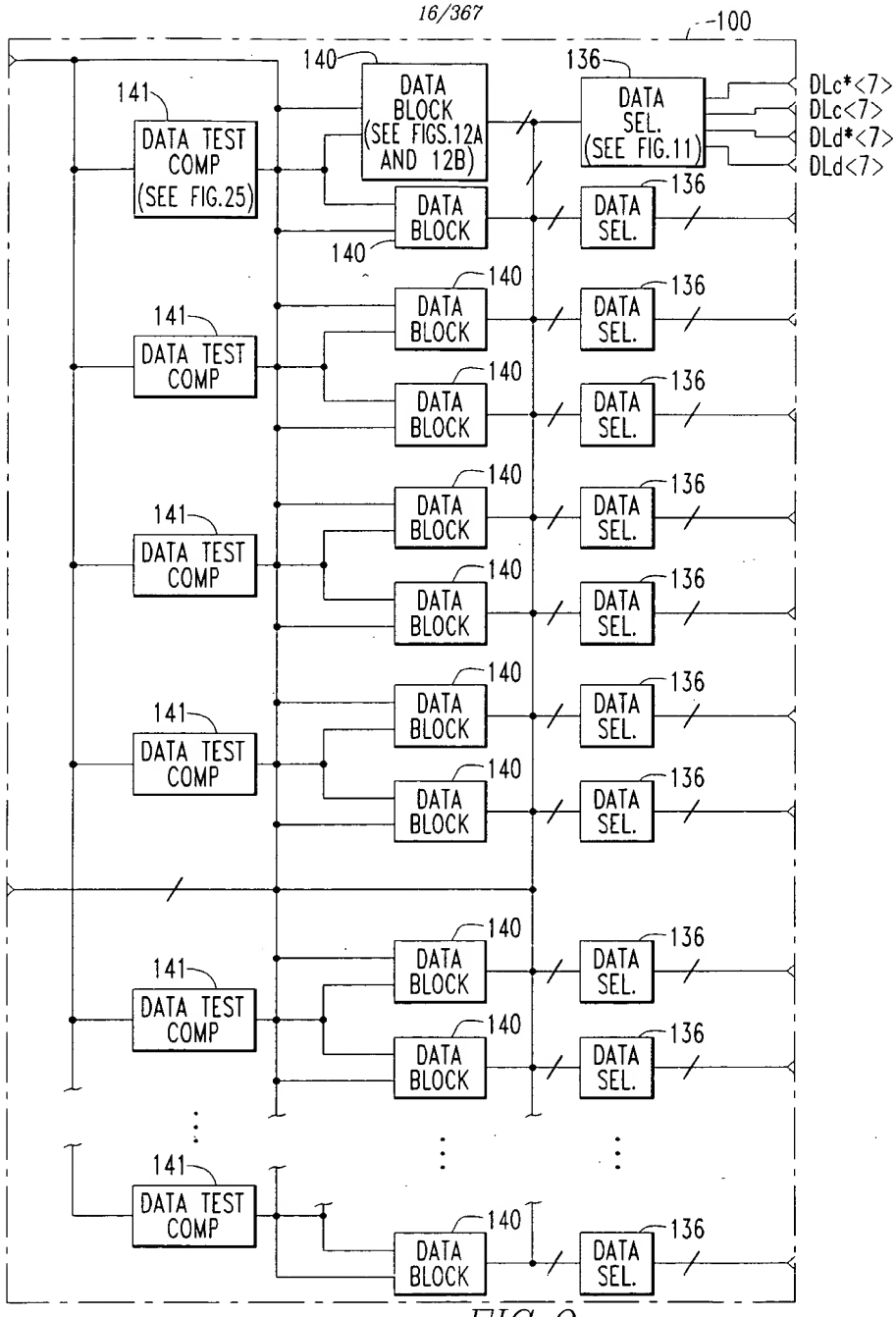

100
140
DATA BLOCK (SEE FIGS.12A AND 12B)
136
DATA SEL. (SEE FIG.11)
DLc*<7>
DLc<7>
DLd*<7>
DLd<7>
141
DATA TEST COMP (SEE FIG.25)
DATA BLOCK
DATA SEL.
DATA TEST COMP

FIG. 9

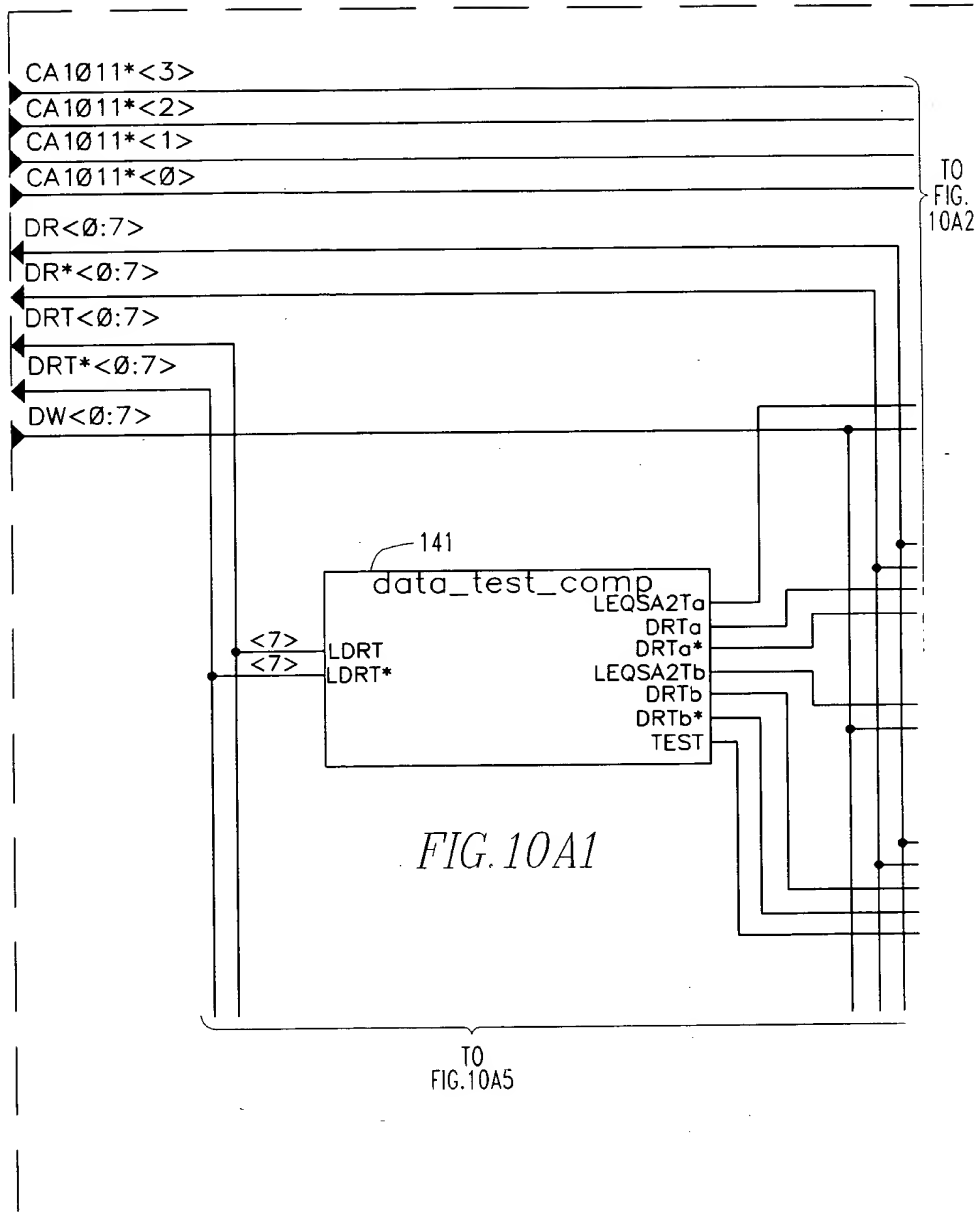

CA1Ø11*<3>
CA1Ø11*<2>
CA1Ø11*<1>
CA1Ø11*<Ø>
TO FIG. 10A2
DR<Ø:7>
DR*<Ø:7>
DRT<Ø:7>
DRT*<Ø:7>
DW<Ø:7>
141
data_test_comp
<7>
LDRT
<7>
LDRT*
LEQSA2Ta
DRTa
DRTa*
LEQSA2Tb
DRTb
DRTb*
TEST
TO FIG.10A5

FIG. 10A1

P0003-8050600

FIG. 10A2

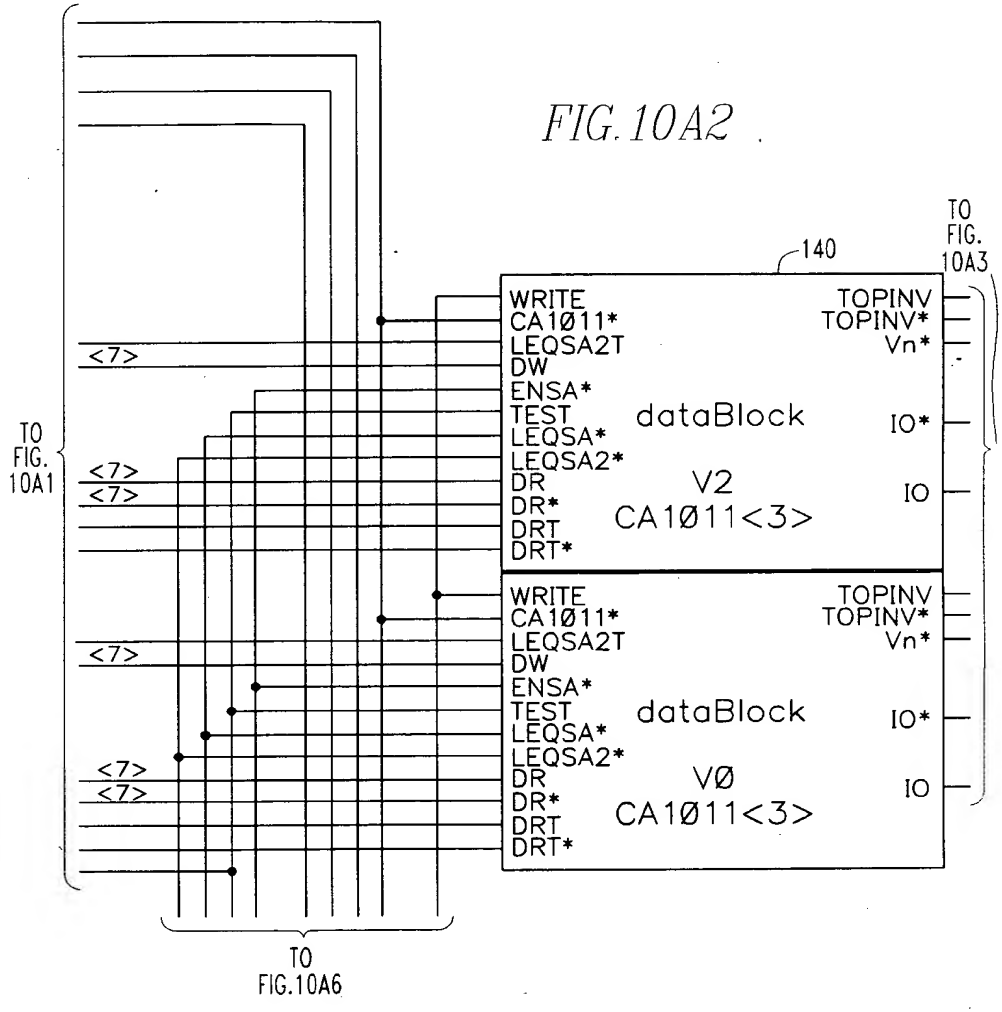
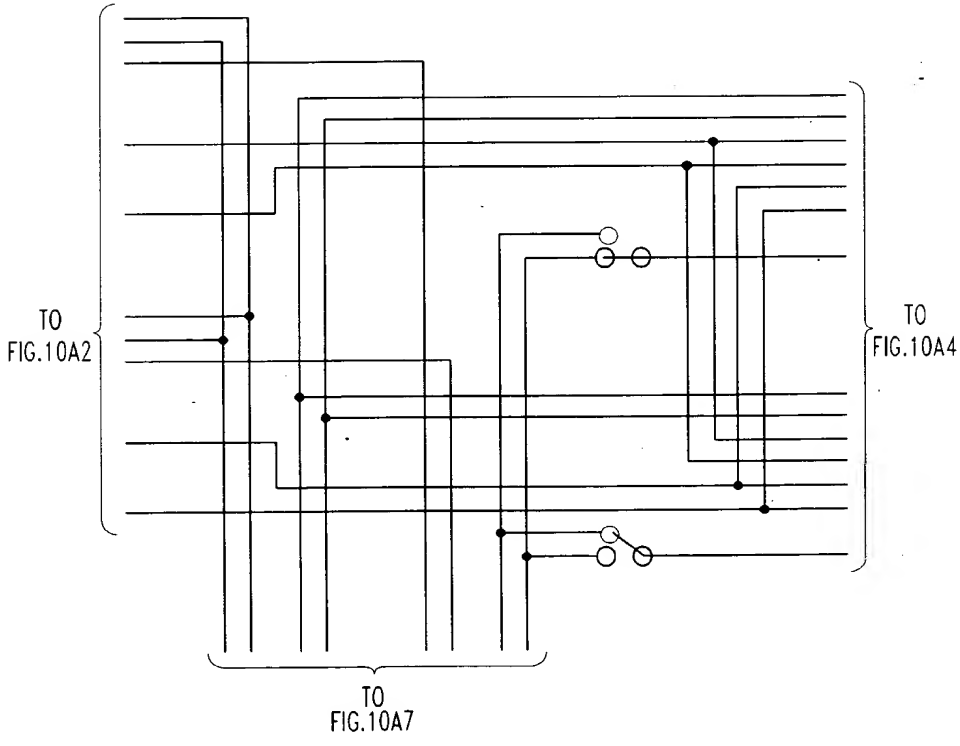


FIG. 10A3



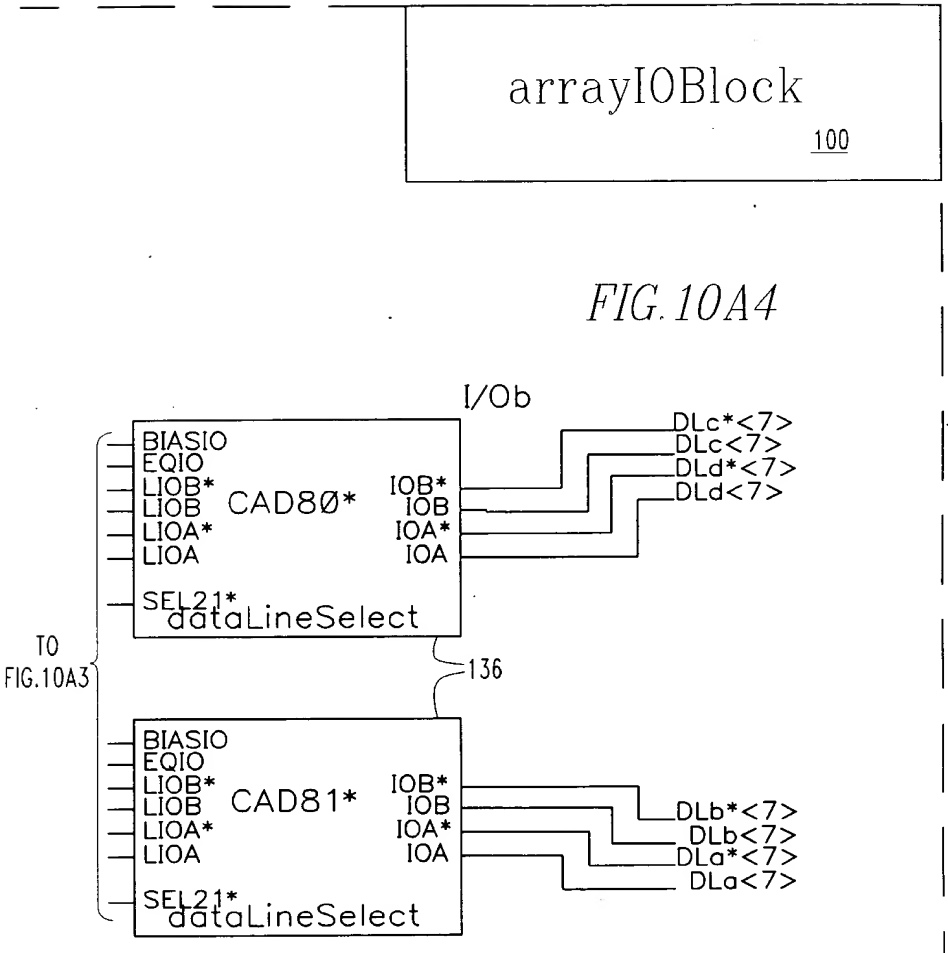

arrayIOBlock
100
I/Ob
BIASIO
EQIO
LIOB*
LIOB
LIOA*
LIOA
CAD80*
IOB*
IOB
IOA*
IOA
SEL21*
dataLineSelect
DLc*<7>
DLc<7>
DLd*<7>
DLd<7>
TO
FIG.10A3
136
BIASIO
EQIO
LIOB*
LIOB
LIOA*
LIOA
CAD81*
IOB*
IOB
IOA*
IOA
SEL21*
dataLineSelect
DLb*<7>
DLb<7>
DLa*<7>
DLa<7>

FIG.10A4

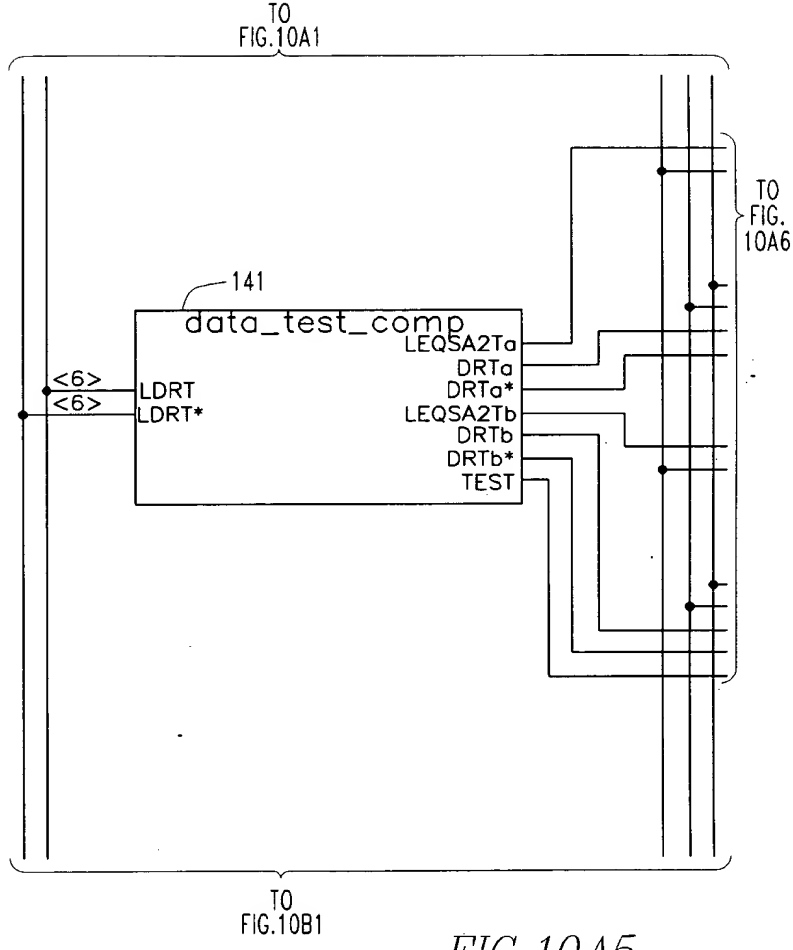

TO
FIG.10A1
TO
FIG.
10A6
141
data_test_comp
<6>
<6>
LDRT
LDRT*
LEQSA2Ta
DRTa
DRTa*
LEQSA2Tb
DRTb
DRTb*
TEST
TO
FIG.10B1

FIG. 10A5

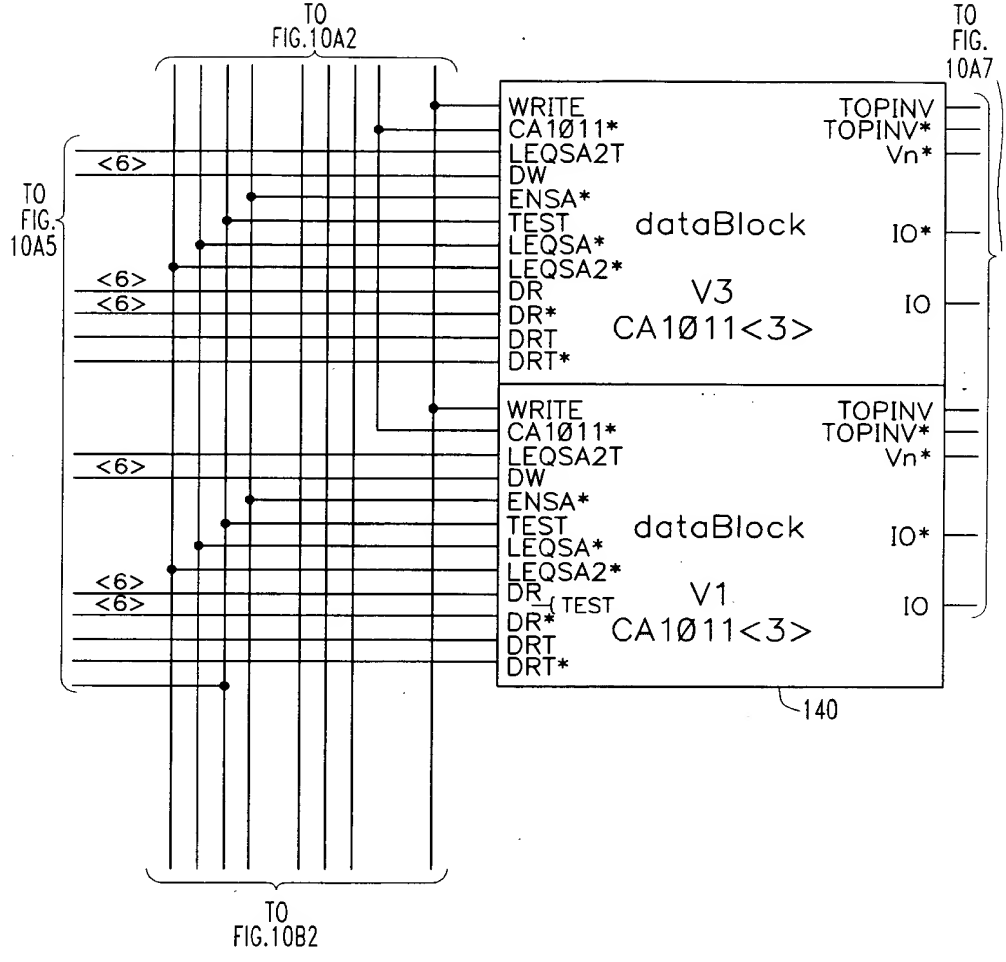

TO FIG.10A2
TO FIG. 10A7
TO FIG. 10A5
TO FIG.10B2
WRITE
CA1Ø11*
LEQSA2T
DW
ENSA*
TEST
LEQSA*
LEQSA2*
DR
DR*
DRT
DRT*
dataBlock
V3
CA1Ø11<3>
TOPINV
TOPINV*
Vn*
IO*
IO
<6>
dataBlock
V1
CA1Ø11<3>
140

FIG. 10A6

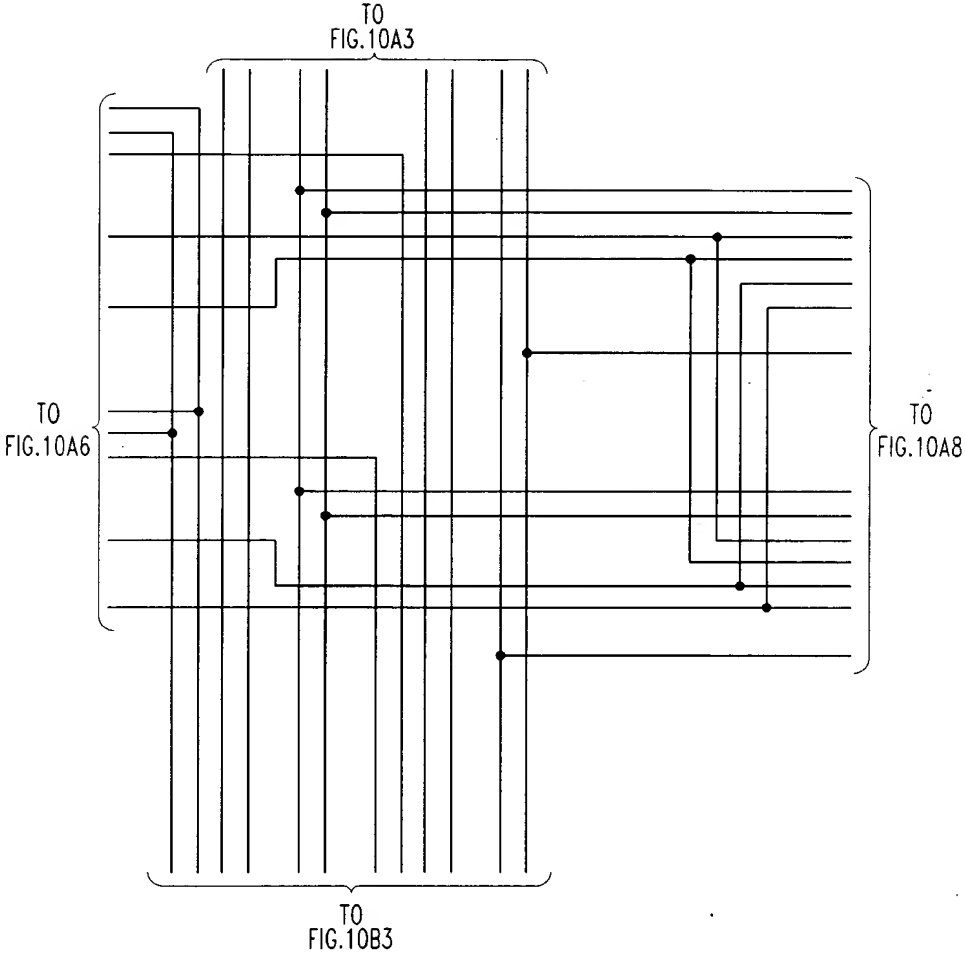


FIG.10A7

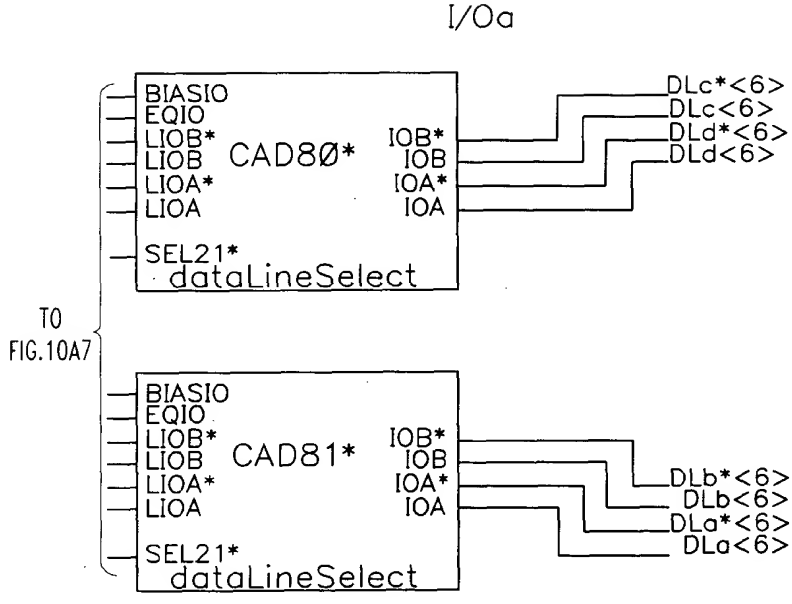

I/Oa
BIASIO
EQIO
LIOB*
LIOB
LIOA*
LIOA
CAD80*
IOB*
IOB
IOA*
IOA
SEL21*
dataLineSelect
DLc*<6>
DLc<6>
DLd*<6>
DLd<6>
TO
FIG.10A7
BIASIO
EQIO
LIOB*
LIOB
LIOA*
LIOA
CAD81*
IOB*
IOB
IOA*
IOA
SEL21*
dataLineSelect
DLb*<6>
DLb<6>
DLa*<6>
DLa<6>

FIG. 10A8

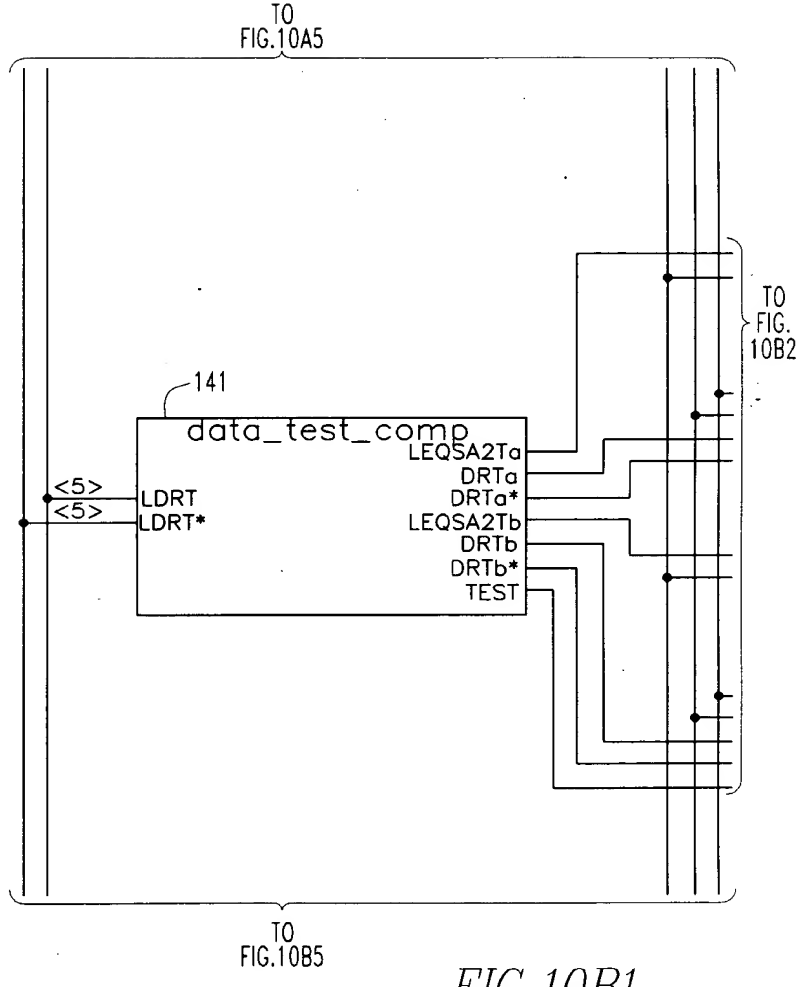

TO
FIG.10A5
TO
FIG.
10B2
141
data_test_comp
<5>
LDRT
<5>
LDRT*
LEQSA2Ta
DRTa
DRTa*
LEQSA2Tb
DRTb
DRTb*
TEST
TO
FIG.10B5

FIG. 10B1

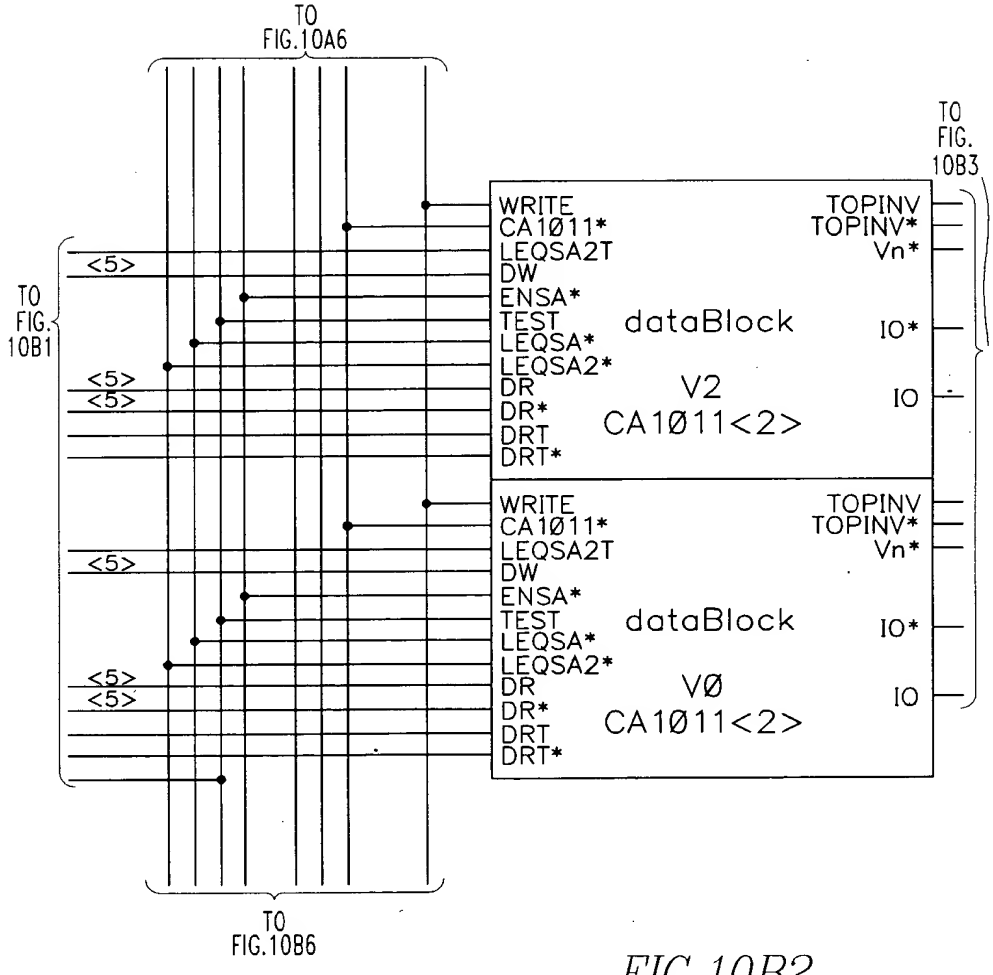

TO
FIG.10A6
TO
FIG.
10B3
TO
FIG.
10B1
<5>
<5>
<5>
<5>
<5>
WRITE
CA1Ø11*
LEQSA2T
DW
ENSA*
TEST
LEQSA*
LEQSA2*
DR
DR*
DRT
DRT*
dataBlock
V2
CA1Ø11<2>
TOPINV
TOPINV*
Vn*
IO*
IO
WRITE
CA1Ø11*
LEQSA2T
DW
ENSA*
TEST
LEQSA*
LEQSA2*
DR
DR*
DRT
DRT*
dataBlock
VØ
CA1Ø11<2>
TOPINV
TOPINV*
Vn*
IO*
IO
TO
FIG.10B6

FIG. 10B2

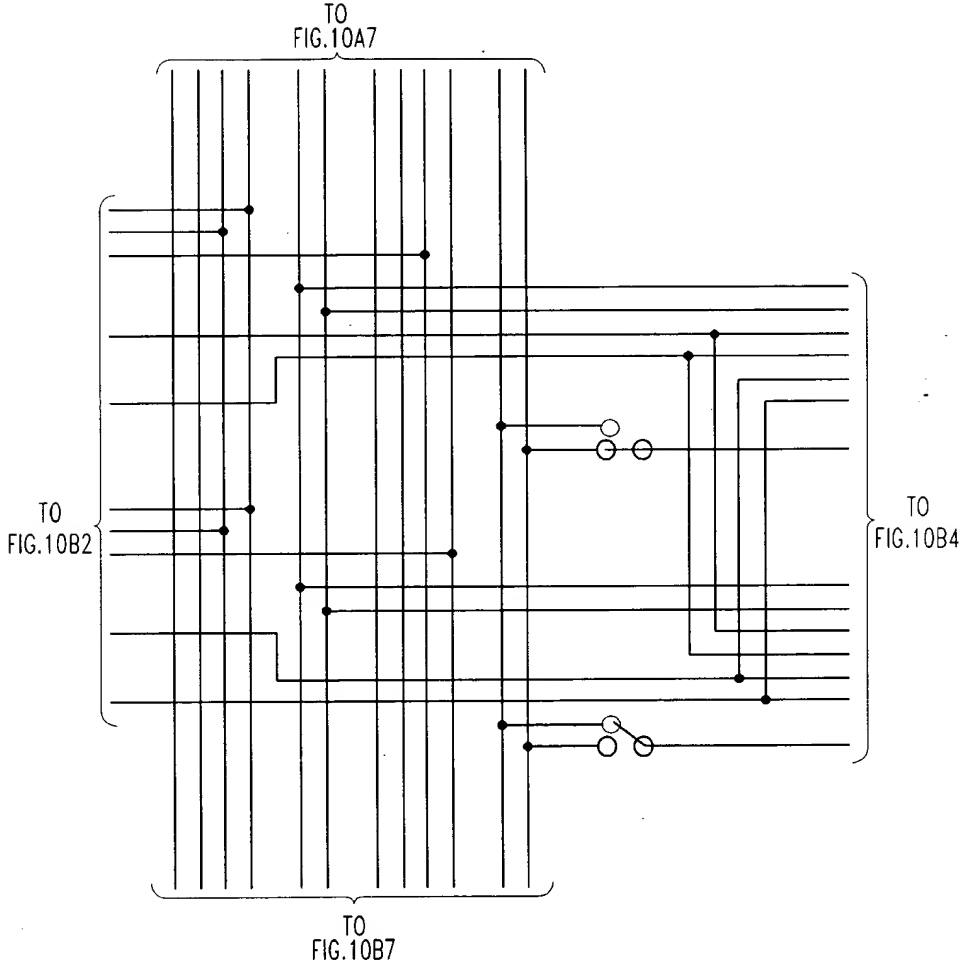


FIG. 10B3

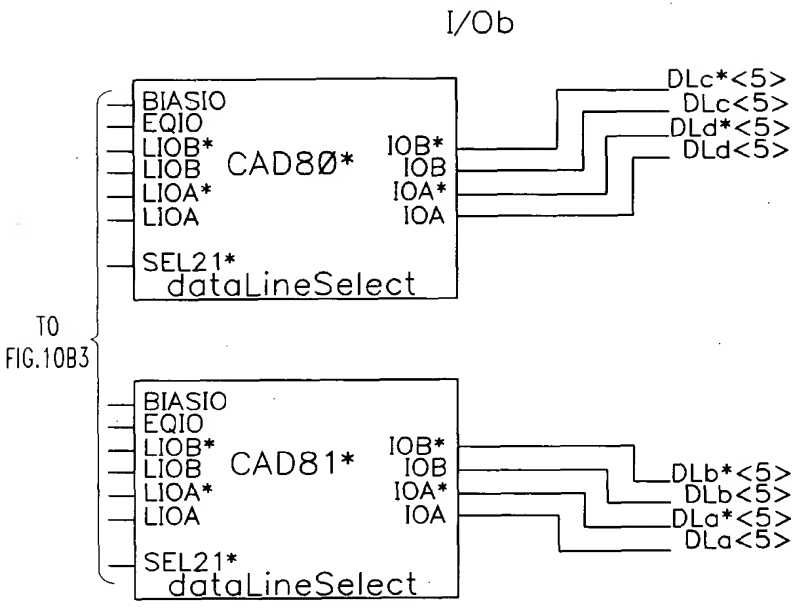

I/Ob
BIASIO
EQIO
LIOB*
LIOB
LIOA*
LIOA
CAD8Ø*
SEL21*
dataLineSelect
IOB*
IOB
IOA*
IOA
DLc*<5>
DLc<5>
DLd*<5>
DLd<5>
TO
FIG.10B3
BIASIO
EQIO
LIOB*
LIOB
LIOA*
LIOA
CAD81*
SEL21*
dataLineSelect
IOB*
IOB
IOA*
IOA
DLb*<5>
DLb<5>
DLa*<5>
DLa<5>

FIG. 10B4

FIG. 10B5

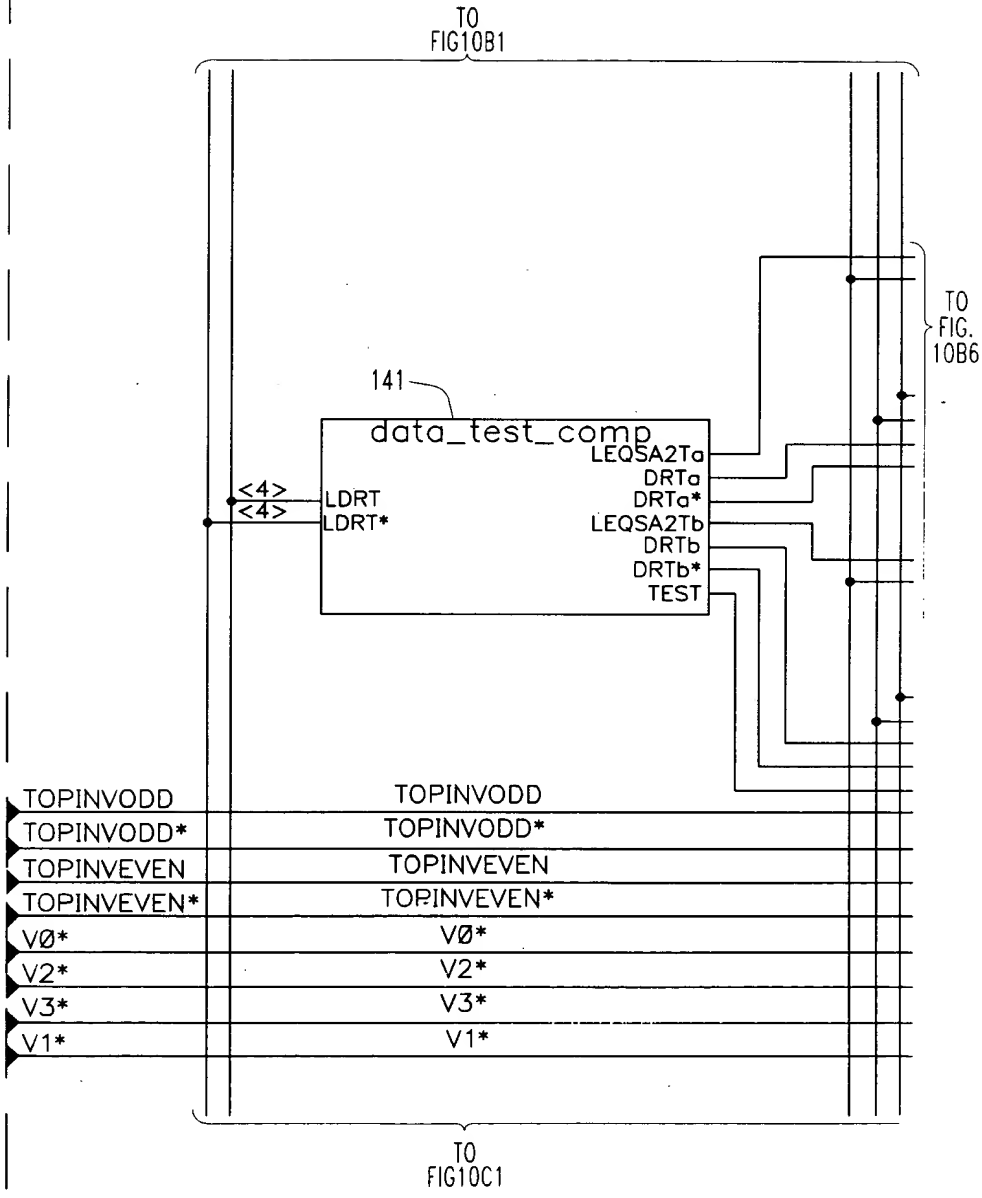

TO
FIG10B1
TO
FIG.
10B6
141
data_test_comp
LEQSA2Ta
DRTa
DRTa*
LEQSA2Tb
DRTb
DRTb*
TEST
<4>
<4>
LDRT
LDRT*
TOPINVODD
TOPINVODD*
TOPINVEVEN
TOPINVEVEN*
V0*
V2*
V3*
V1*
TOPINVODD
TOPINVODD*
TOPINVEVEN
TOPINVEVEN*
V0*
V2*
V3*
V1*
TO
FIG10C1

FIG. 10B6

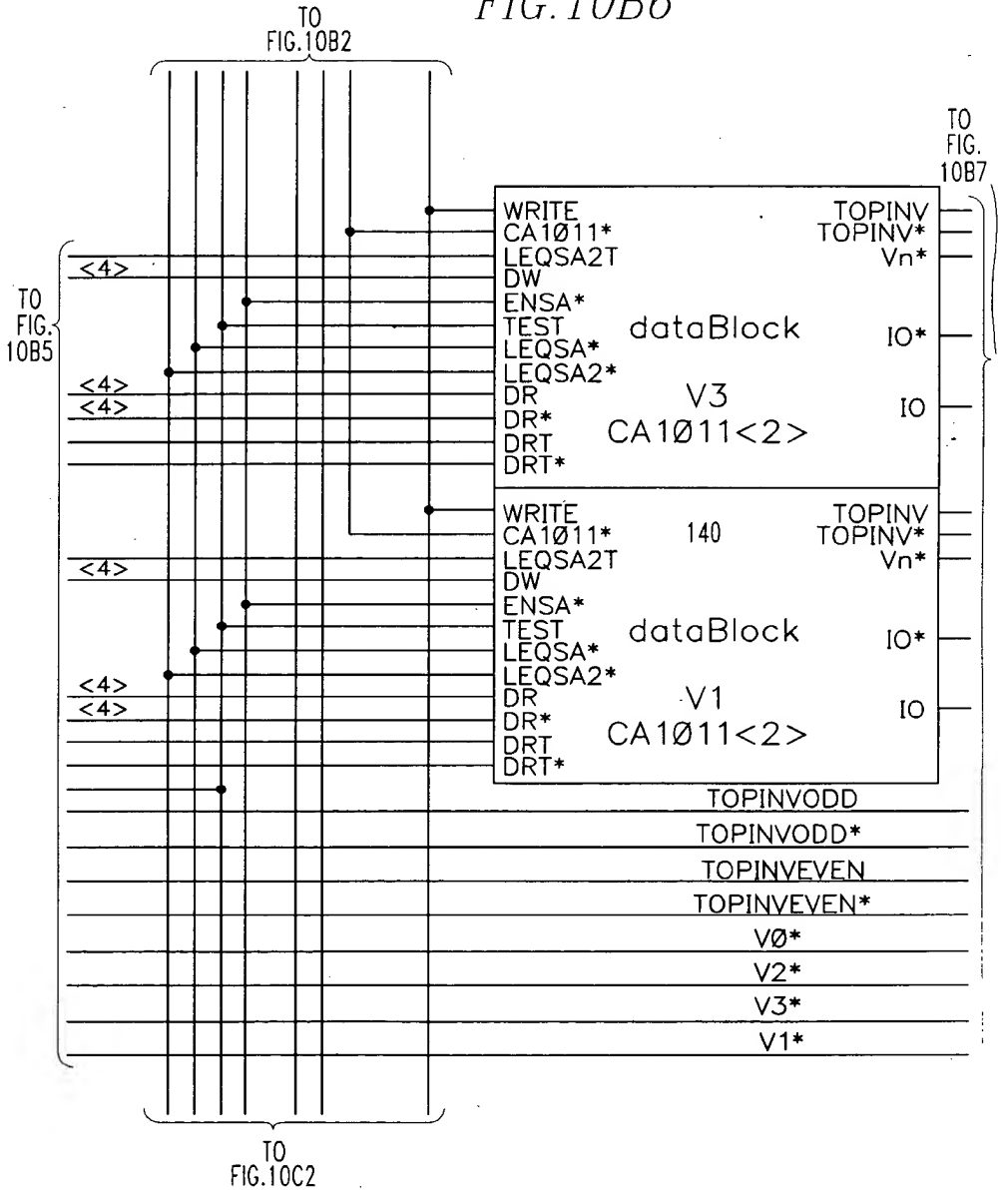

TO FIG.10B2
TO FIG. 10B7
TO FIG. 10B5
<4>
<4>
<4>
<4>
<4>
WRITE
CA1Ø11*
LEQSA2T
DW
ENSA*
TEST
LEQSA*
LEQSA2*
DR
DR*
DRT
DRT*
dataBlock
V3
CA1Ø11<2>
TOPINV
TOPINV*
Vn*
IO*
IO
140
dataBlock
V1
CA1Ø11<2>
TOPINVODD
TOPINVODD*
TOPINVEVEN
TOPINVEVEN*
VØ*
V2*
V3*
V1*
TO FIG.10C2

FIG. 10B7

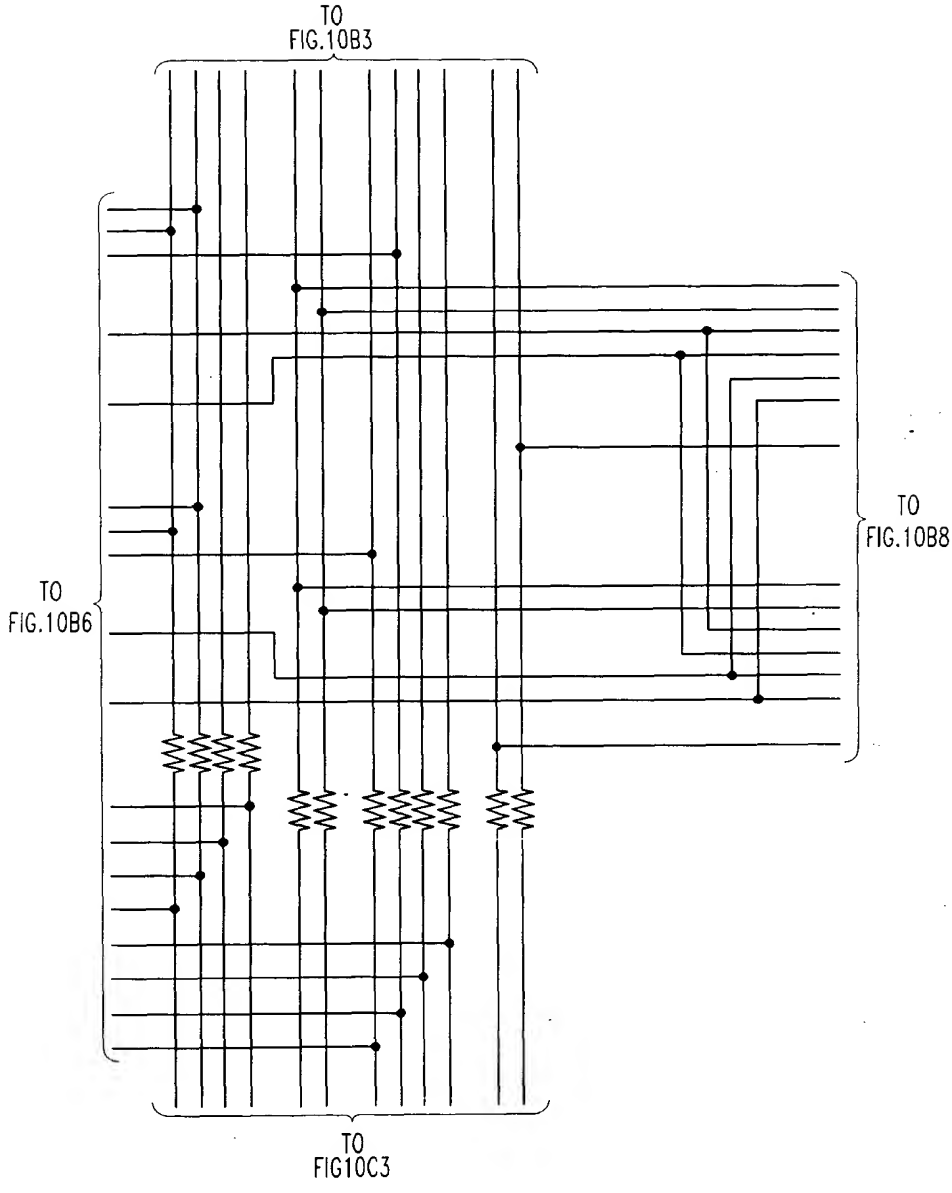
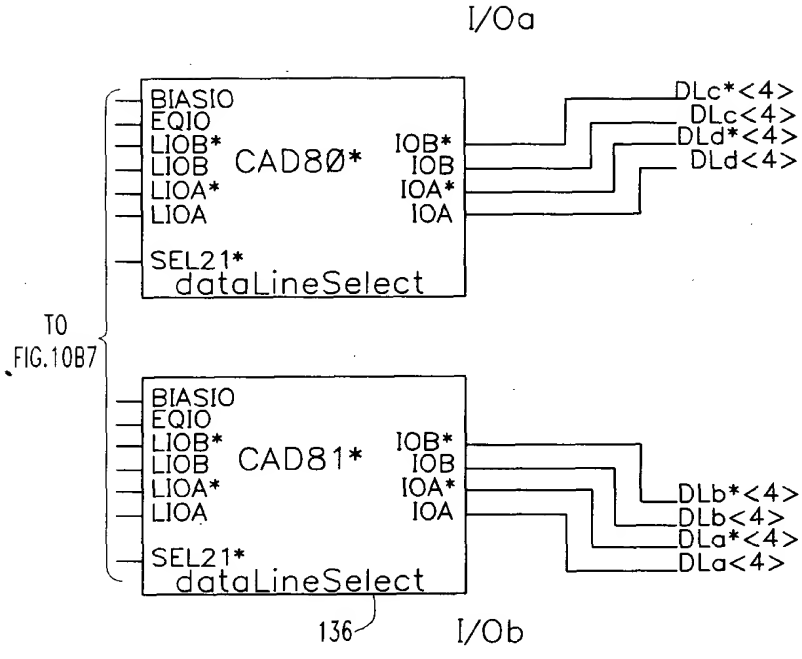


FIG. 10B8


I/Oa
BIASIO
EQIO
LIOB*
LIOB
LIOA*
LIOA
CAD80*
IOB*
IOB
IOA*
IOA
SEL21*
dataLineSelect
DLc*<4>
DLc<4>
DLd*<4>
DLd<4>
TO
FIG.10B7
BIASIO
EQIO
LIOB*
LIOB
LIOA*
LIOA
CAD81*
IOB*
IOB
IOA*
IOA
SEL21*
dataLineSelect
DLb*<4>
DLb<4>
DLa*<4>
DLa<4>
136
I/Ob

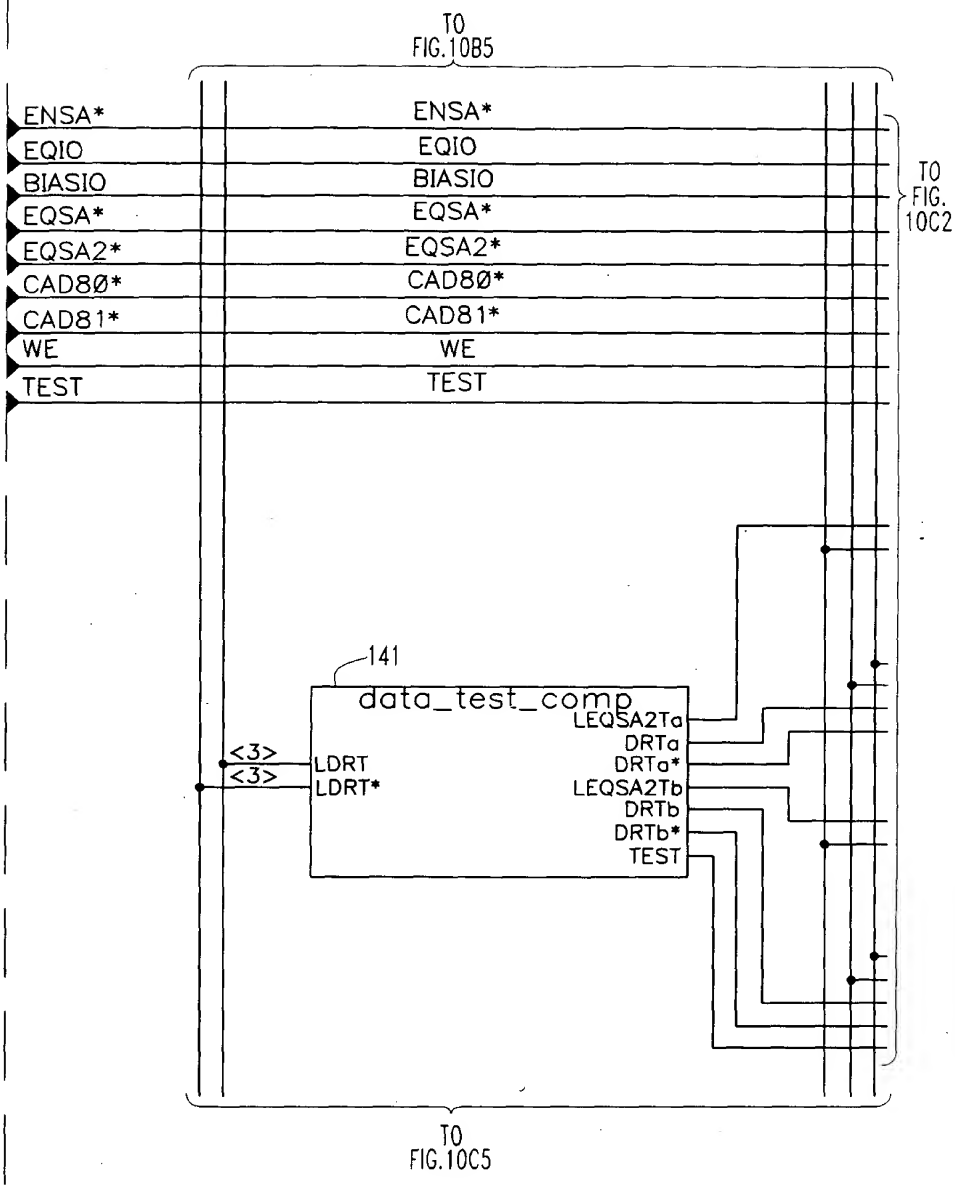

TO
FIG.10B5
ENSA*
EQIO
BIASIO
EQSA*
EQSA2*
CAD8Ø*
CAD81*
WE
TEST
TO
FIG.
10C2
141
data_test_comp
<3>
LDRT
<3>
LDRT*
LEQSA2Ta
DRTa
DRTa*
LEQSA2Tb
DRTb
DRTb*
TEST
TO
FIG.10C5

FIG. 10C1

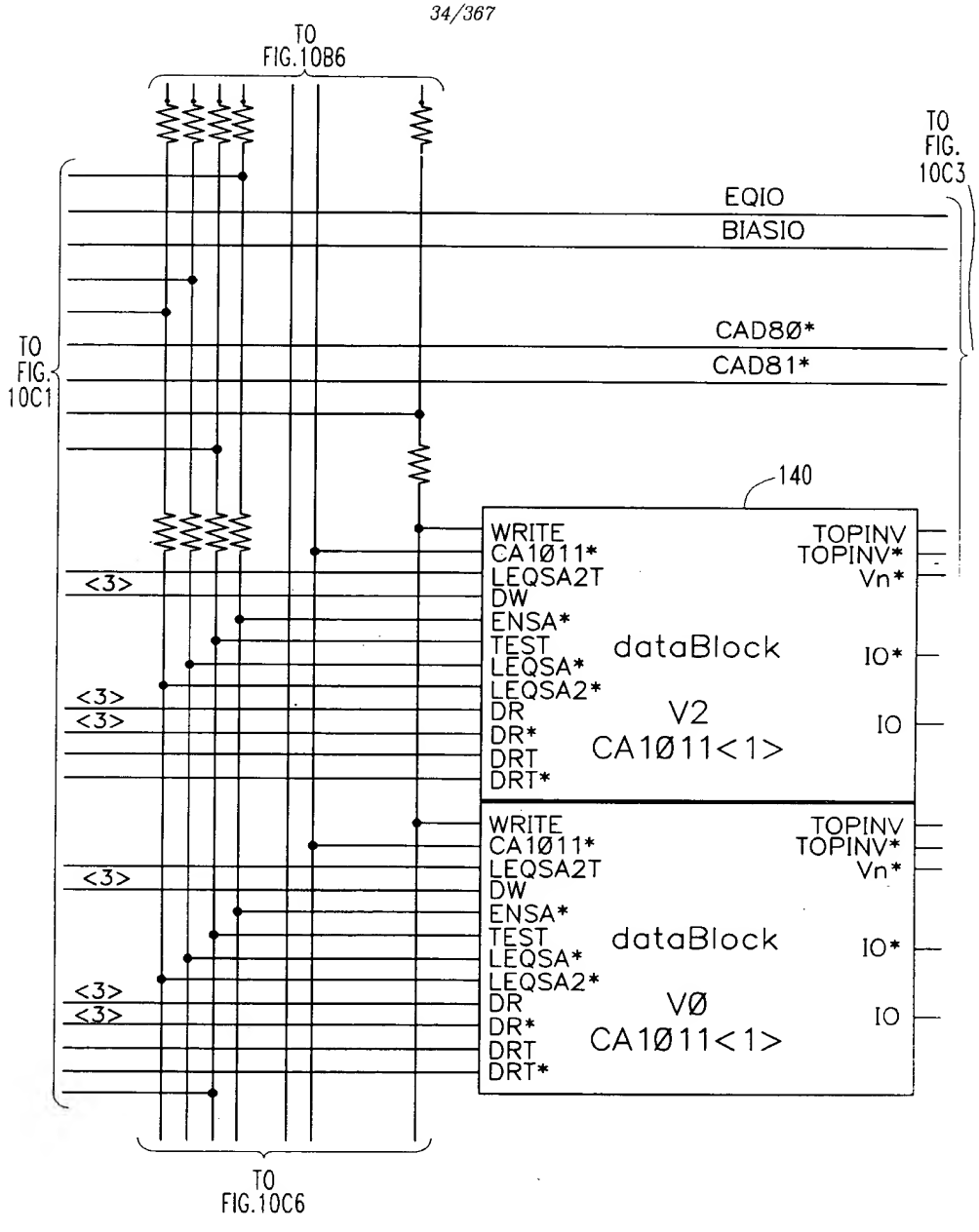

TO
FIG.10B6
TO
FIG.
10C3
EQIO
BIASIO
CAD8Ø*
CAD81*
TO
FIG.
10C1
140
WRITE
CA1Ø11*
LEQSA2T
DW
ENSA*
TEST
LEQSA*
LEQSA2*
DR
DR*
DRT
DRT*
dataBlock
V2
CA1Ø11<1>
TOPINV
TOPINV*
Vn*
IO*
IO
<3>
WRITE
CA1Ø11*
LEQSA2T
DW
ENSA*
TEST
LEQSA*
LEQSA2*
DR
DR*
DRT
DRT*
dataBlock
VØ
CA1Ø11<1>
TOPINV
TOPINV*
Vn*
IO*
IO
TO
FIG.10C6

FIG. 10C2

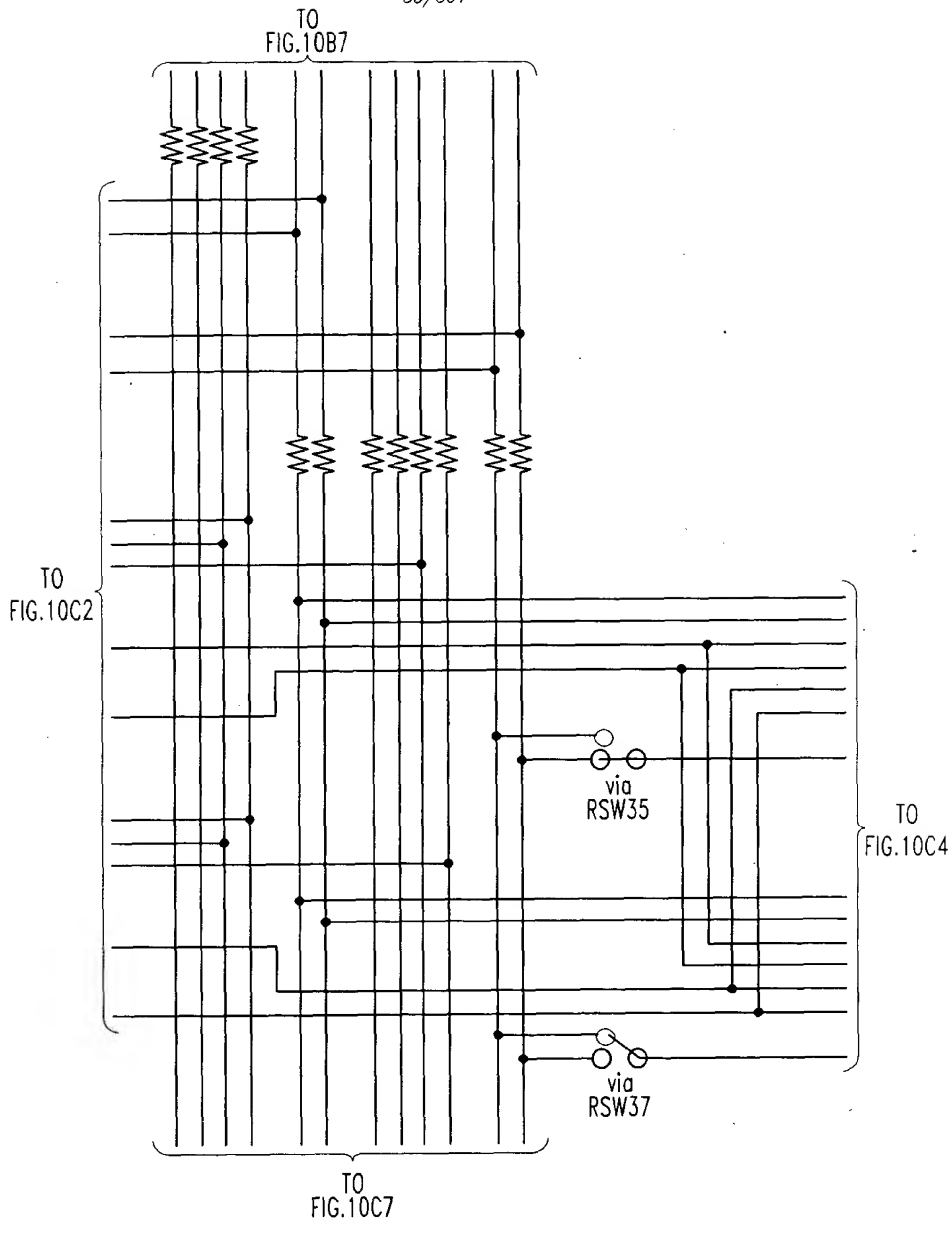
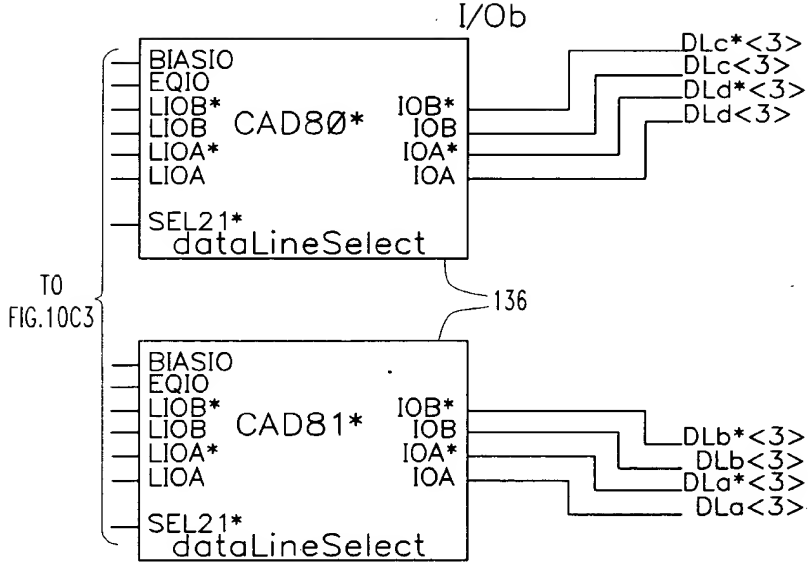

TO
FIG.10B7
TO
FIG.10C2
via
RSW35
TO
FIG.10C4
via
RSW37
TO
FIG.10C7

FIG. 10C3

FIG. 10C4


I/Ob
BIASIO
EQIO
LIOB*
LIOB
LIOA*
LIOA
CAD80*
IOB*
IOB
IOA*
IOA
SEL21*
dataLineSelect
DLc*<3>
DLc<3>
DLd*<3>
DLd<3>
TO
FIG.10C3
136
BIASIO
EQIO
LIOB*
LIOB
LIOA*
LIOA
CAD81*
IOB*
IOB
IOA*
IOA
SEL21*
dataLineSelect
DLb*<3>
DLb<3>
DLa*<3>
DLa<3>

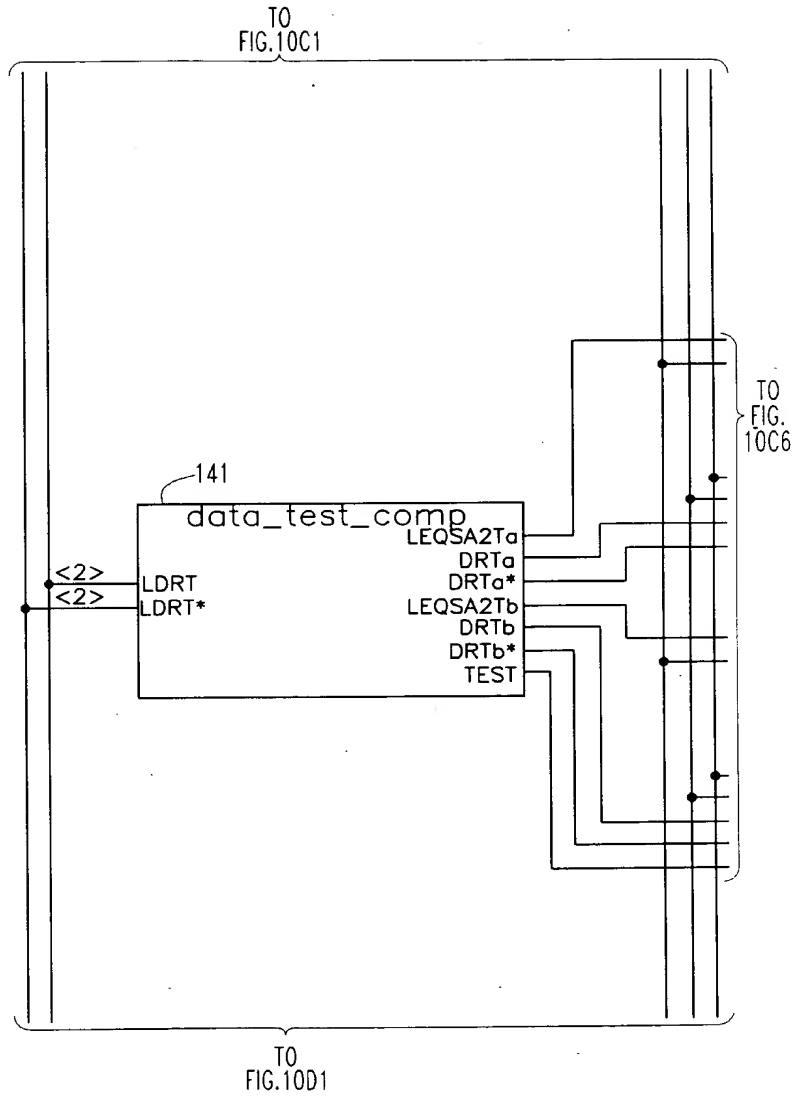

TO
FIG.10C1
TO
FIG.
10C6
141
data_test_comp
<2>
<2>
LDRT
LDRT*
LEQSA2Ta
DRTa
DRTa*
LEQSA2Tb
DRTb
DRTb*
TEST
TO
FIG.10D1

FIG. 10C5

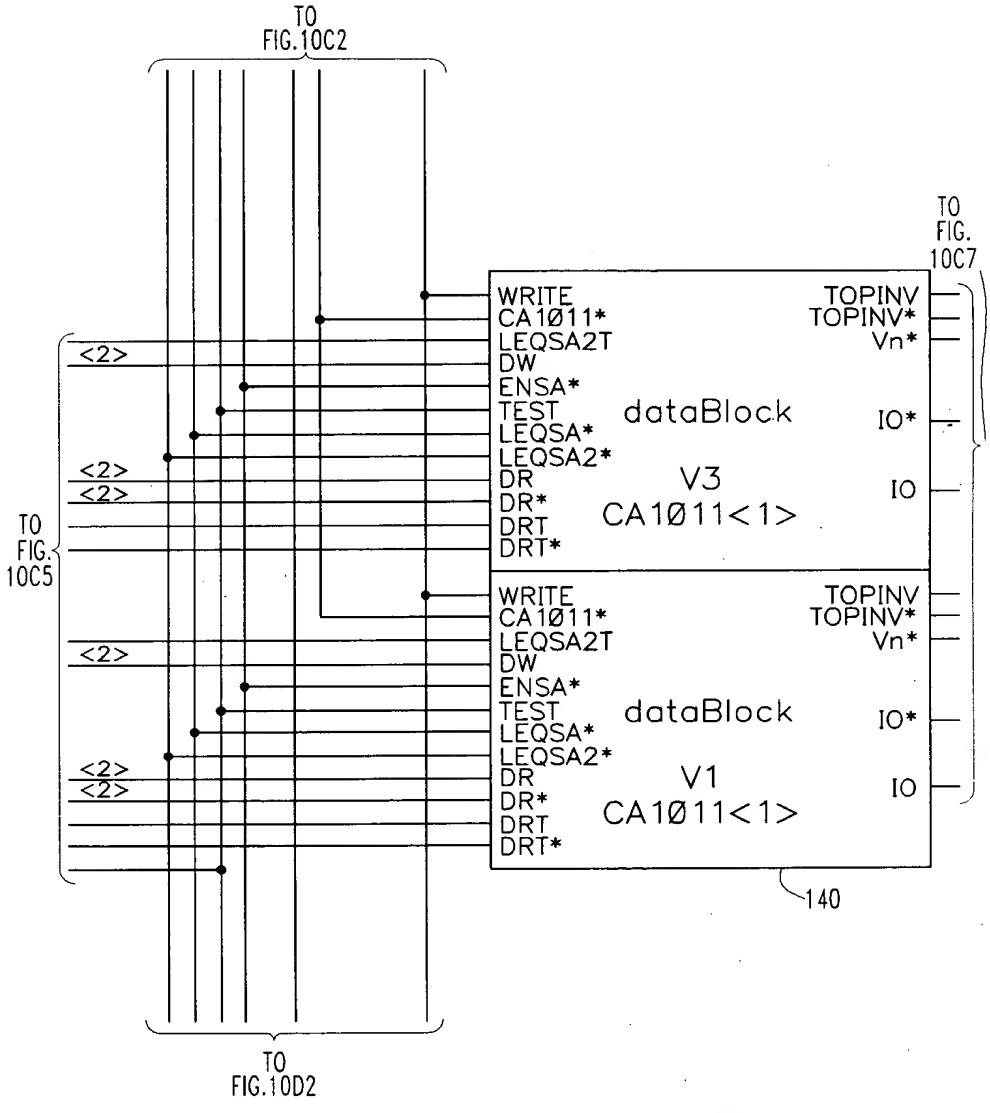

TO
FIG.10C2
TO
FIG.
10C7
TO
FIG.
10C5
TO
FIG.10D2
WRITE
CA1Ø11*
LEQSA2T
DW
ENSA*
TEST
LEQSA*
LEQSA2*
DR
DR*
DRT
DRT*
dataBlock
V3
CA1Ø11<1>
TOPINV
TOPINV*
Vn*
IO*
IO
<2>
<2>
<2>
<2>
<2>
WRITE
CA1Ø11*
LEQSA2T
DW
ENSA*
TEST
LEQSA*
LEQSA2*
DR
DR*
DRT
DRT*
dataBlock
V1
CA1Ø11<1>
TOPINV
TOPINV*
Vn*
IO*
IO
140

FIG. 10C6

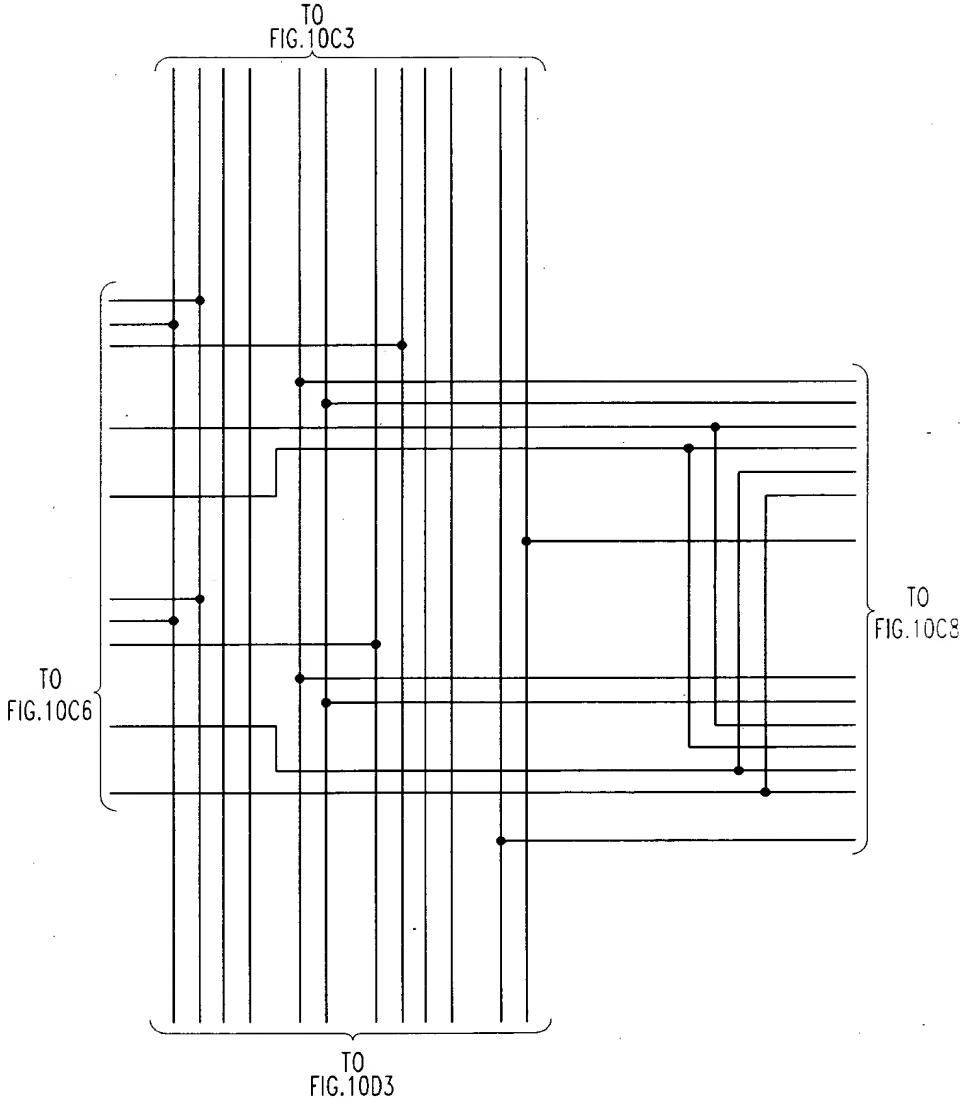


FIG.10C7

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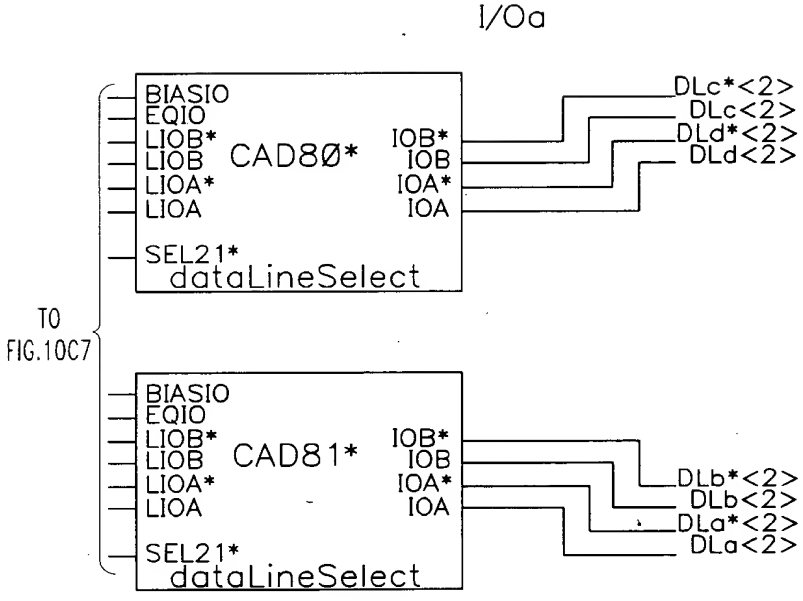


FIG. 10C8

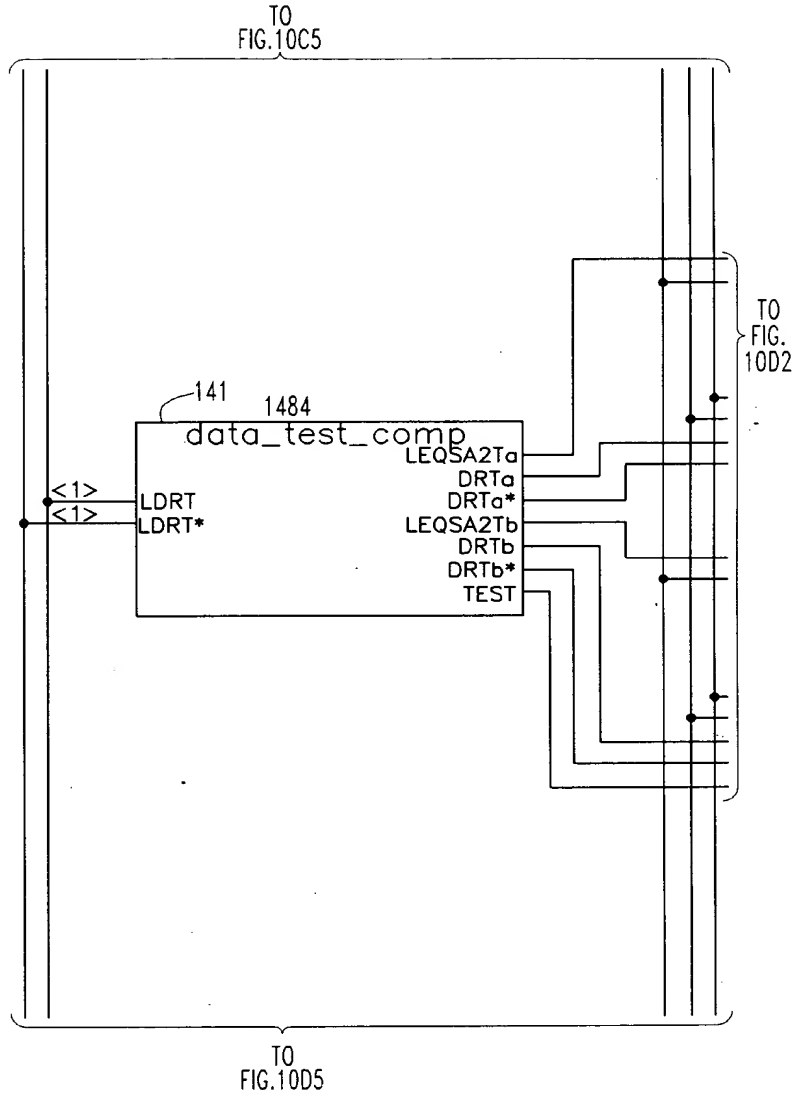

TO
FIG.10C5
TO
FIG.
10D2
141
1484
data_test_comp
LEQSA2Ta
DRTa
DRTa*
LEQSA2Tb
DRTb
DRTb*
TEST
<1>
LDRT
<1>
LDRT*
TO
FIG.10D5

FIG. 10D1

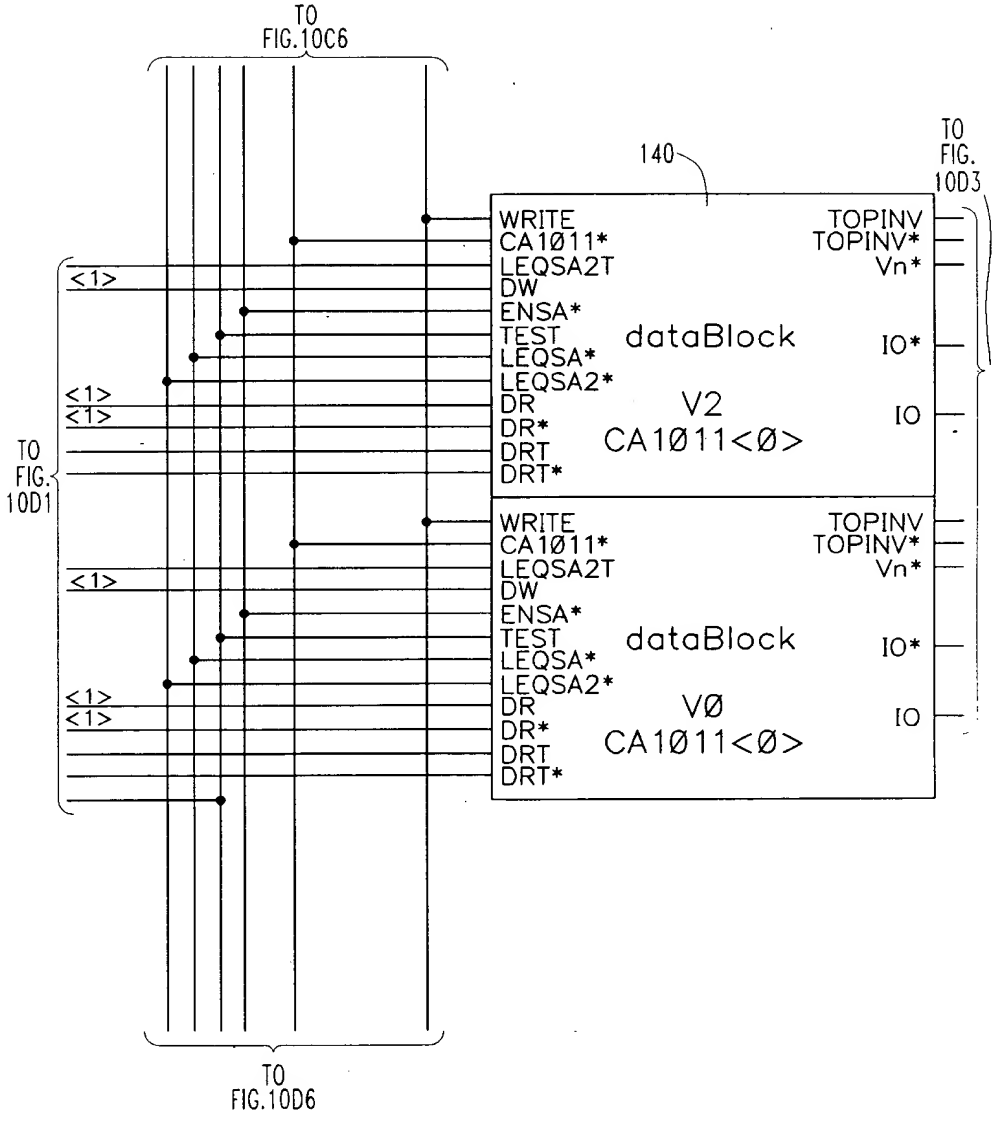

TO
FIG.10C6
140
TO
FIG.
10D3
WRITE
CA1Ø11*
LEQSA2T
DW
ENSA*
TEST
LEQSA*
LEQSA2*
DR
DR*
DRT
DRT*
dataBlock
V2
CA1Ø11<Ø>
TOPINV
TOPINV*
Vn*
IO*
IO
TO
FIG.
10D1
<1>
WRITE
CA1Ø11*
LEQSA2T
DW
ENSA*
TEST
LEQSA*
LEQSA2*
DR
DR*
DRT
DRT*
dataBlock
VØ
CA1Ø11<Ø>
TOPINV
TOPINV*
Vn*
IO*
IO
TO
FIG.10D6

FIG. 10D2

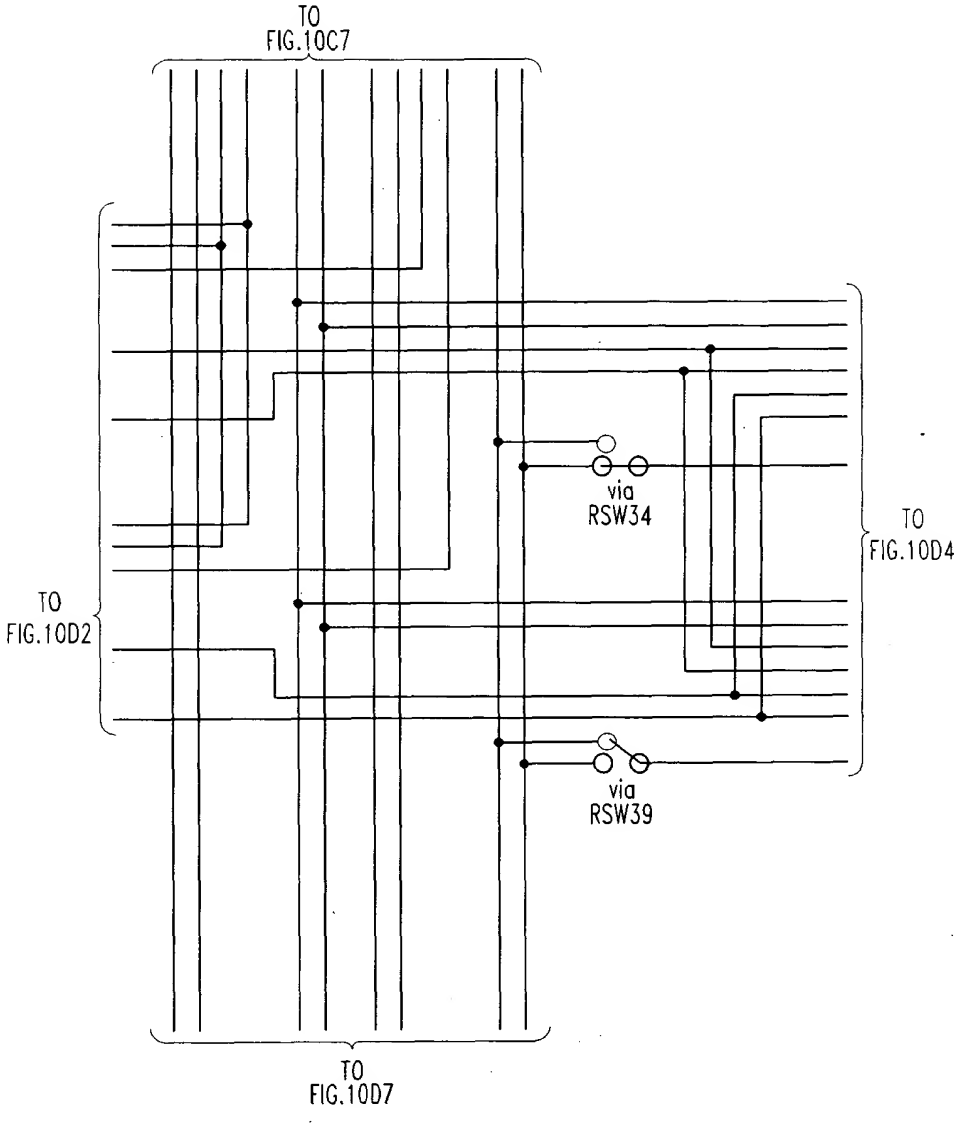

TO
FIG.10C7
TO
FIG.10D2
via
RSW34
TO
FIG.10D4
via
RSW39
TO
FIG.10D7

FIG.10D3

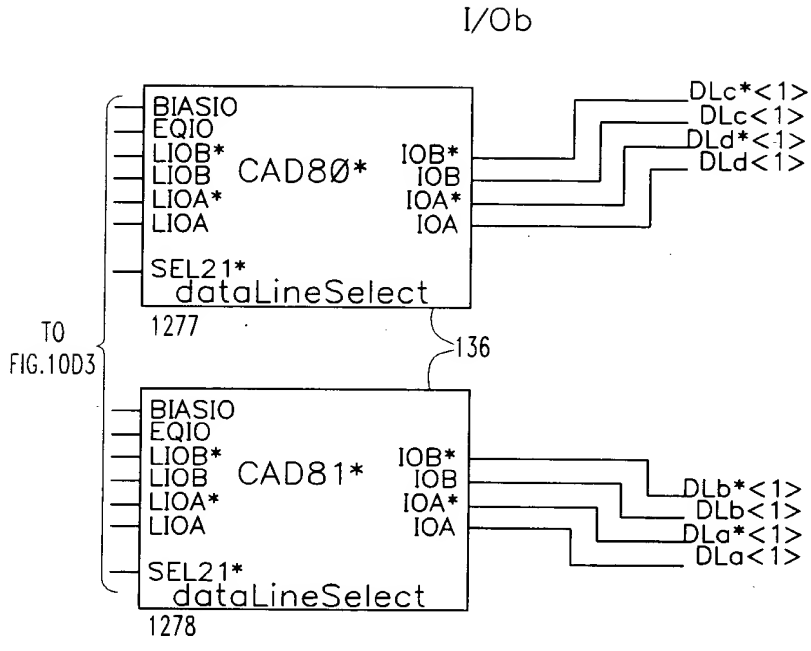

I/Ob
BIASIO
EQIO
LIOB*
LIOB
LIOA*
LIOA
CAD80*
IOB*
IOB
IOA*
IOA
SEL21*
dataLineSelect
1277
DLc*<1>
DLc<1>
DLd*<1>
DLd<1>
TO
FIG.10D3
136
BIASIO
EQIO
LIOB*
LIOB
LIOA*
LIOA
CAD81*
IOB*
IOB
IOA*
IOA
SEL21*
dataLineSelect
1278
DLb*<1>
DLb<1>
DLa*<1>
DLa<1>

FIG. 10D4

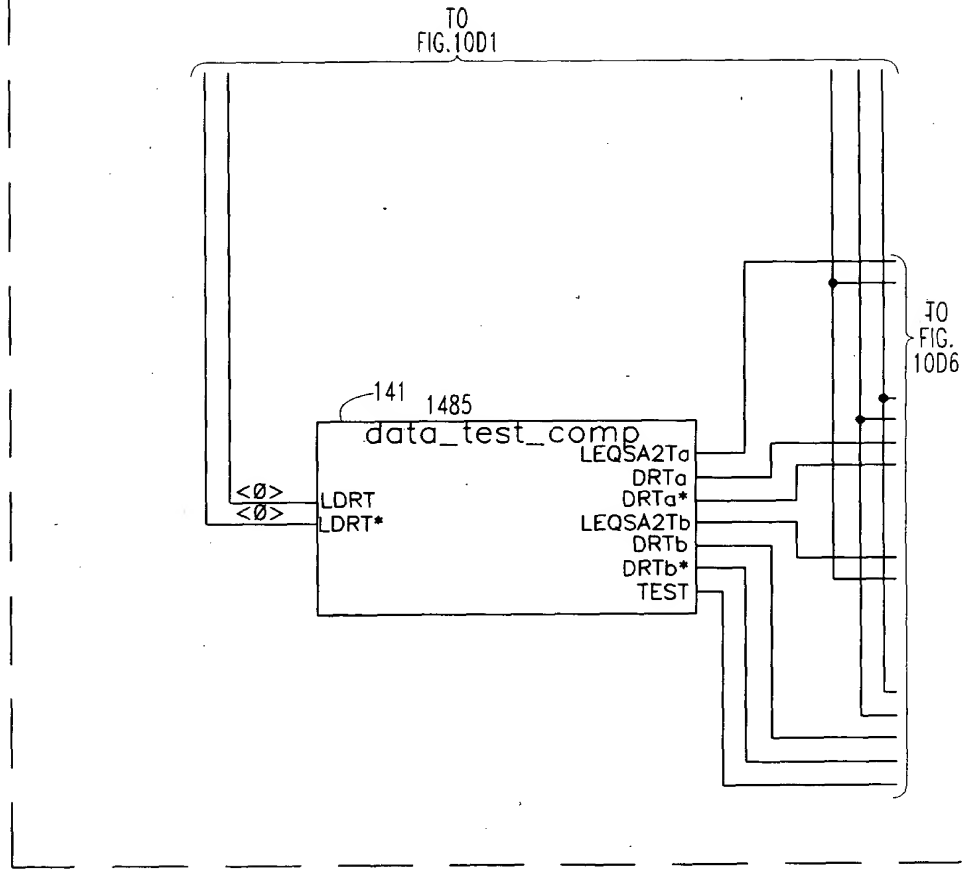

TO
FIG.10D1
TO
FIG.
10D6
141
1485
data_test_comp
LEQSA2Ta
DRTa
DRTa*
LEQSA2Tb
DRTb
DRTb*
TEST
<0>
LDRT
<0>
LDRT*

FIG. 10D5

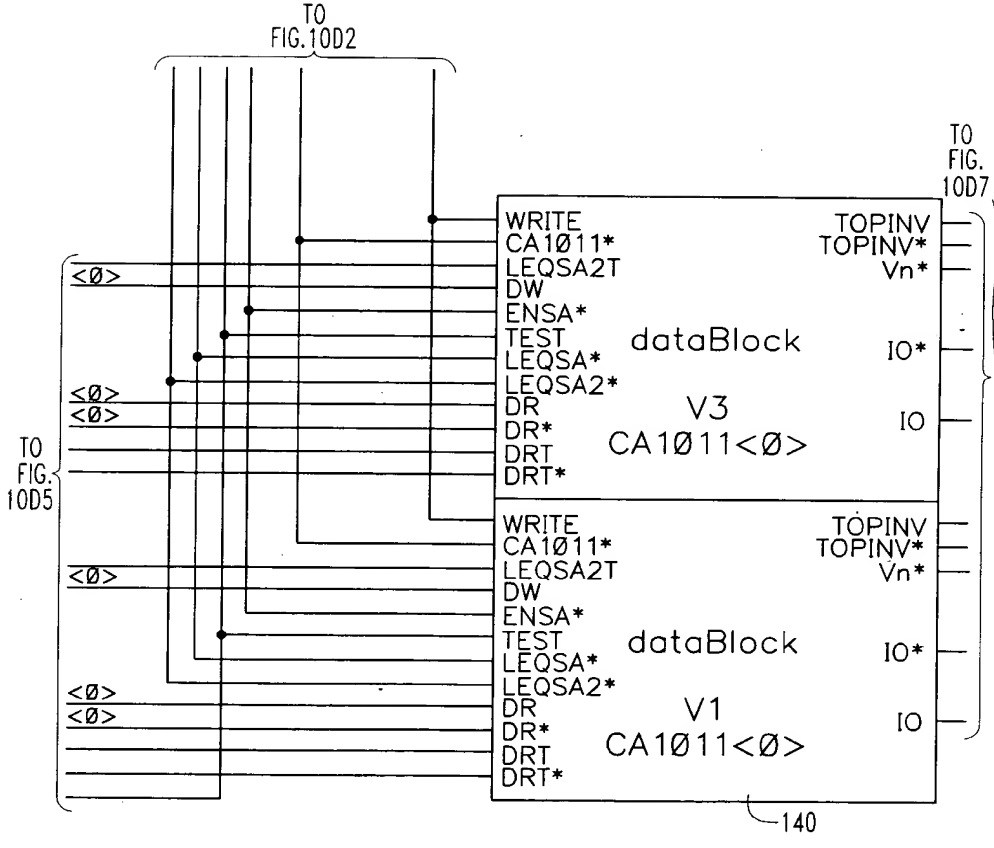

TO
FIG.10D2
TO
FIG.
10D7
TO
FIG.
10D5
WRITE
CA1Ø11*
LEQSA2T
DW
ENSA*
TEST
LEQSA*
LEQSA2*
DR
DR*
DRT
DRT*
dataBlock
V3
CA1Ø11<Ø>
TOPINV
TOPINV*
Vn*
IO*
IO
<Ø>
dataBlock
V1
CA1Ø11<Ø>
140

FIG. 10D6

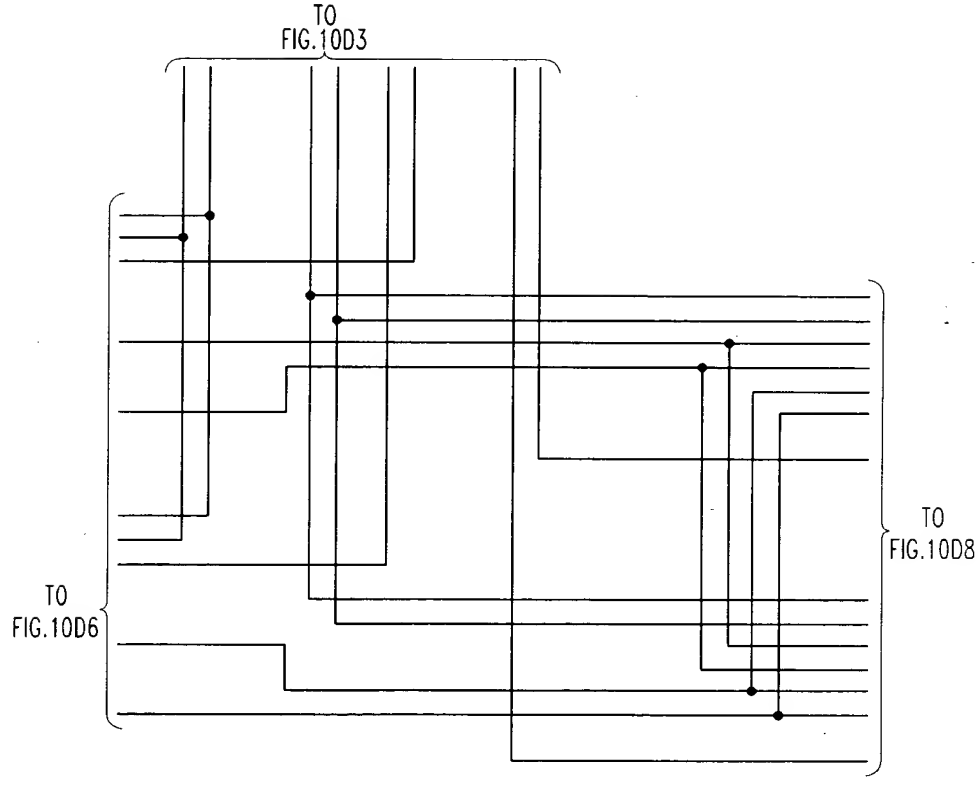


FIG. 10D7

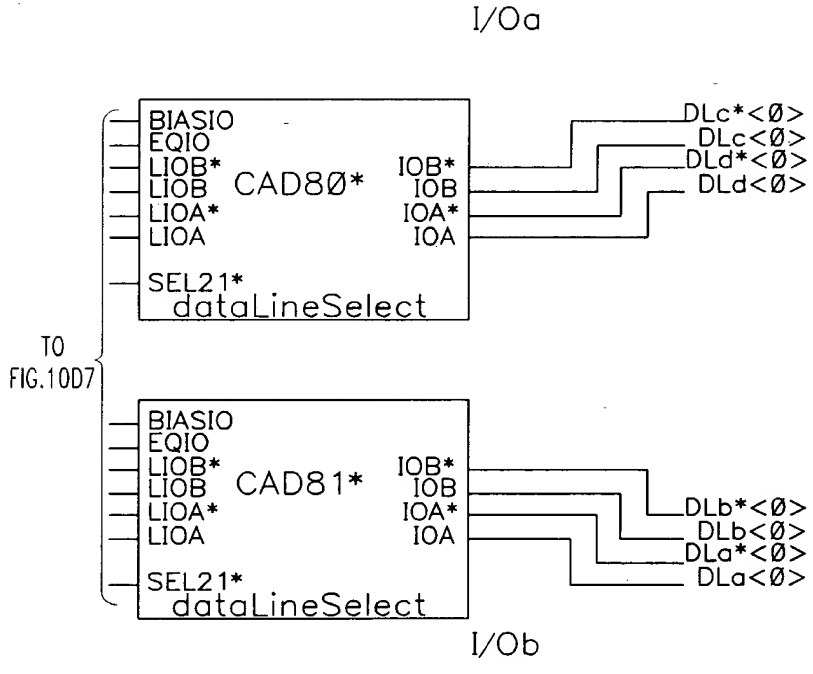

I/Oa
BIASIO
EQIO
LIOB*
LIOB
LIOA*
LIOA
CAD80*
IOB*
IOB
IOA*
IOA
SEL21*
dataLineSelect
DLc*<0>
DLc<0>
DLd*<0>
DLd<0>
TO
FIG.10D7
BIASIO
EQIO
LIOB*
LIOB
LIOA*
LIOA
CAD81*
IOB*
IOB
IOA*
IOA
SEL21*
dataLineSelect
DLb*<0>
DLb<0>
DLa*<0>
DLa<0>
I/Ob

FIG. 10D8

FIG. 11-1

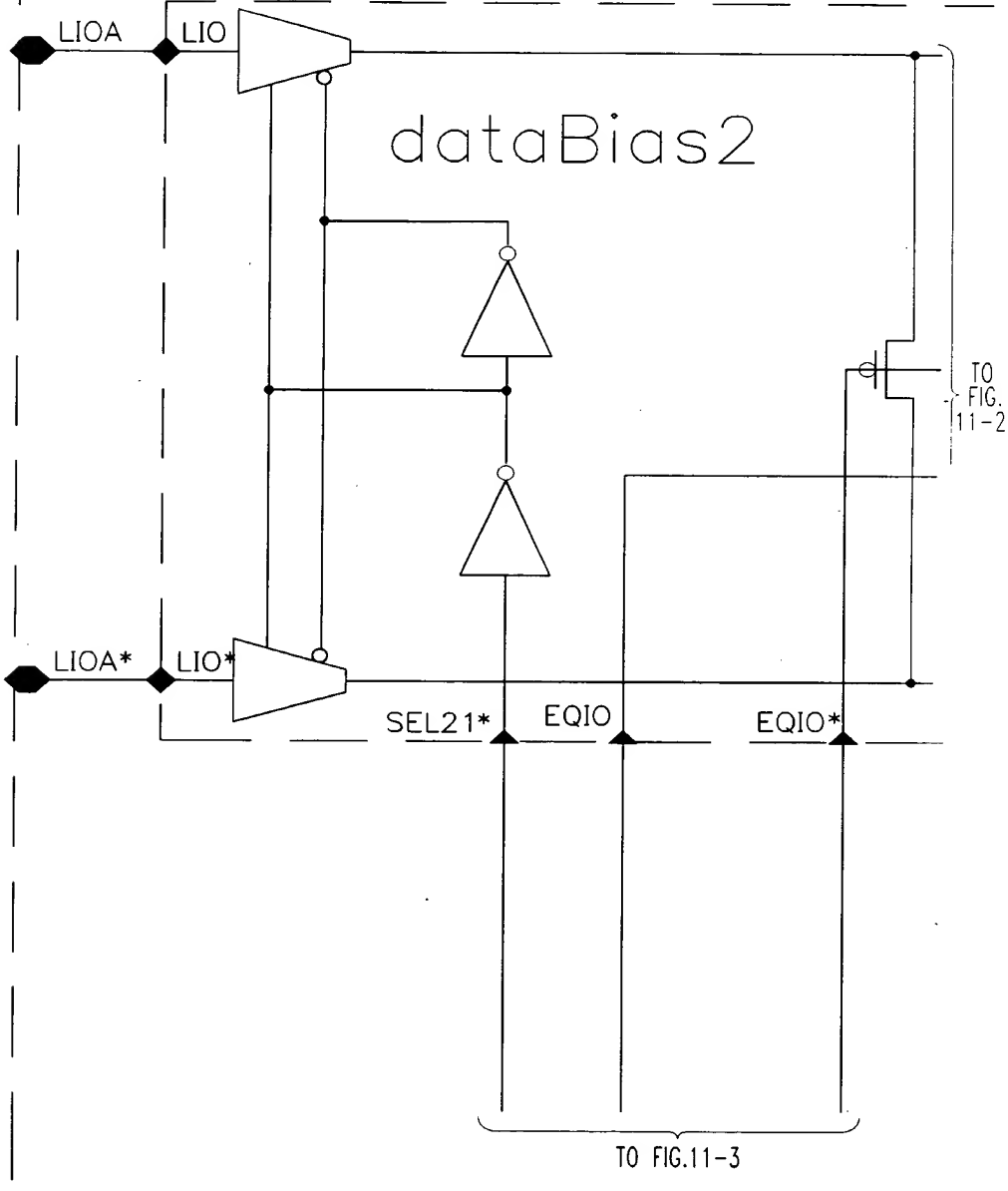
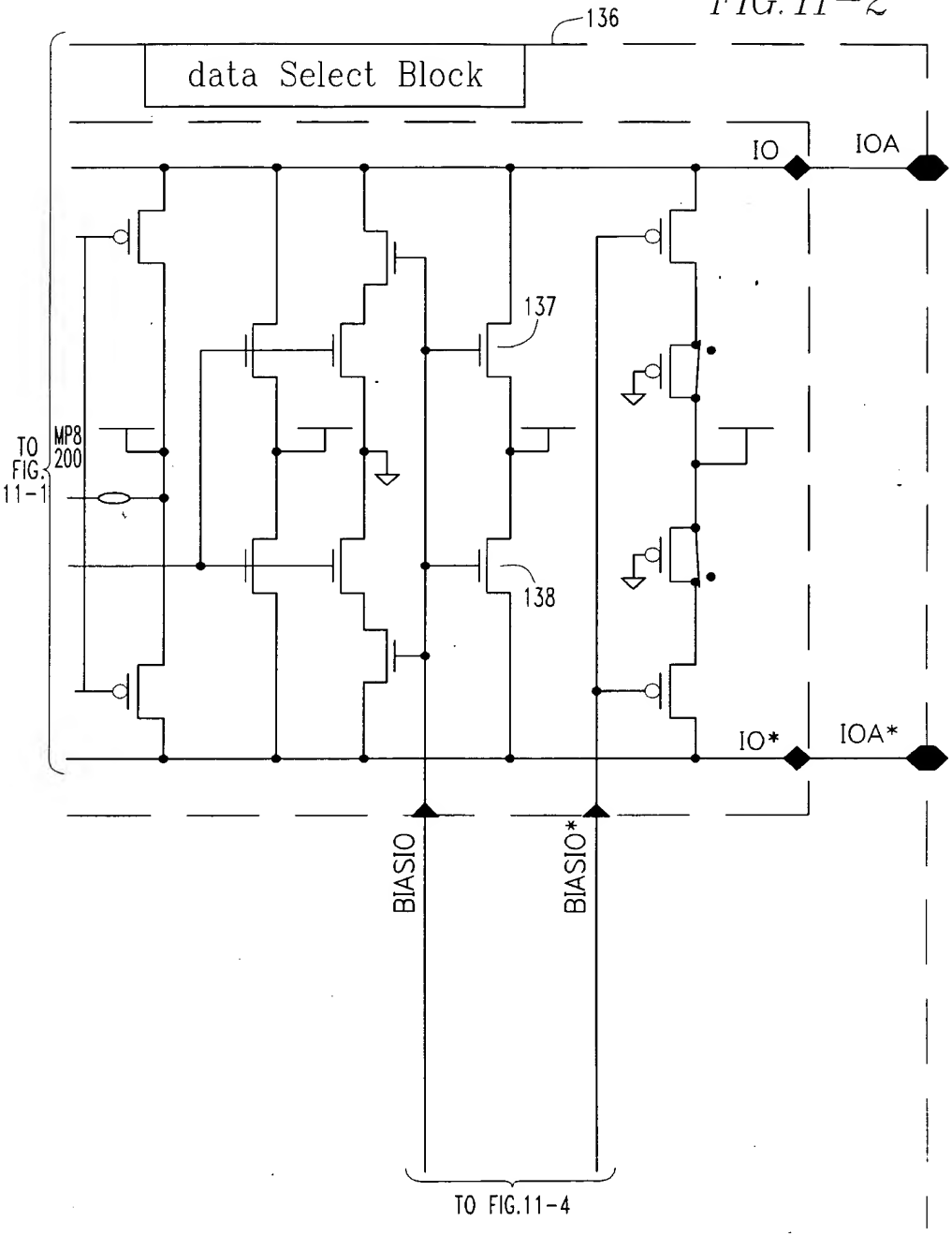

136
LIOA
LIO
dataBias2
TO FIG. 11-2
LIOA*
LIO*
SEL21*
EQIO
EQIO*
TO FIG.11-3

FIG. 11-2


136
data Select Block
IO
IOA
137
TO FIG. 11-1
MP8 200
138
IO*
IOA*
BIASIO
BIASIO*
TO FIG.11-4

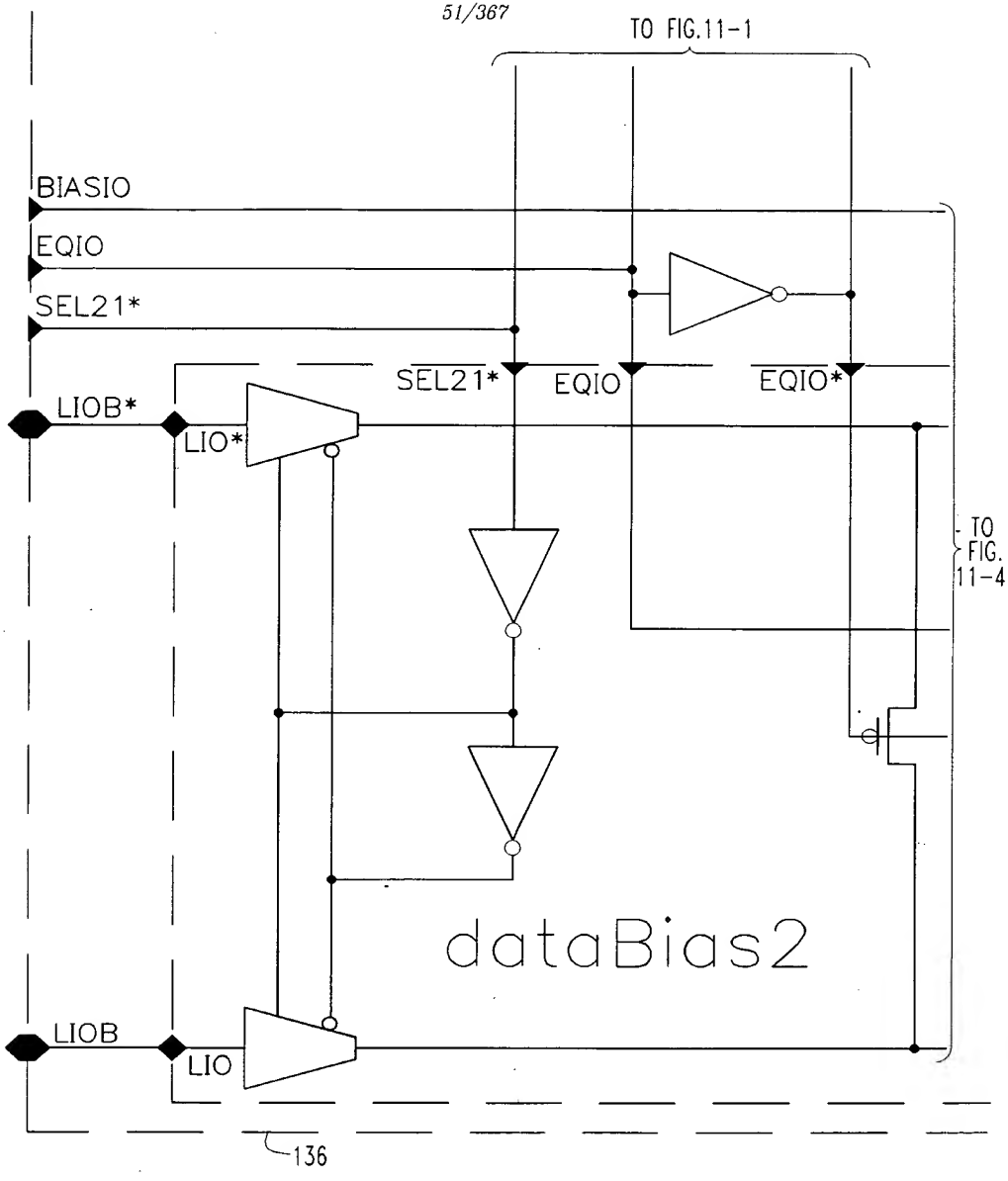

TO FIG.11-1
BIASIO
EQIO
SEL21*
SEL21*
EQIO
EQIO*
LIOB*
LIO*
TO FIG. 11-4
dataBias2
LIOB
LIO
136

FIG. 11-3

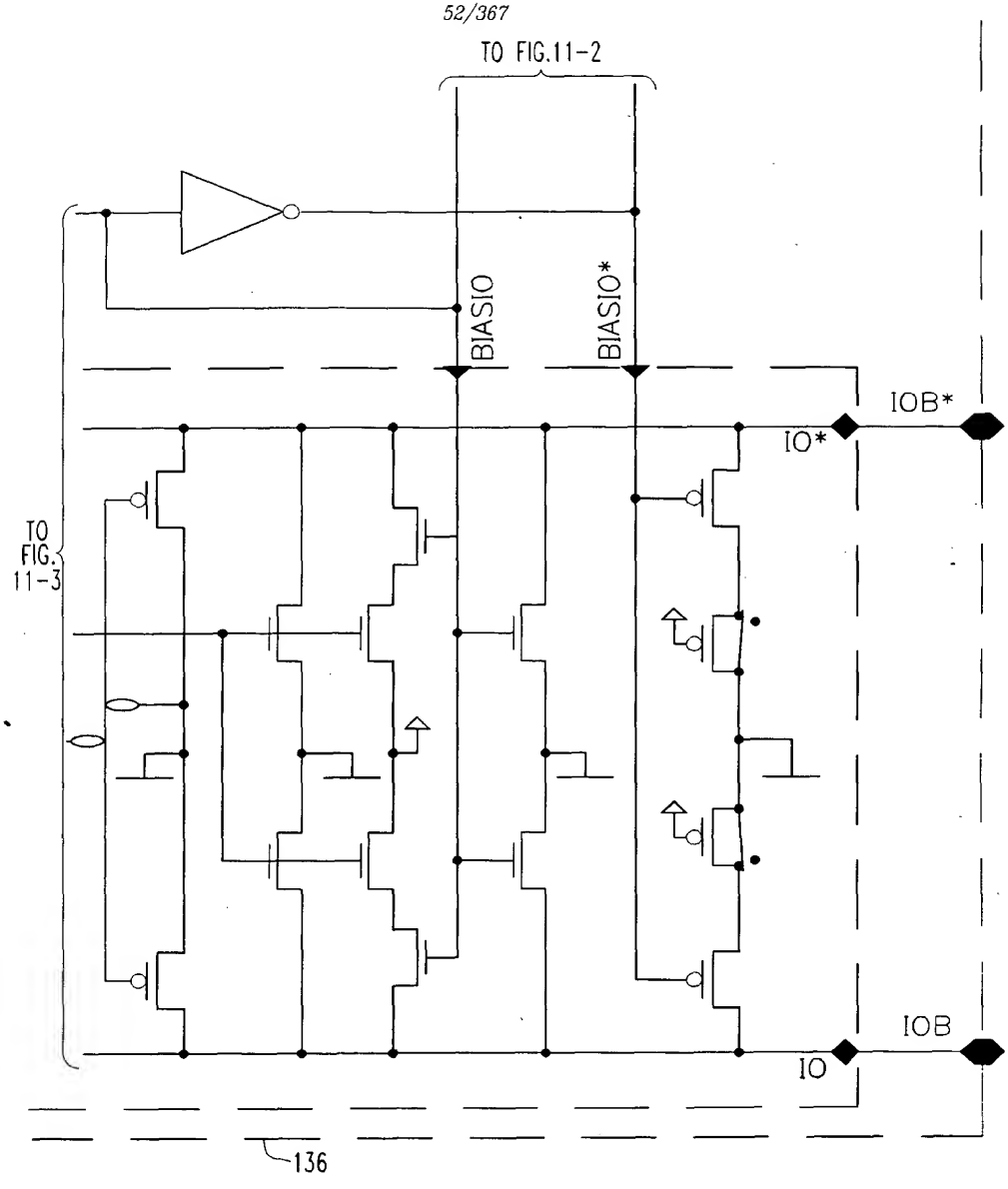


FIG. 11-4

TOSHIBA 0270860

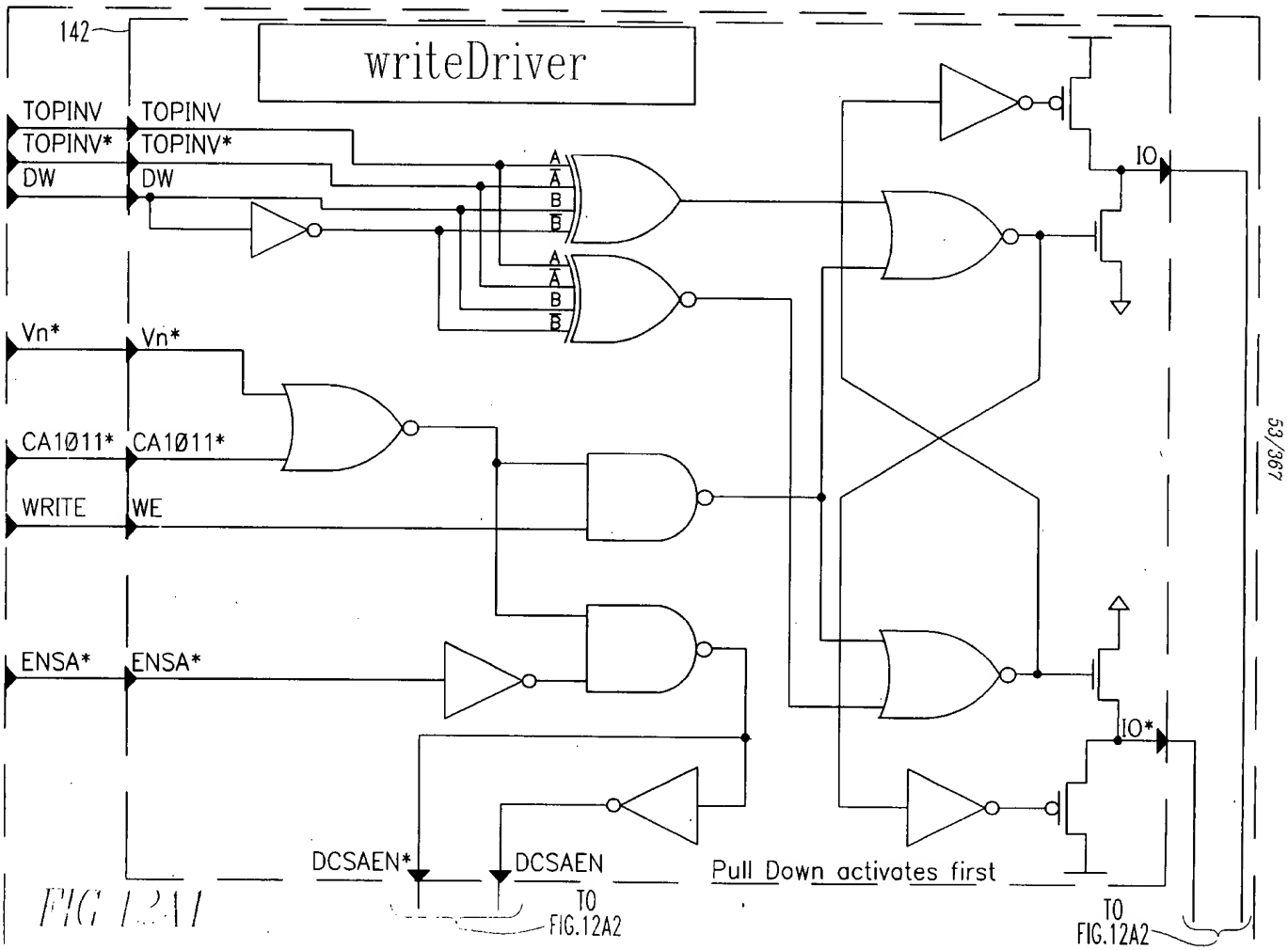


FIG 12A1

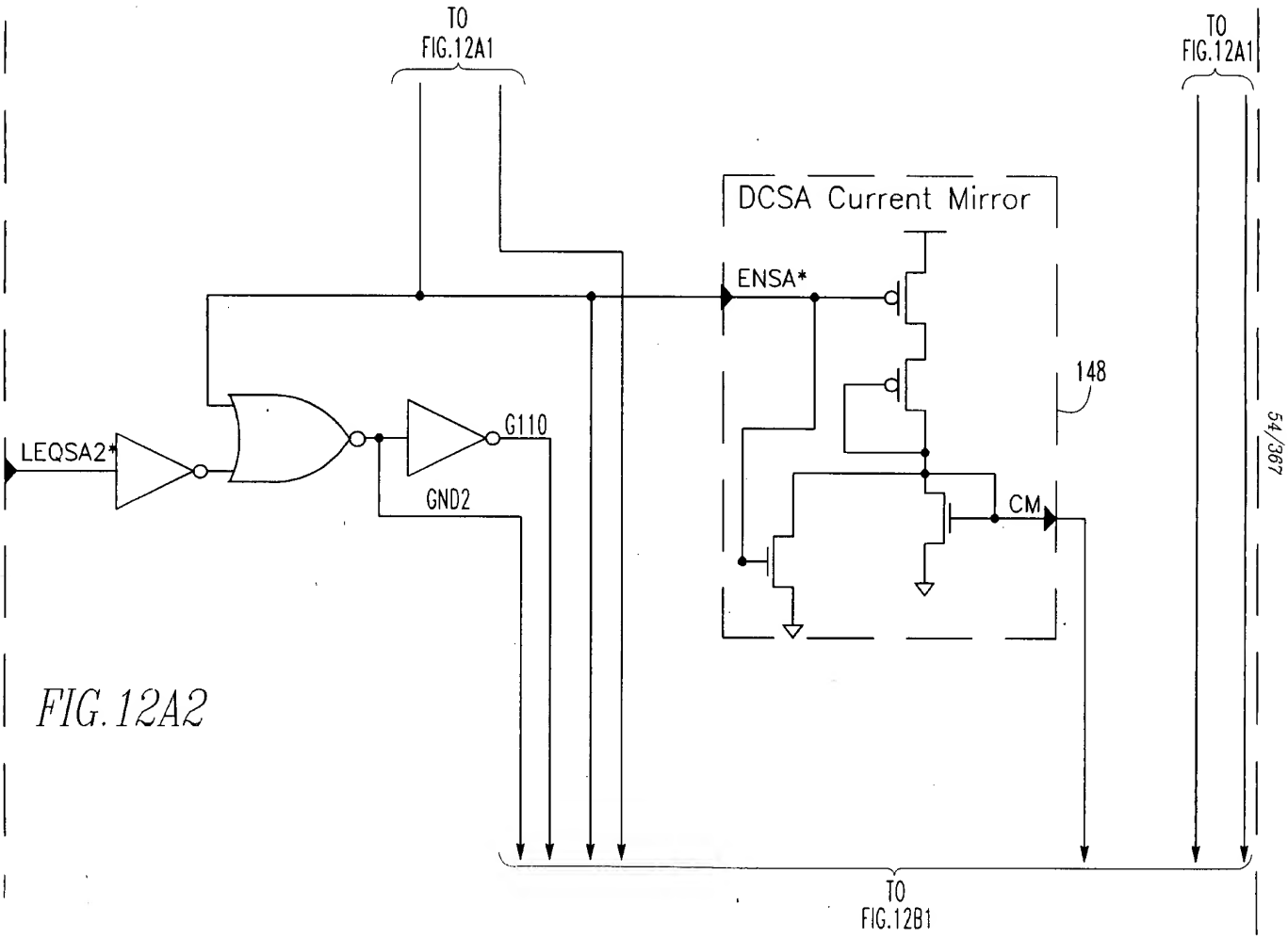
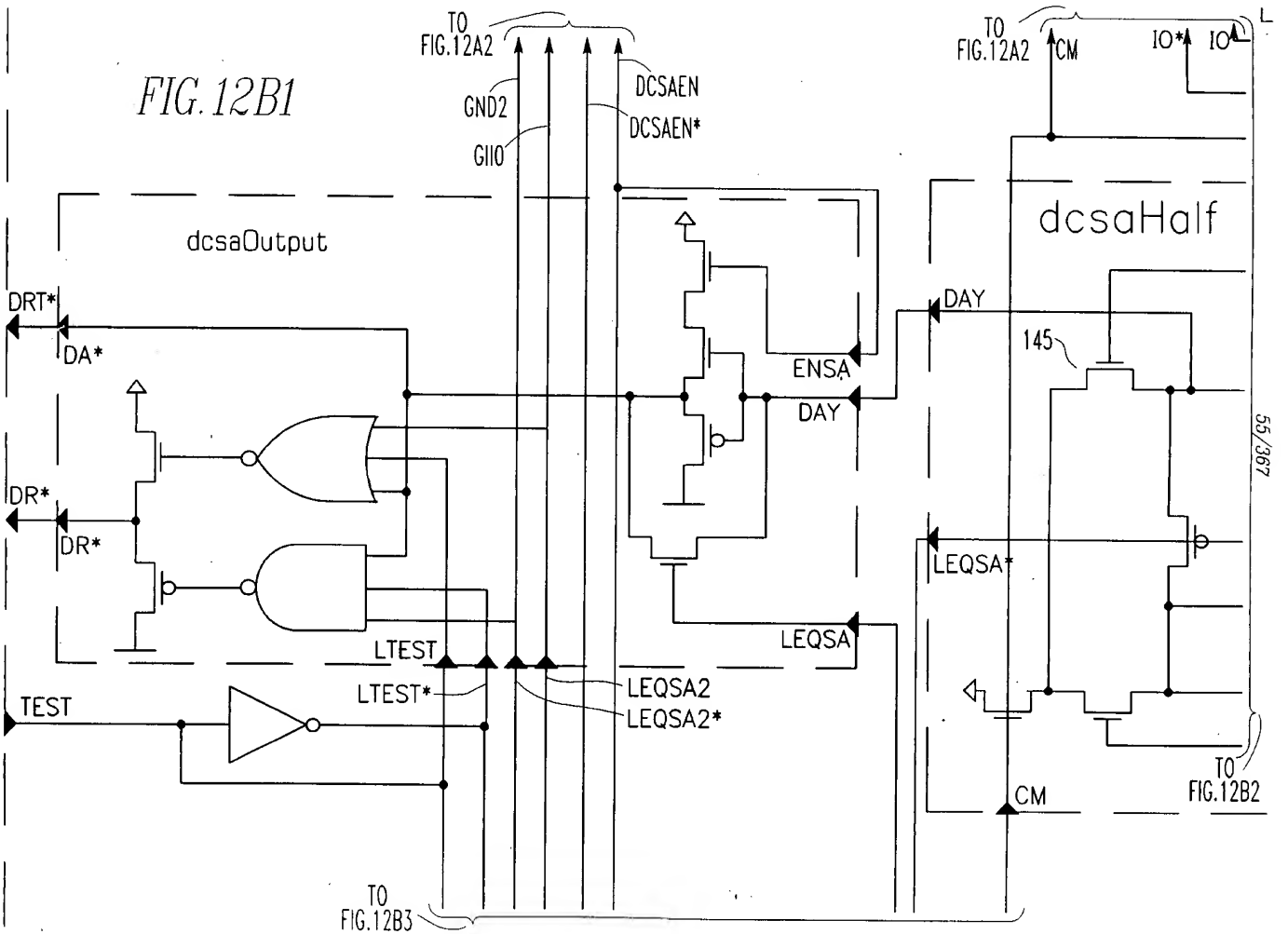

TO
FIG.12A1
TO
FIG.12A1
DCSA Current Mirror
ENSA*
148
LEQSA2*
G110
GND2
CM
TO
FIG.12B1

FIG. 12A2

FIG. 12B1


TO FIG.12A2
GND2
GII0
DCSAEN
DCSAEN*
dcsaOutput
DRT*
DA*
DR*
DR*
TEST
LTEST
LTEST*
LEQSA2
LEQSA2*
ENSA
DAY
LEQSA
TO FIG.12B3
TO FIG.12A2
CM
IO*
IO
dcsaHalf
DAY
145
LEQSA*
CM
TO FIG.12B2
L

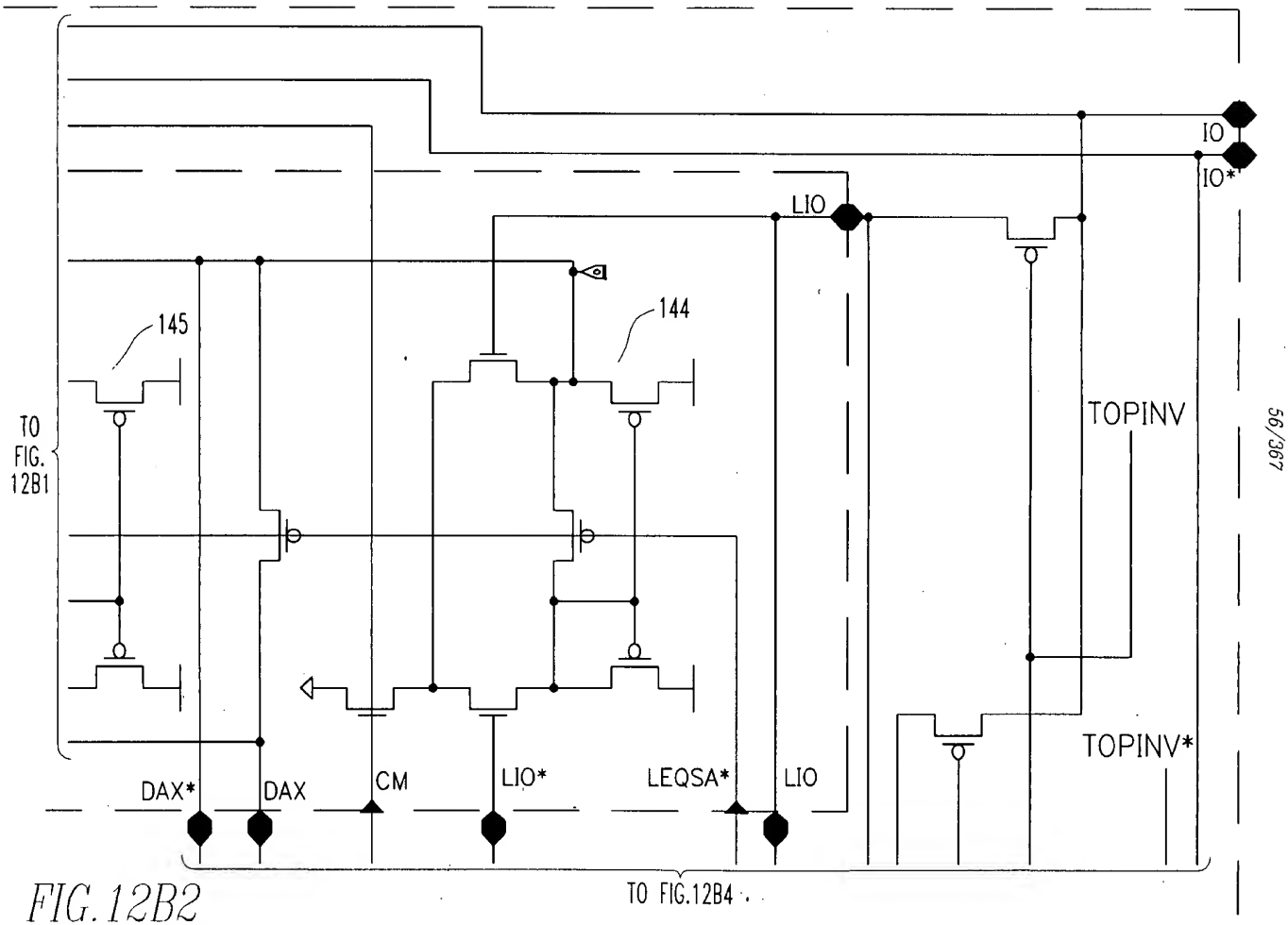

IO
IO*
LIO
145
144
TO
FIG.
12B1
TOPINV
TOPINV*
DAX*
DAX
CM
LIO*
LEQSA*
LIO
TO FIG.12B4

FIG. 12B2

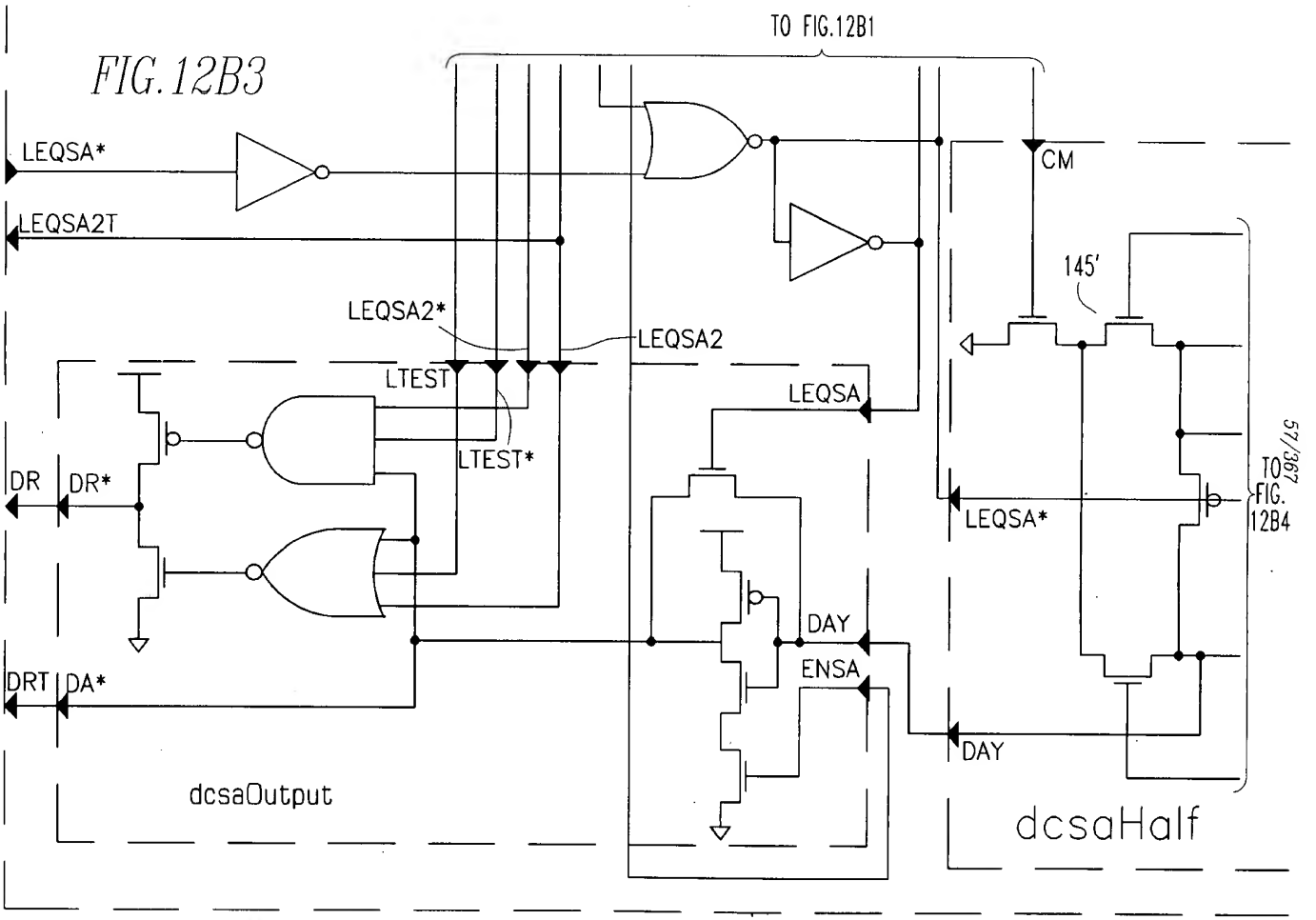

TO FIG.12B1
LEQSA*
LEQSA2T
LEQSA2*
LEQSA2
LTEST
LTEST*
LEQSA
CM
145'
DR
DR*
DRT
DA*
DAY
ENSA
LEQSA*
TO FIG. 12B4
dcsaOutput
dcsaHalf

FIG.12B3

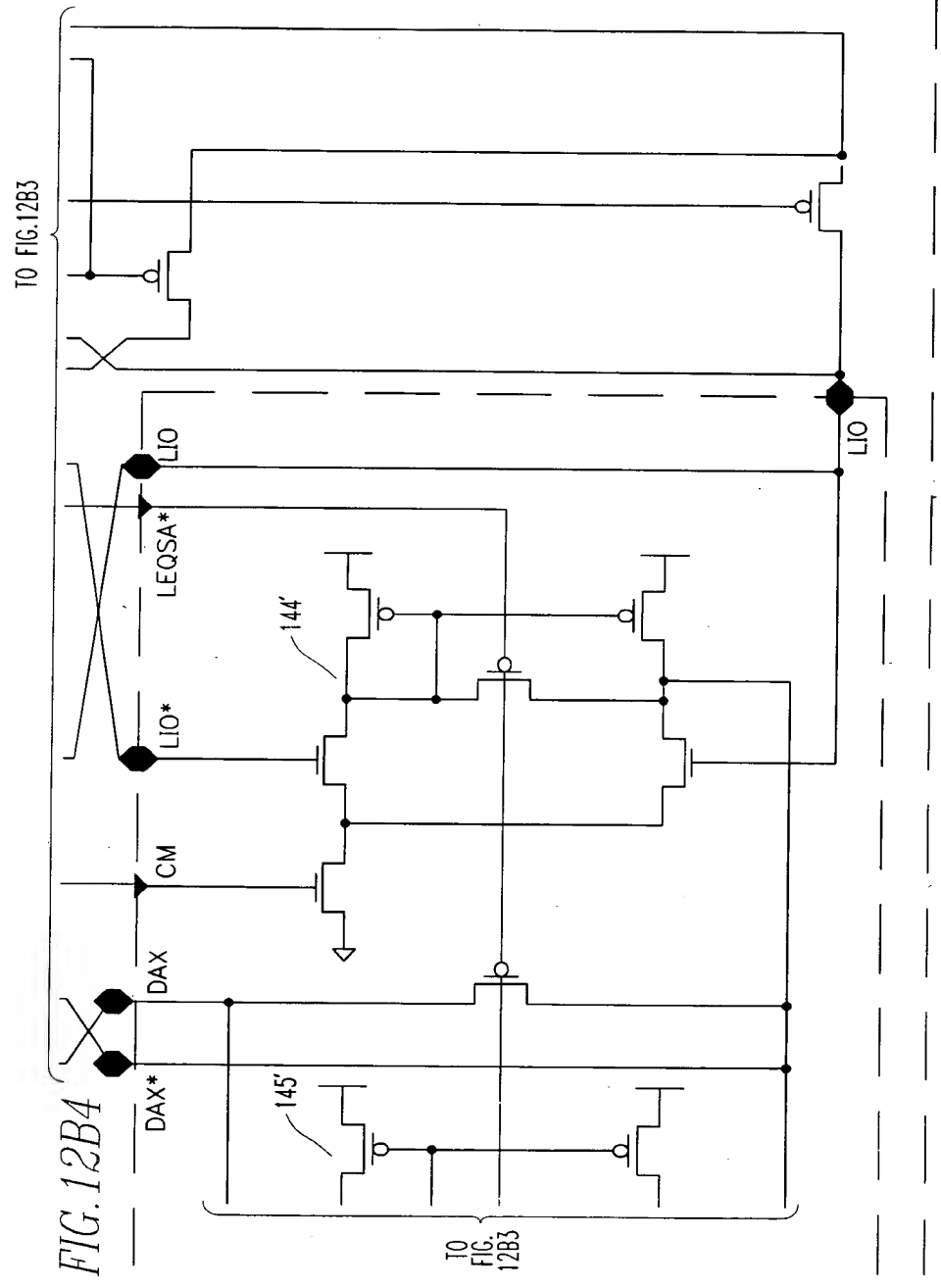


FIG. 12B4

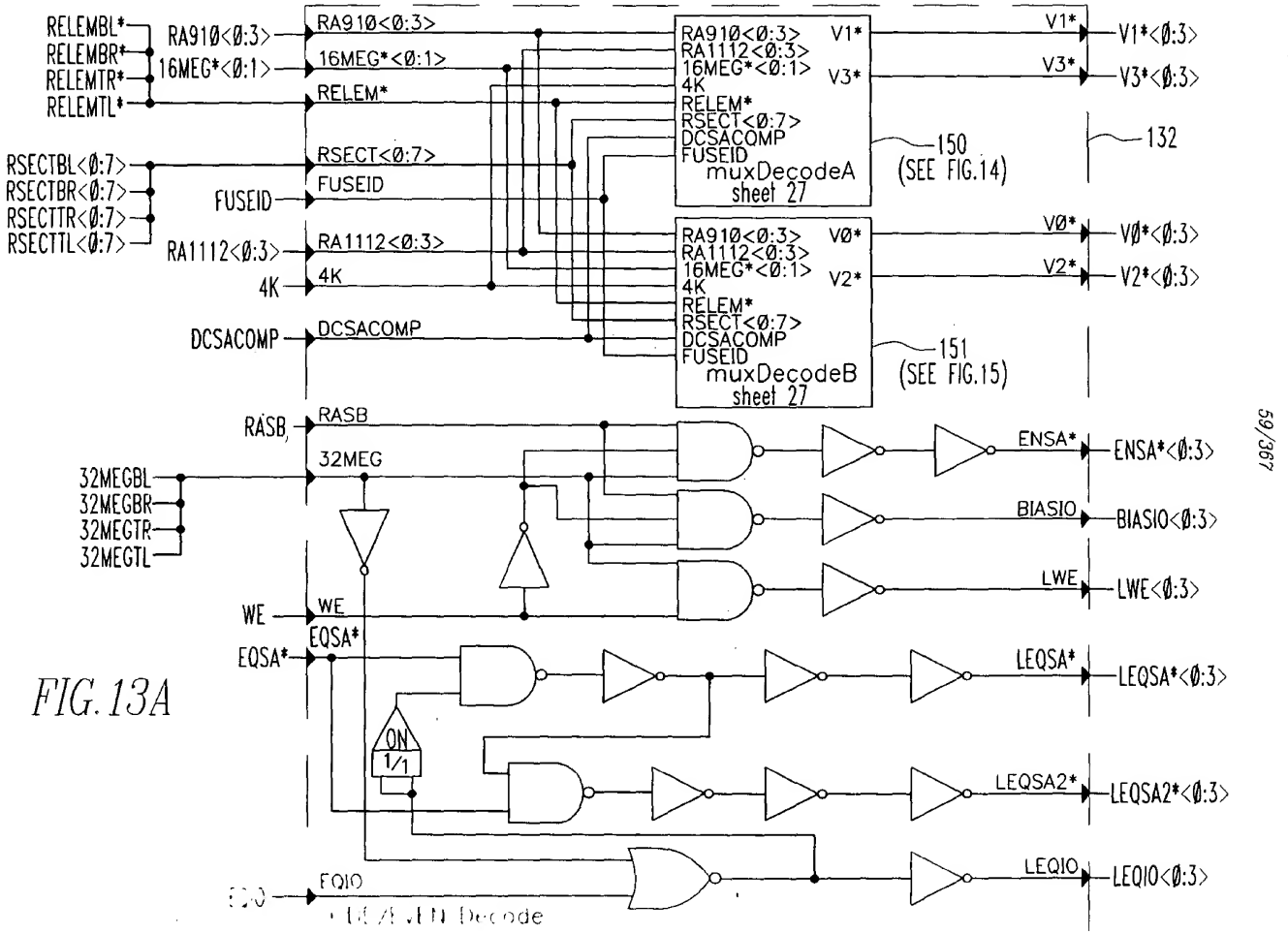

RELEMBL*
RELEMBR*
RELEMTR*
RELEMTL*
RA910<Ø:3>
16MEG*<Ø:1>
RELEM*
RSECTBL<Ø:7>
RSECTBR<Ø:7>
RSECTTR<Ø:7>
RSECTTL<Ø:7>
RSECT<Ø:7>
FUSEID
RA1112<Ø:3>
4K
DCSACOMP
RA910<Ø:3>
RA1112<Ø:3>
16MEG*<Ø:1>
4K
RELEM*
RSECT<Ø:7>
DCSACOMP
FUSEID
muxDecodeA
sheet 27
V1*
V3*
150
(SEE FIG.14)
132
muxDecodeB
sheet 27
VØ*
V2*
151
(SEE FIG.15)
RASB
32MEG
32MEGBL
32MEGBR
32MEGTR
32MEGTL
WE
EQSA*
ON
1/1
FQIO
ENSA*
BIASIO
LWE
LEQSA*
LEQSA2*
LEQIO
V1*<Ø:3>
V3*<Ø:3>
VØ*<Ø:3>
V2*<Ø:3>
ENSA*<Ø:3>
BIASIO<Ø:3>
LWE<Ø:3>
LEQSA*<Ø:3>
LEQSA2*<Ø:3>
LEQIO<Ø:3>

FIG. 13A

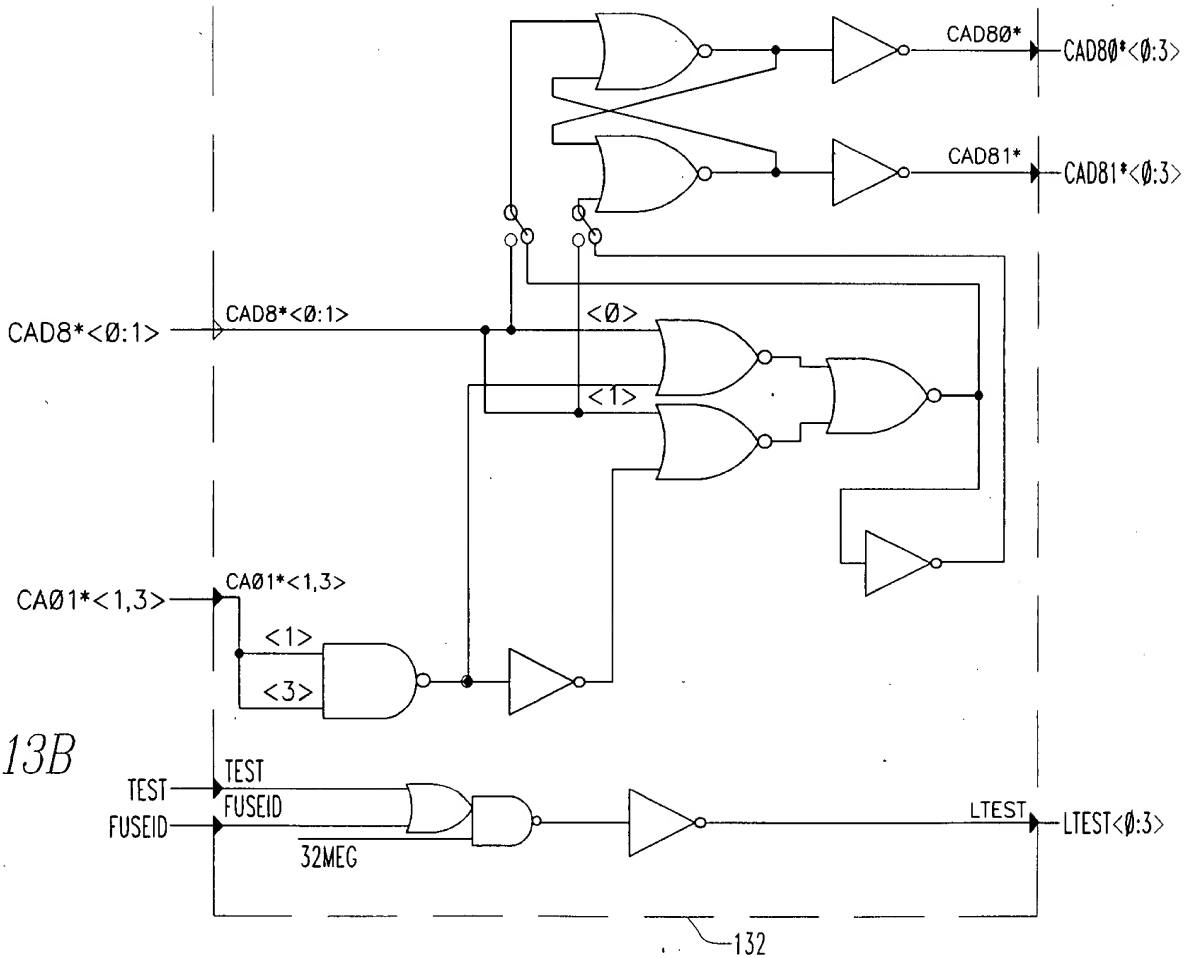

CAD8Ø*
CAD8Ø*<Ø:3>
CAD81*
CAD81*<Ø:3>
CAD8*<Ø:1>
CAD8*<Ø:1>
<Ø>
<1>
CAØ1*<1,3>
CAØ1*<1,3>
<1>
<3>
TEST
TEST
FUSEID
FUSEID
32MEG
LTEST
LTEST<Ø:3>
132

FIG. 13B

FOSDEC' 62970860

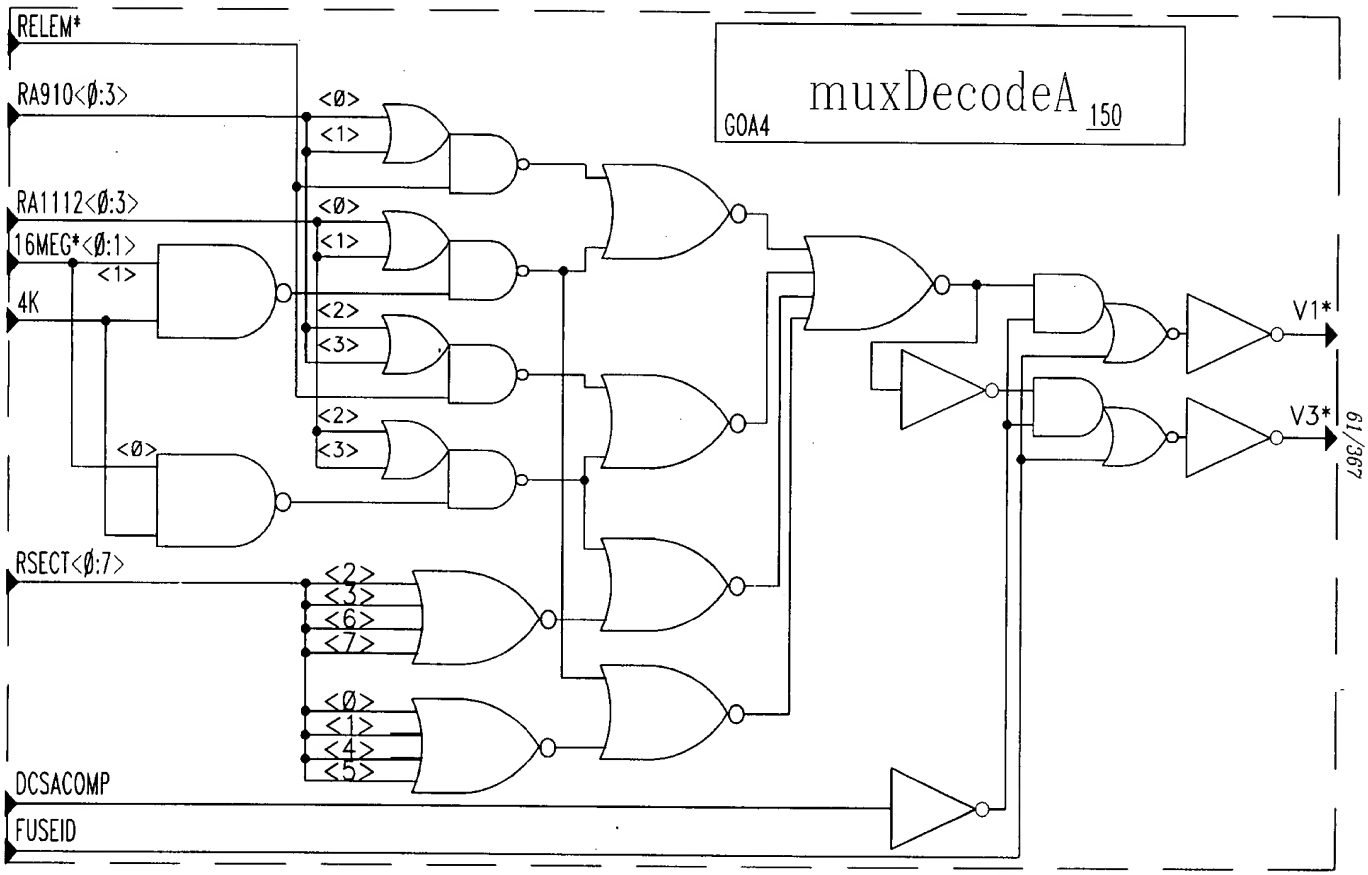
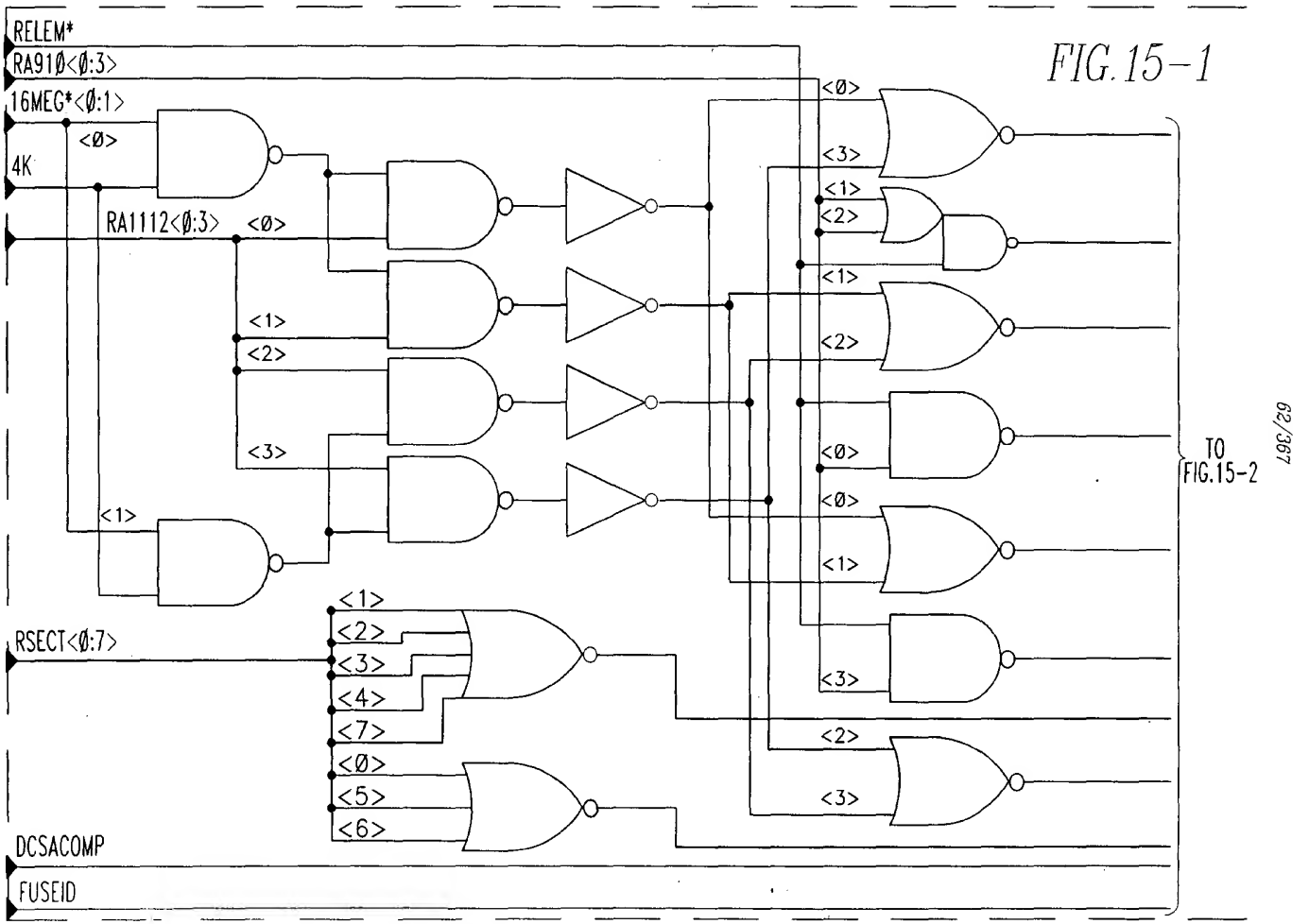


FIG. 14

FIG. 15-1


RELEM*
RA91Ø<Ø:3>
16MEG*<Ø:1>
4K
<Ø>
RA1112<Ø:3>
<Ø>
<1>
<2>
<3>
<1>
RSECT<Ø:7>
<1>
<2>
<3>
<4>
<7>
<Ø>
<5>
<6>
DCSACOMP
FUSEID
<Ø>
<3>
<1>
<2>
<1>
<2>
<Ø>
<Ø>
<1>
<3>
<2>
<3>
TO
FIG.15-2

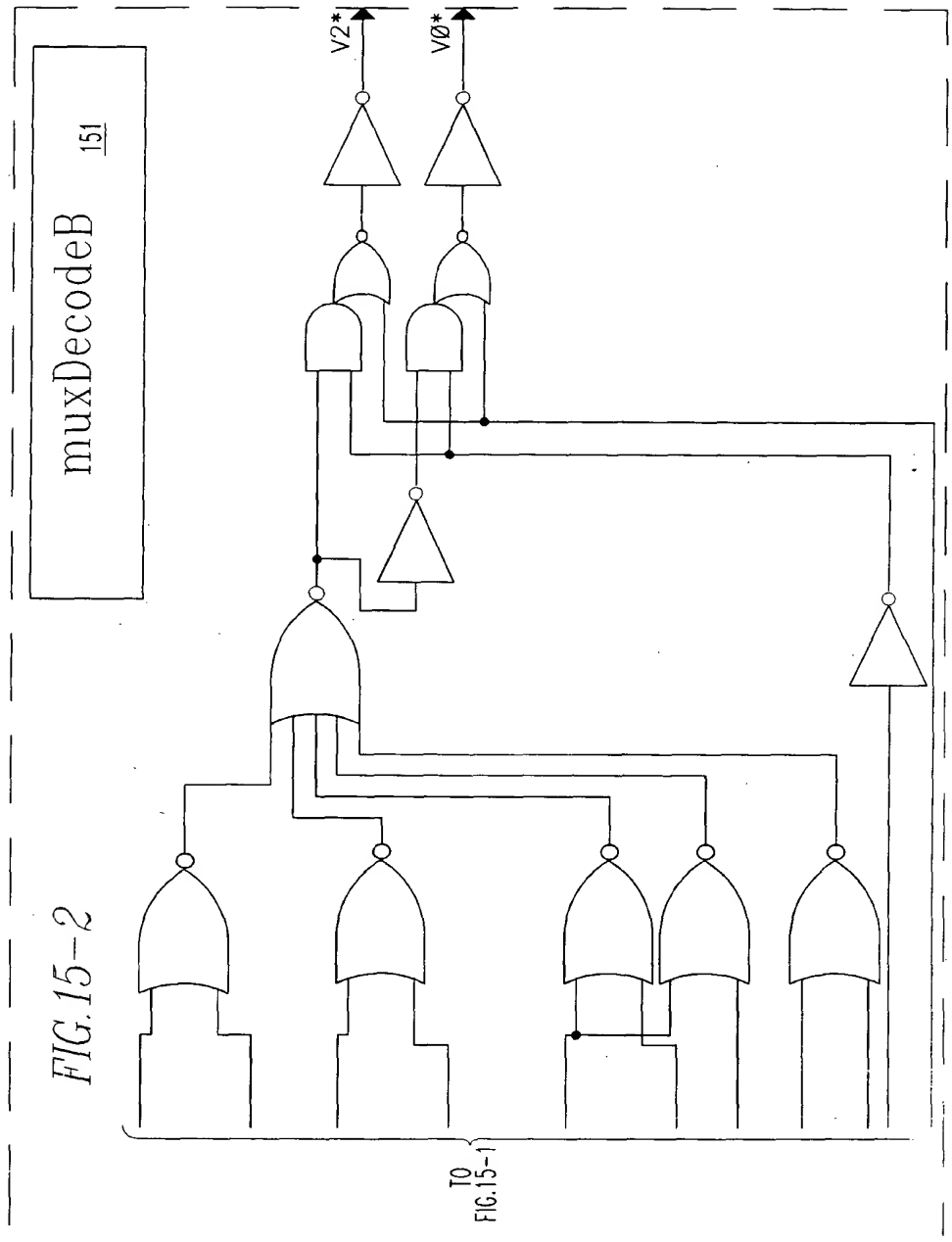
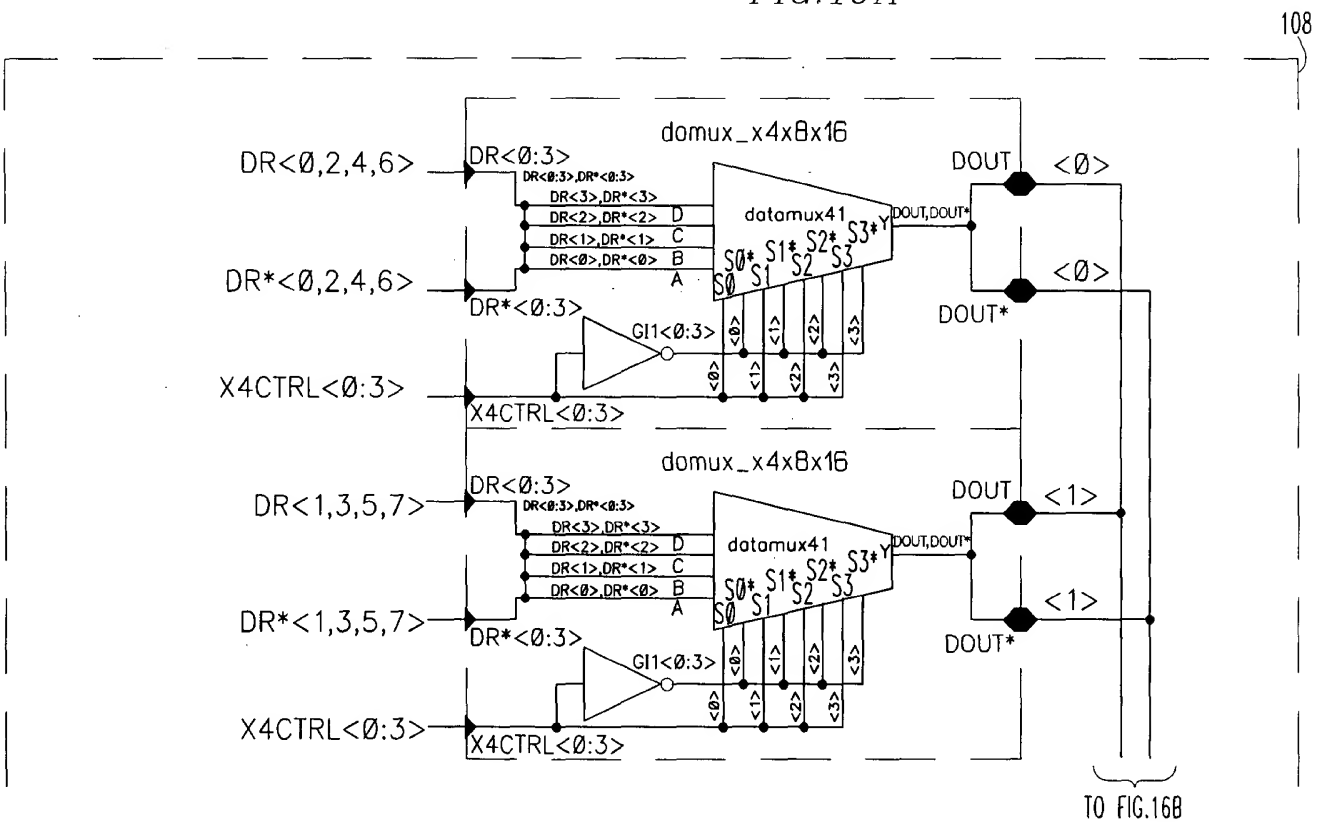


FIG.15-2

FIG. 16A


108
domux_x4x8x16
DR<0,2,4,6>
DR<0:3>
DR<0:3>,DR*<0:3>
DR<3>,DR*<3>
DR<2>,DR*<2>
DR<1>,DR*<1>
DR<0>,DR*<0>
D
C
B
A
datamux41
S0* S1* S2* S3*
S0 S1 S2 S3
Y
DOUT,DOUT*
DOUT
<0>
DOUT*
DR*<0,2,4,6>
DR*<0:3>
GI1<0:3>
X4CTRL<0:3>
domux_x4x8x16
DR<1,3,5,7>
DR*<1,3,5,7>
<1>
TO FIG.16B
64/367

Read Data			
LDQ<n>	X16	X8	X4
Ø	Ø	Ø,2	Ø,2,4,6
1	1	1,3	1,3,5,7
2	2		
3	3		
4	4		
5	5		
6	6	4,6	
7	7	5,7	

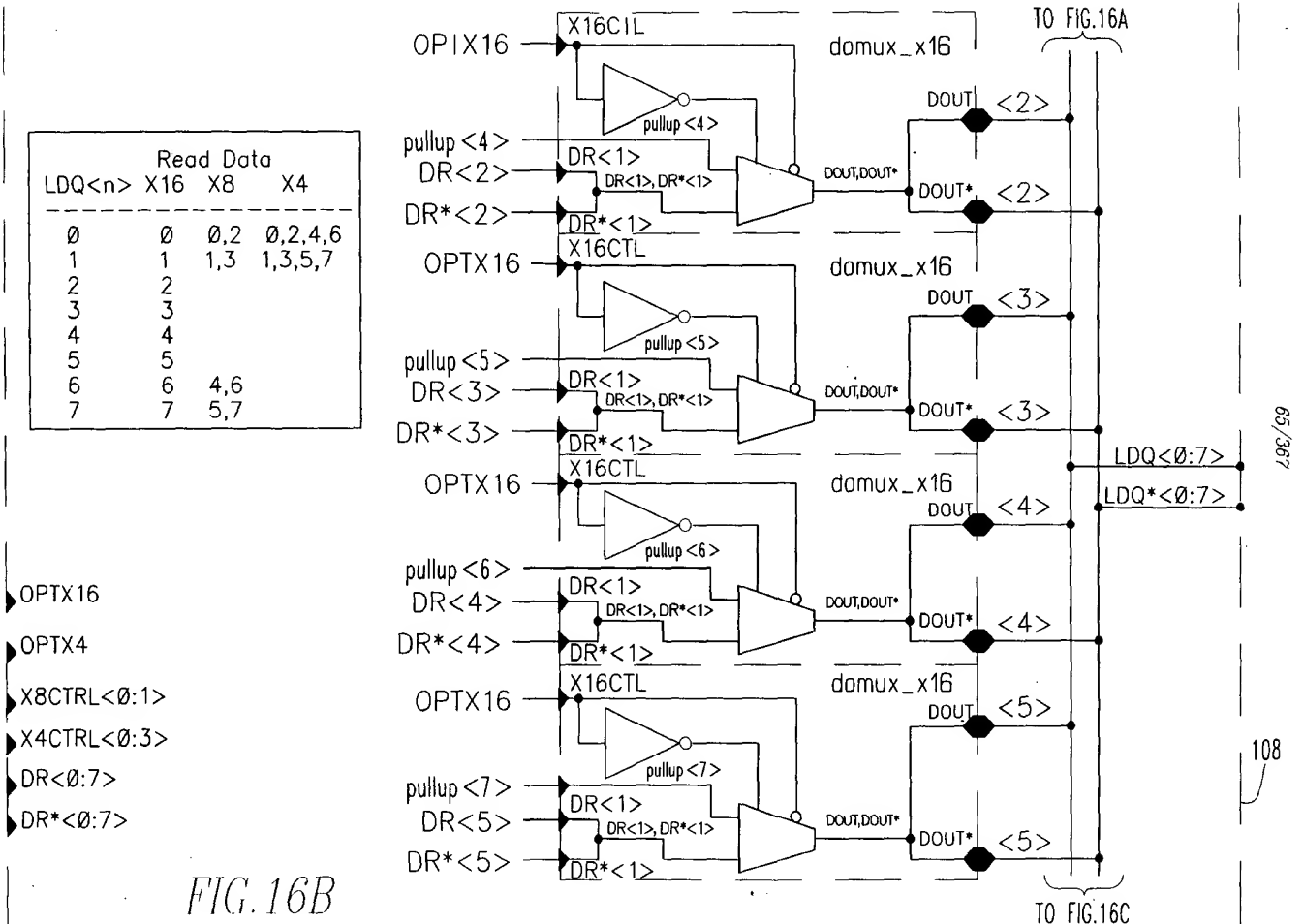


FIG.16B

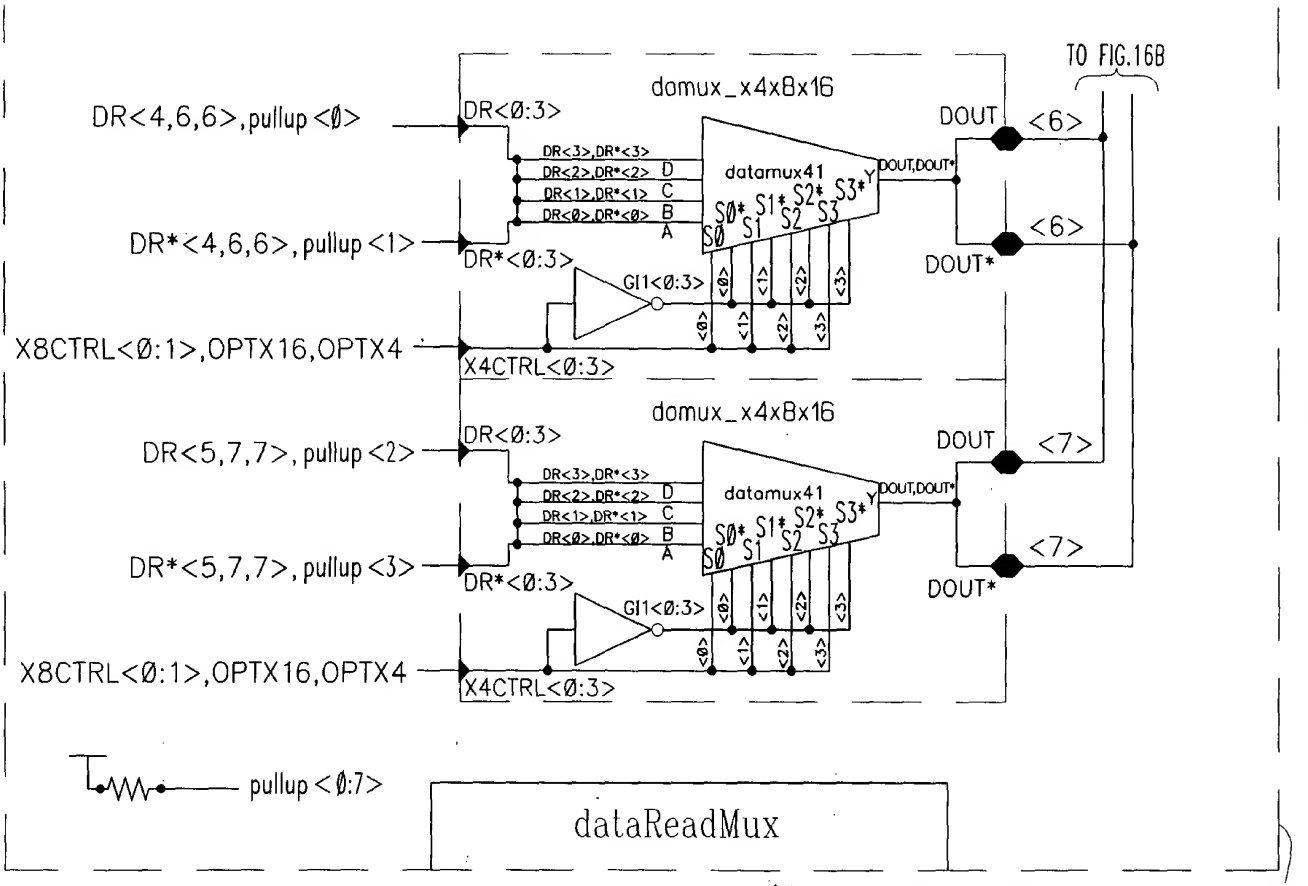

TO FIG.16B
domux_x4x8x16
DR<4,6,6>,pullup <Ø>
DR<Ø:3>
DR<3>,DR*<3>
DR<2>,DR*<2>
DR<1>,DR*<1>
DR<Ø>,DR*<Ø>
D
C
B
A
datamux41
DOUT,DOUT*
DOUT
<6>
DR*<4,6,6>,pullup <1>
DR*<Ø:3>
GI1<Ø:3>
DOUT*
X8CTRL<Ø:1>,OPTX16,OPTX4
X4CTRL<Ø:3>
domux_x4x8x16
DR<5,7,7>, pullup <2>
<7>
DR*<5,7,7>, pullup <3>
pullup <Ø:7>
dataReadMux
108

FIG.16C

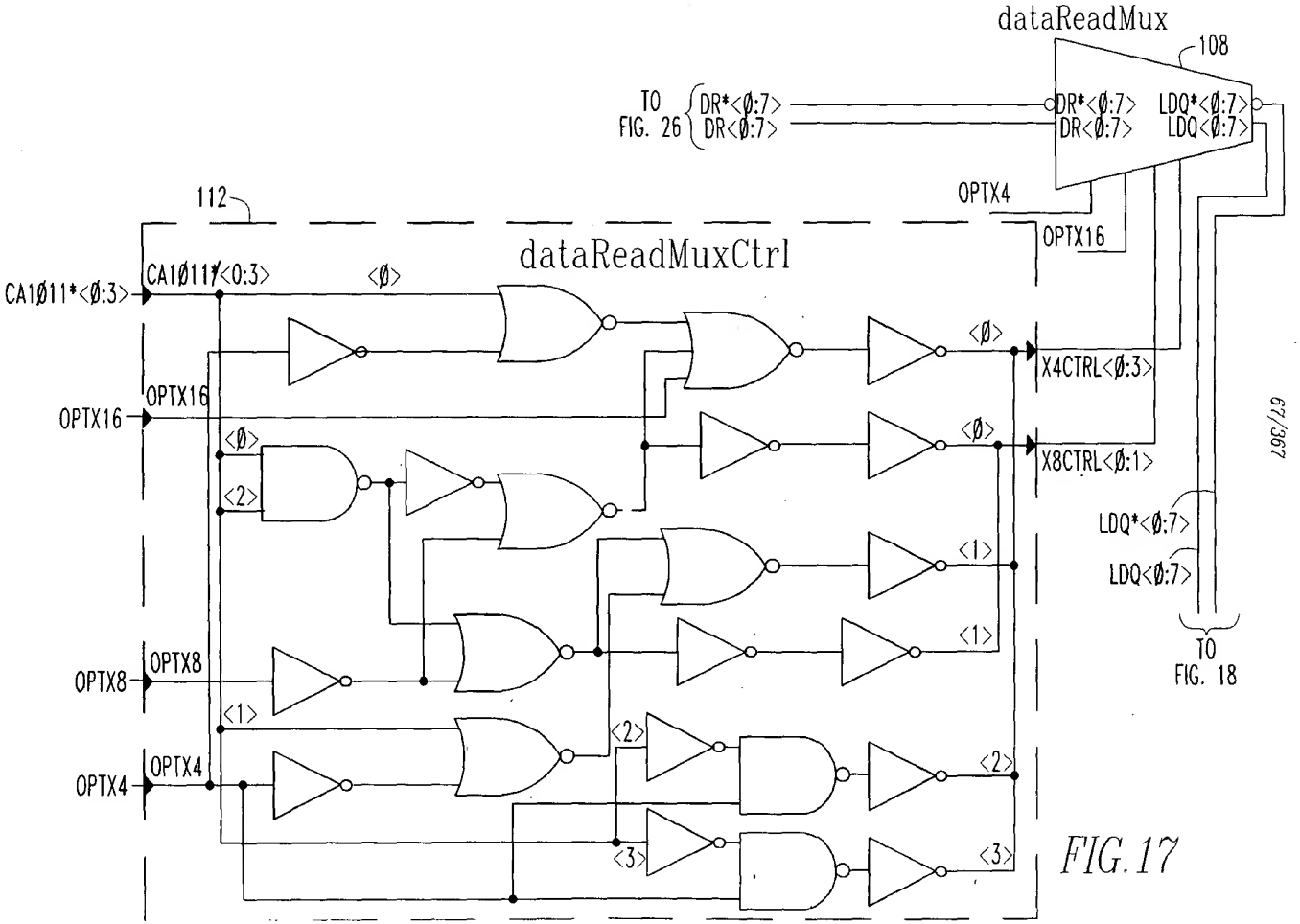

dataReadMux
108
TO FIG. 26
DR*<Ø:7>
DR<Ø:7>
DR*<Ø:7>
DR<Ø:7>
LDQ*<Ø:7>
LDQ<Ø:7>
112
dataReadMuxCtrl
OPTX4
OPTX16
CA1Ø11*<Ø:3>
CA1Ø11*<0:3>
<Ø>
X4CTRL<Ø:3>
X8CTRL<Ø:1>
<2>
<1>
OPTX8
<3>
LDQ*<Ø:7>
LDQ<Ø:7>
TO FIG. 18
67/367

FIG. 17

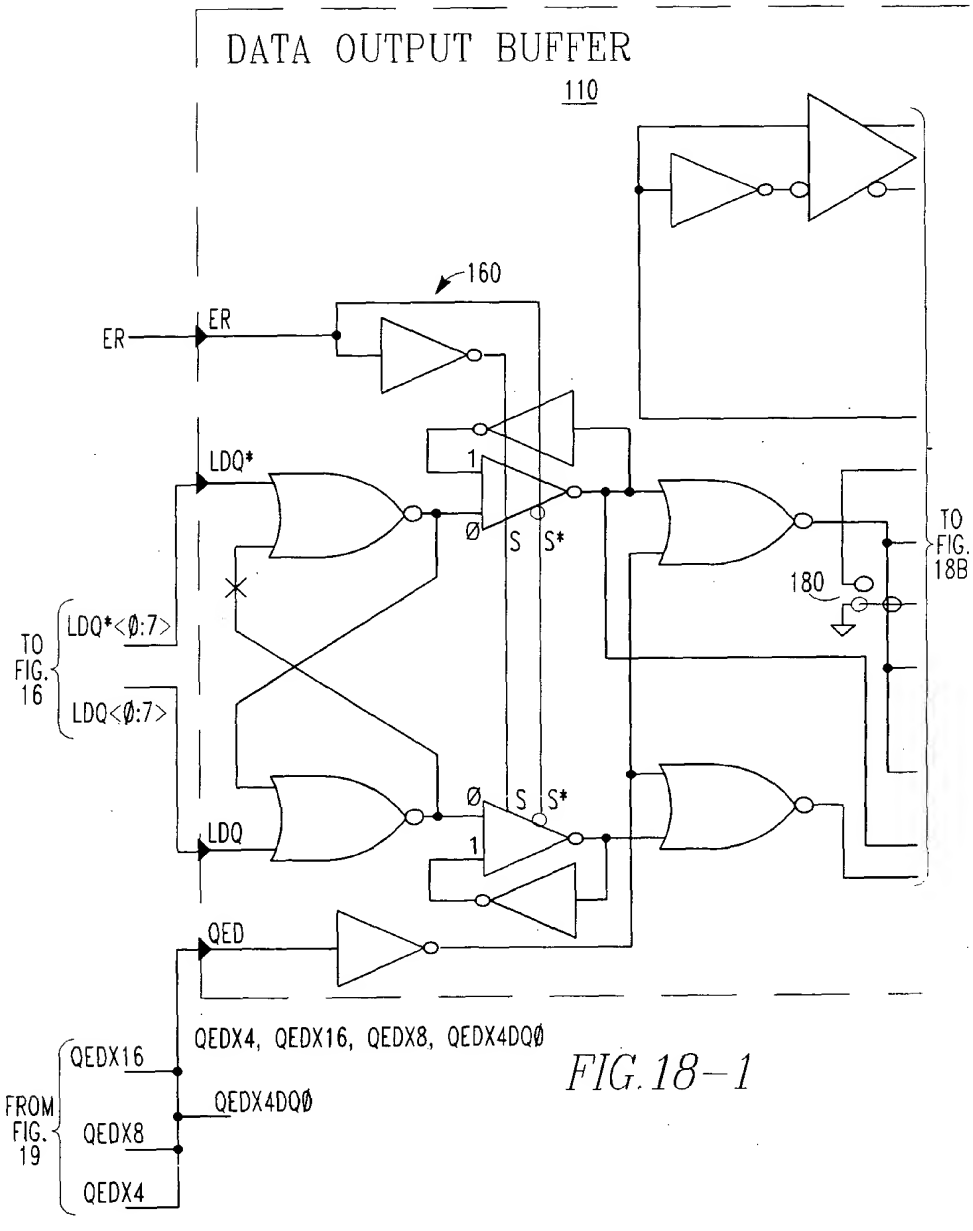

DATA OUTPUT BUFFER
110
160
ER
ER
LDQ*
1
Ø
S
S*
TO
FIG.
18B
180
TO
FIG.
16
LDQ*<Ø:7>
LDQ<Ø:7>
Ø
S
S*
LDQ
1
QED
QEDX4, QEDX16, QEDX8, QEDX4DQØ
FROM
FIG.
19
QEDX16
QEDX4DQØ
QEDX8
QEDX4

FIG. 18-1

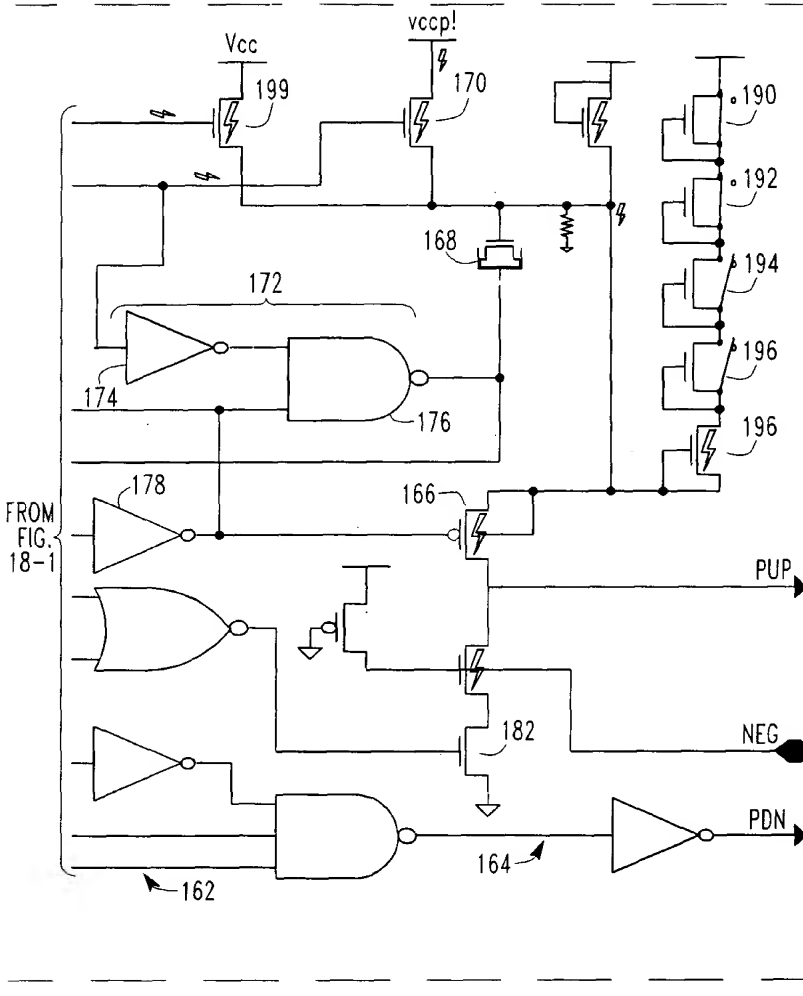

Vcc
vccp!
199
170
190
192
194
196
196
168
172
174
176
178
166
FROM
FIG.
18-1
PUP
167
182
NEG
181
PDN
183
164
162

FIG. 18-2

T0800 "8970860

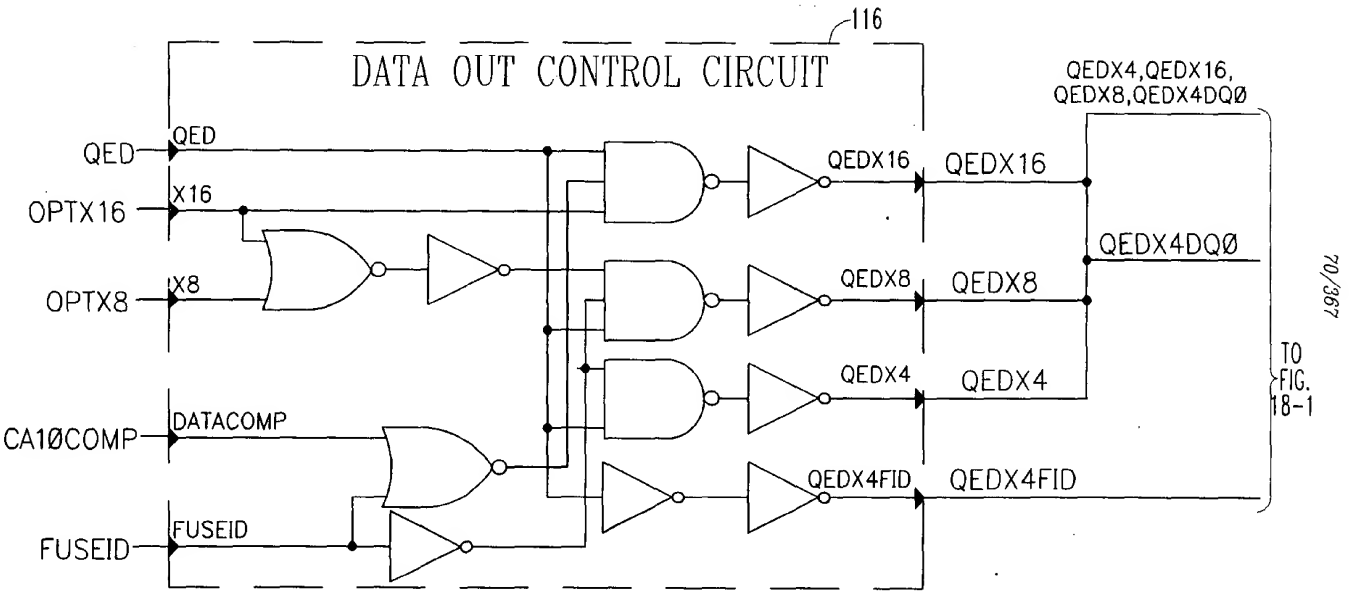


FIG. 19

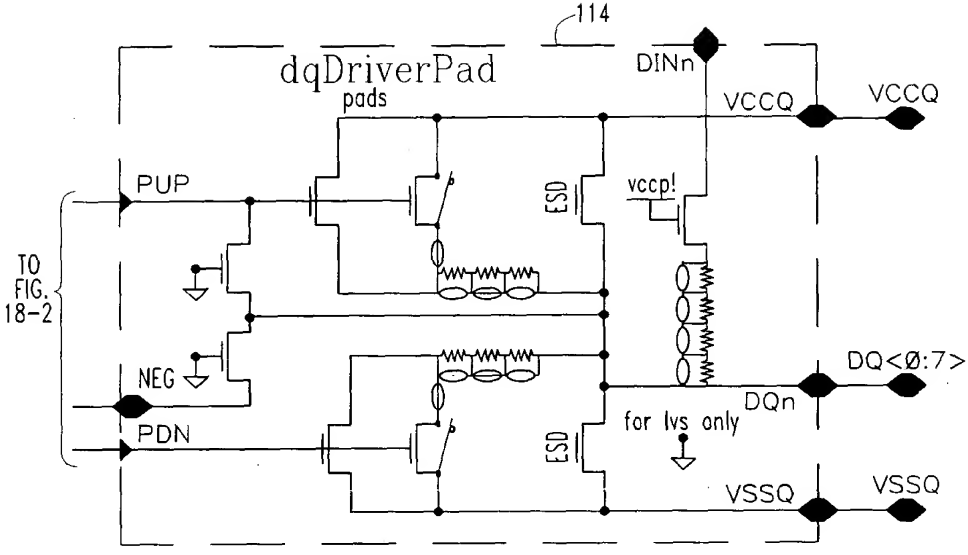

114
dqDriverPad
pads
DINn
VCCQ
VCCQ
PUP
ESD
vccp!
TO
FIG.
18-2
NEG
DQ<Ø:7>
DQn
for lvs only
PDN
ESD
VSSQ
VSSQ

FIG. 20

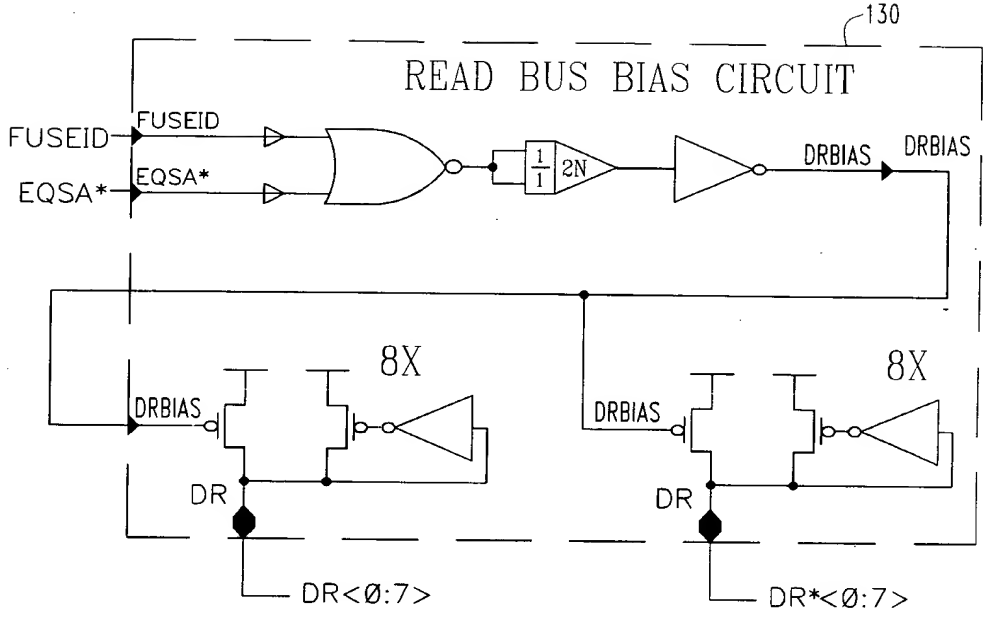

130
READ BUS BIAS CIRCUIT
FUSEID
FUSEID
EQSA*
EQSA*
1/1
2N
DRBIAS
DRBIAS
8X
8X
DRBIAS
DRBIAS
DR
DR
DR<Ø:7>
DR*<Ø:7>

FIG. 21

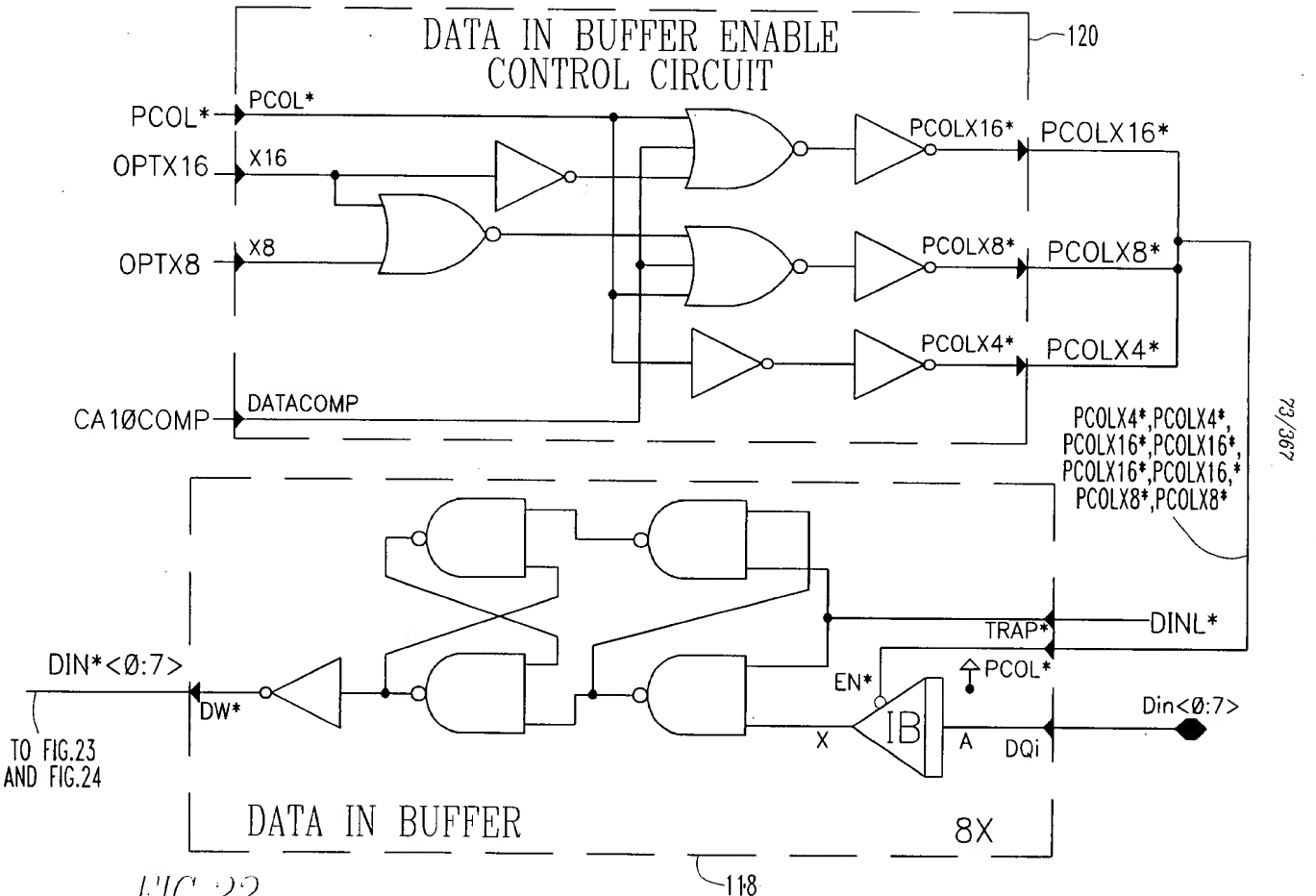
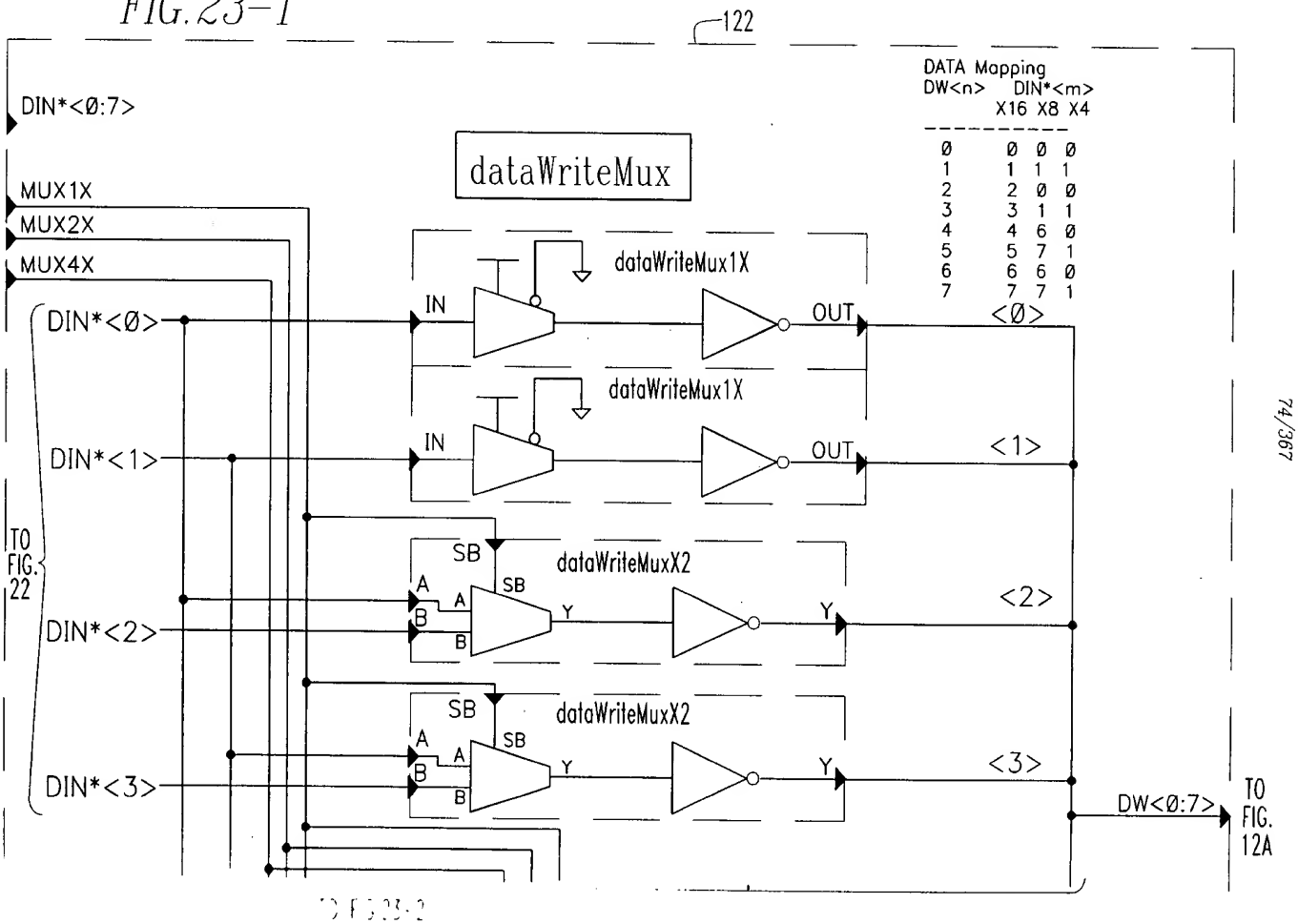

DATA IN BUFFER ENABLE CONTROL CIRCUIT
120
PCOL*
PCOL*
OPTX16
X16
OPTX8
X8
CA1ØCOMP
DATACOMP
PCOLX16*
PCOLX16*
PCOLX8*
PCOLX8*
PCOLX4*
PCOLX4*
PCOLX4*,PCOLX4*,
PCOLX16*,PCOLX16*,
PCOLX16*,PCOLX16,*
PCOLX8*,PCOLX8*
DIN*<Ø:7>
TO FIG.23
AND FIG.24
DW*
TRAP*
DINL*
EN*
PCOL*
IB
X
A
DQi
Din<Ø:7>
DATA IN BUFFER
8X
118

FIG 22

FIG. 23-1


122
DIN*<0:7>
MUX1X
MUX2X
MUX4X
DIN*<0>
DIN*<1>
DIN*<2>
DIN*<3>
TO FIG. 22
dataWriteMux
dataWriteMux1X
IN
OUT
dataWriteMux1X
IN
OUT
SB
dataWriteMuxX2
A
B
SB
Y
Y
SB
dataWriteMuxX2
A
B
SB
Y
Y
DATA Mapping
DW<n> DIN*<m>
X16 X8 X4
0 0 0 0
1 1 1 1
2 2 0 0
3 3 1 1
4 4 6 0
5 5 7 1
6 6 6 0
7 7 7 1
<0>
<1>
<2>
<3>
DW<0:7>
TO FIG. 12A

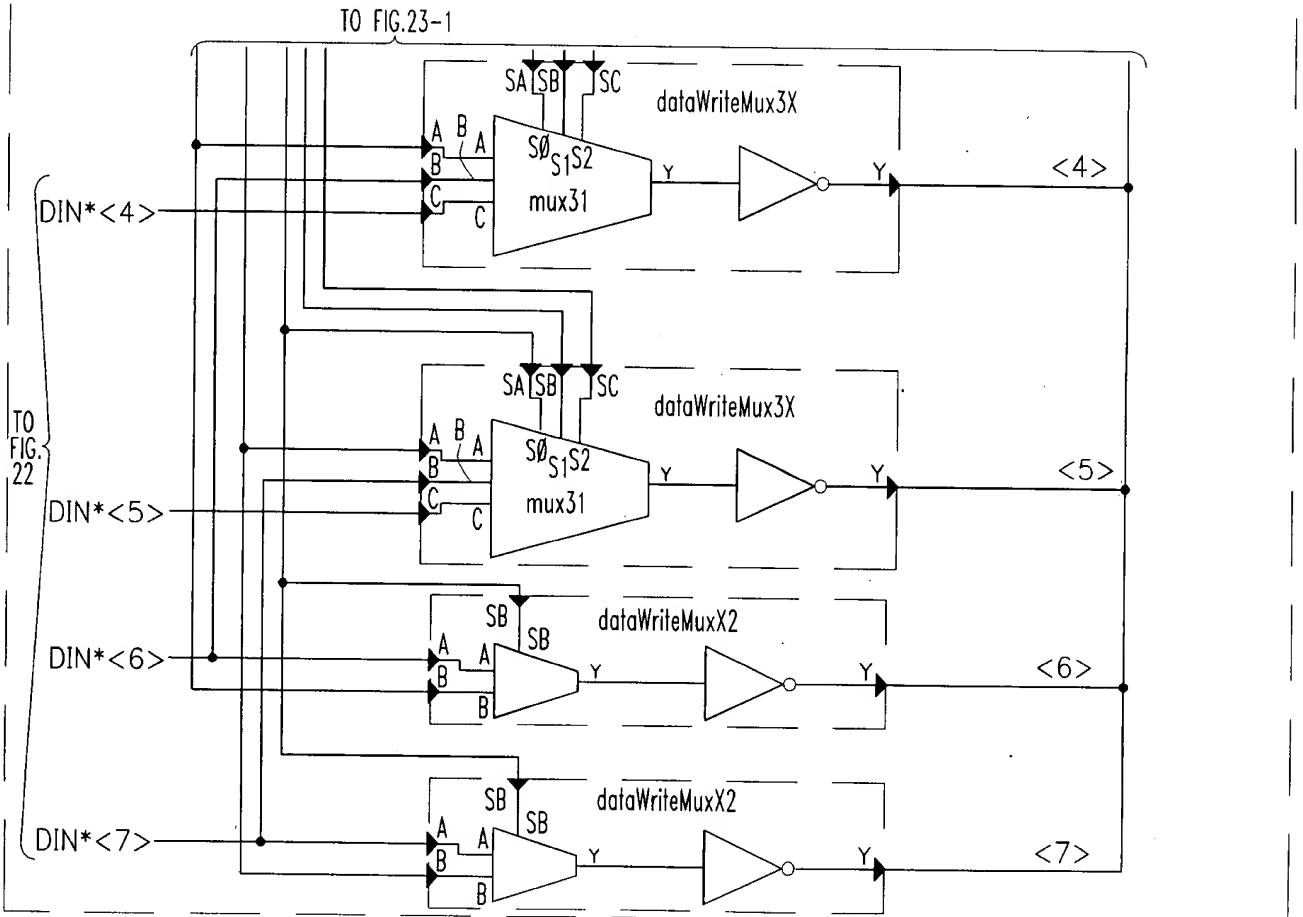

TO FIG.23-1
SA
SB
SC
dataWriteMux3X
A
B
C
mux31
S1
S2
Y
<4>
DIN*<4>
TO FIG. 22
<5>
DIN*<5>
dataWriteMuxX2
<6>
DIN*<6>
<7>
DIN*<7>
122

FIG. 23-2

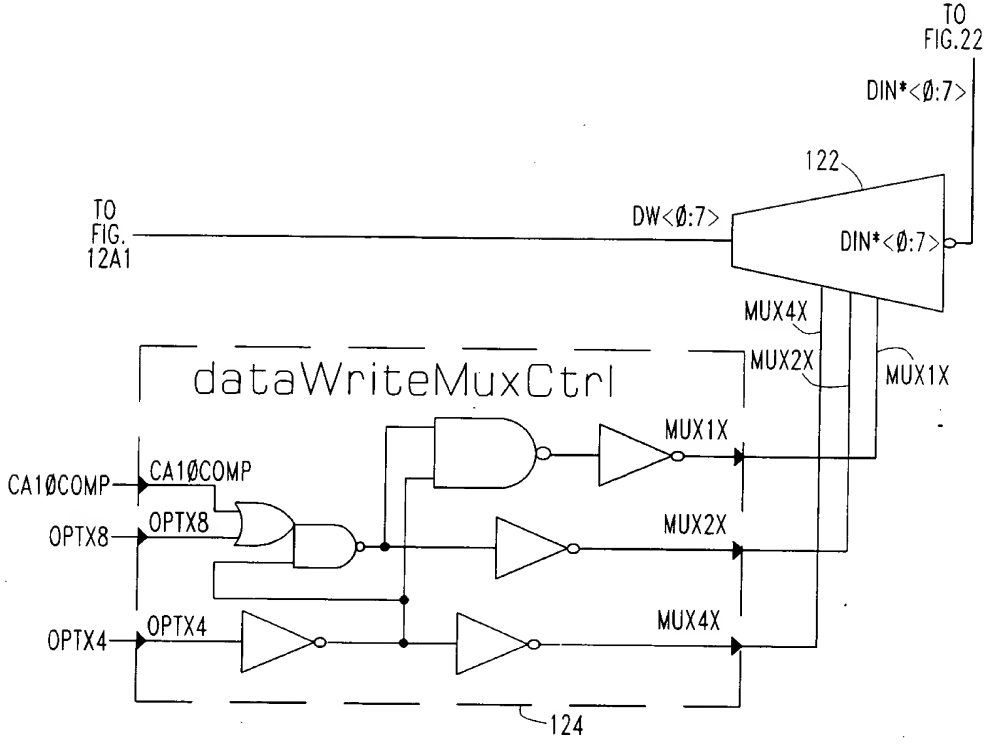

TO
FIG.22
DIN*<Ø:7>
122
TO
FIG.
12A1
DW<Ø:7>
DIN*<Ø:7>
MUX4X
MUX2X
MUX1X
dataWriteMuxCtrl
MUX1X
CA1ØCOMP
CA1ØCOMP
OPTX8
MUX2X
OPTX4
OPTX4
MUX4X
124

FIG. 24

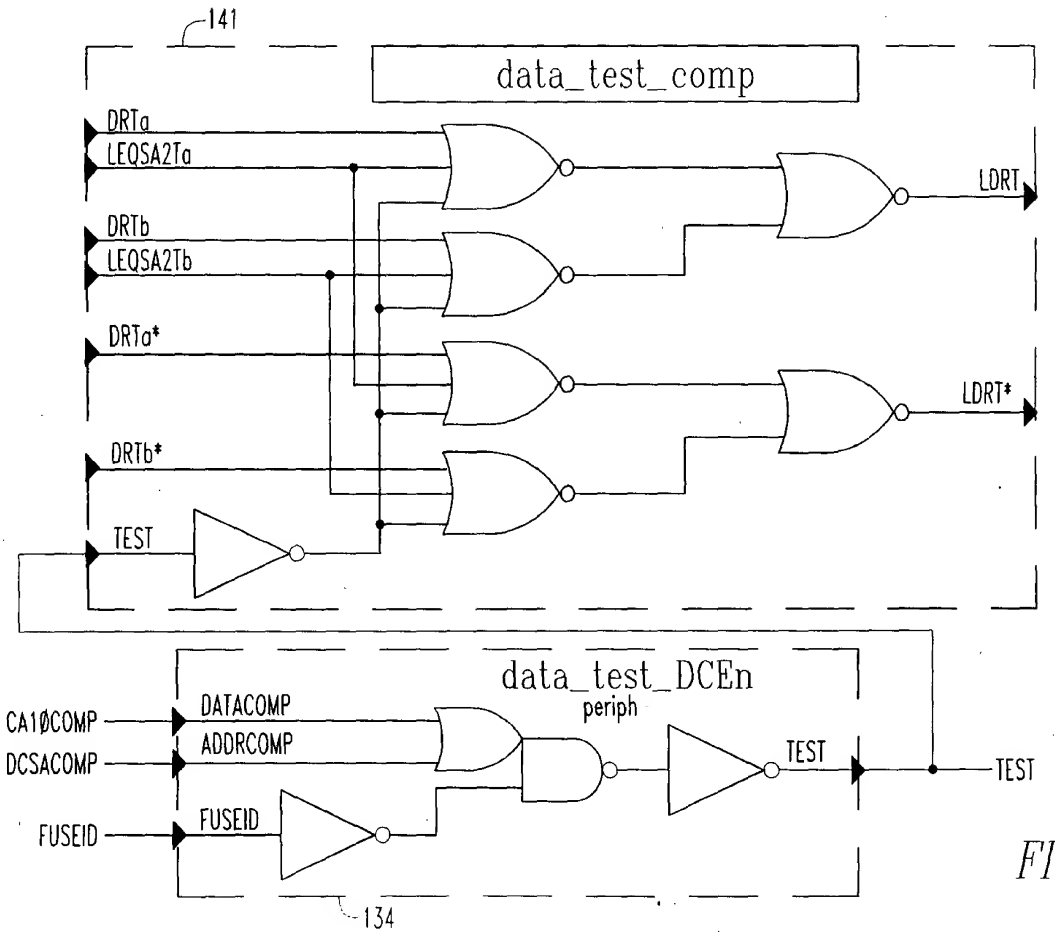

141
data_test_comp
DRTa
LEQSA2Ta
DRTb
LEQSA2Tb
DRTa*
DRTb*
TEST
LDRT
LDRT*
data_test_DCEn
periph
CA1ØCOMP
DCSACOMP
FUSEID
DATACOMP
ADDRCOMP
FUSEID
TEST
TEST
134

FIG.25

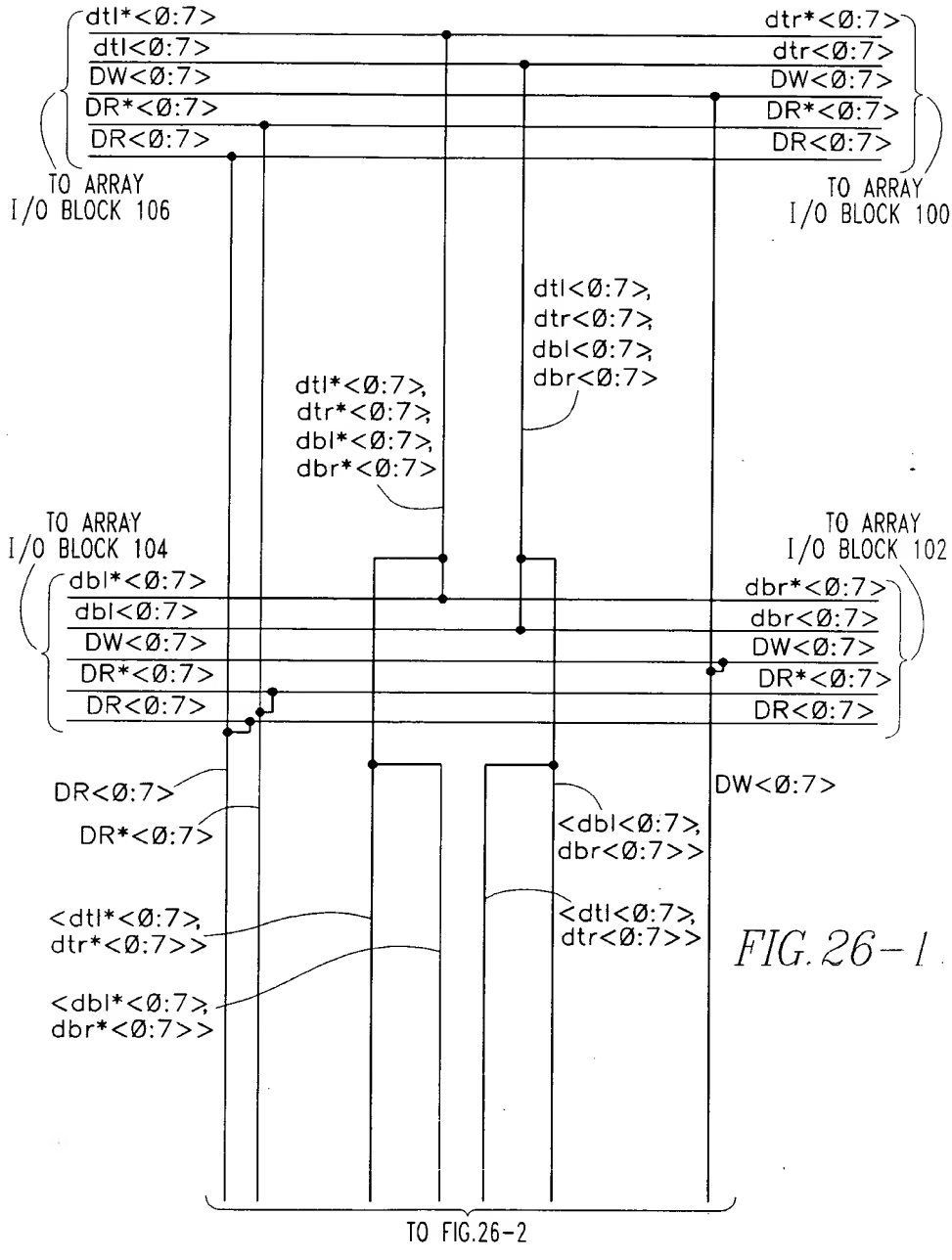

dtl*<Ø:7>
dtl<Ø:7>
DW<Ø:7>
DR*<Ø:7>
DR<Ø:7>
TO ARRAY I/O BLOCK 106
dtr*<Ø:7>
dtr<Ø:7>
DW<Ø:7>
DR*<Ø:7>
DR<Ø:7>
TO ARRAY I/O BLOCK 100
dtl<Ø:7>, dtr<Ø:7>, dbl<Ø:7>, dbr<Ø:7>
dtl*<Ø:7>, dtr*<Ø:7>, dbl*<Ø:7>, dbr*<Ø:7>
TO ARRAY I/O BLOCK 104
dbl*<Ø:7>
dbl<Ø:7>
DW<Ø:7>
DR*<Ø:7>
DR<Ø:7>
TO ARRAY I/O BLOCK 102
dbr*<Ø:7>
dbr<Ø:7>
DW<Ø:7>
DR*<Ø:7>
DR<Ø:7>
DR<Ø:7>
DR*<Ø:7>
<dtl*<Ø:7>, dtr*<Ø:7>>
<dbl*<Ø:7>, dbr*<Ø:7>>
DW<Ø:7>
<dbl<Ø:7>, dbr<Ø:7>>
<dtl<Ø:7>, dtr<Ø:7>>
TO FIG.26-2

FIG. 26-1

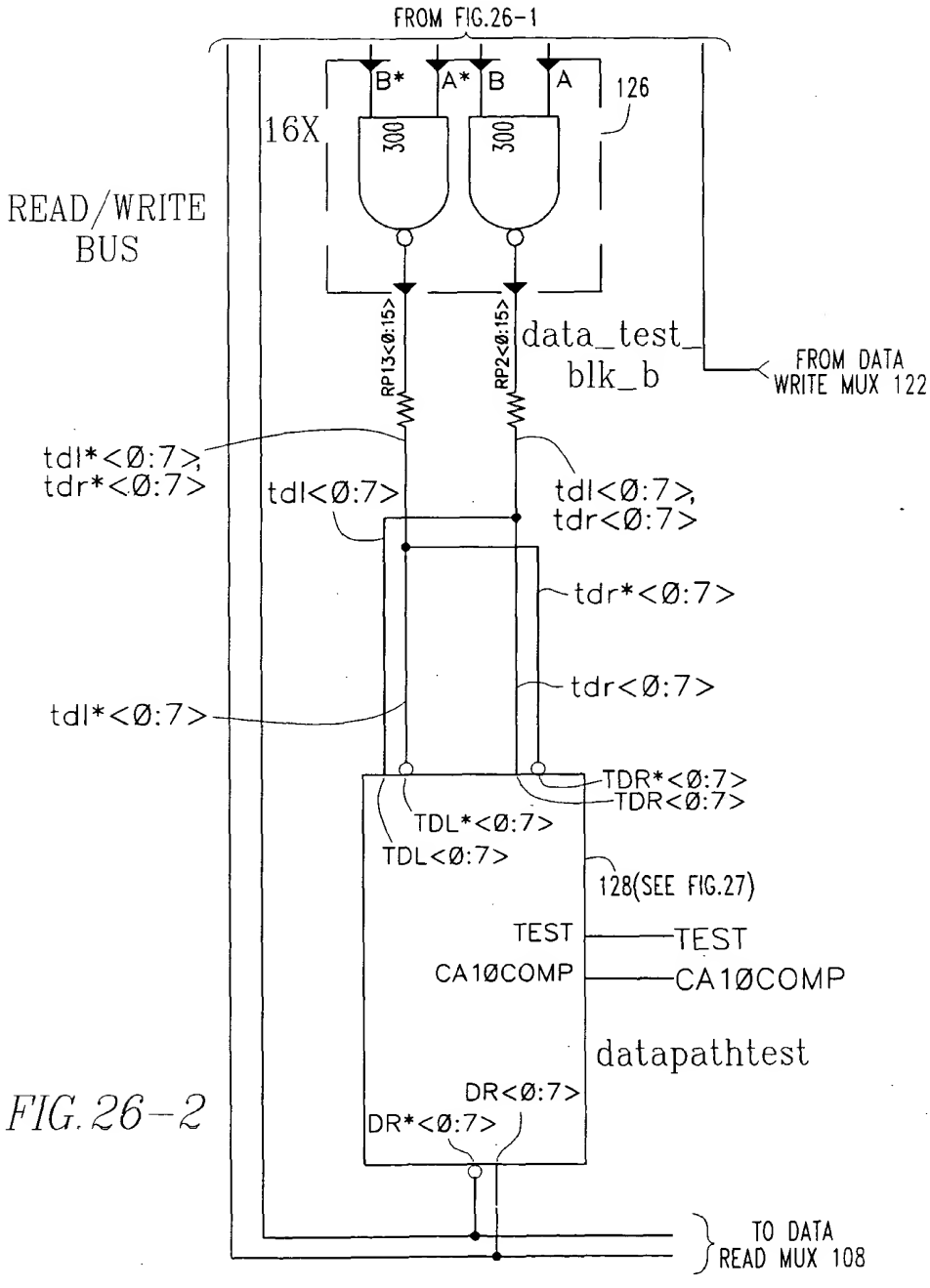

FROM FIG.26-1
B*
A*
B
A
126
16X
300
300
READ/WRITE BUS
RP13<0:15>
RP2<0:15>
data_test_blk_b
FROM DATA WRITE MUX 122
tdl*<0:7>; tdr*<0:7>
tdl<0:7>
tdl<0:7>; tdr<0:7>
tdr*<0:7>
tdr<0:7>
tdl*<0:7>
TDR*<0:7>
TDR<0:7>
TDL*<0:7>
TDL<0:7>
128(SEE FIG.27)
TEST
TEST
CA10COMP
CA10COMP
datapathtest
DR<0:7>
DR*<0:7>
TO DATA READ MUX 108

FIG. 26-2

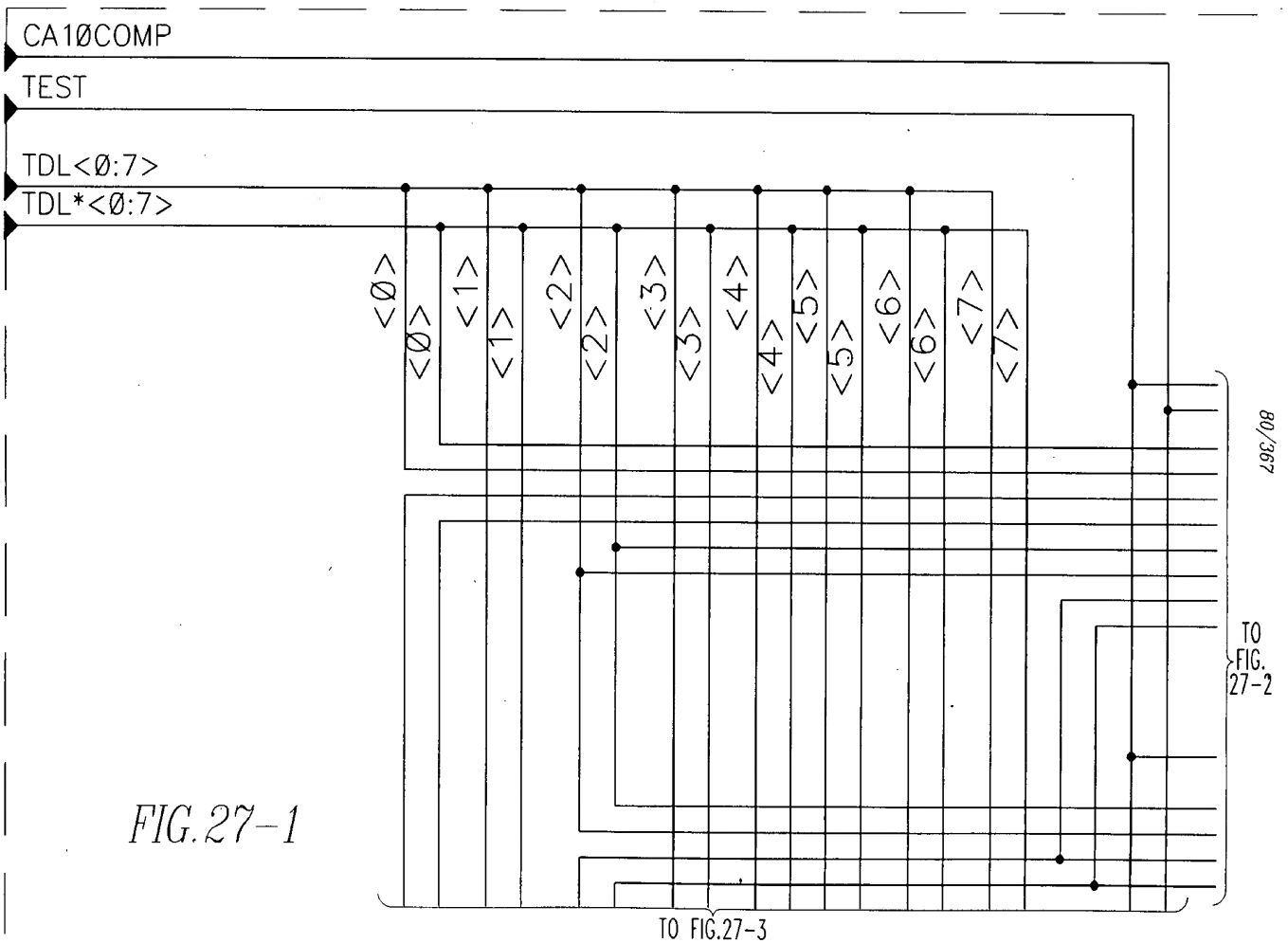
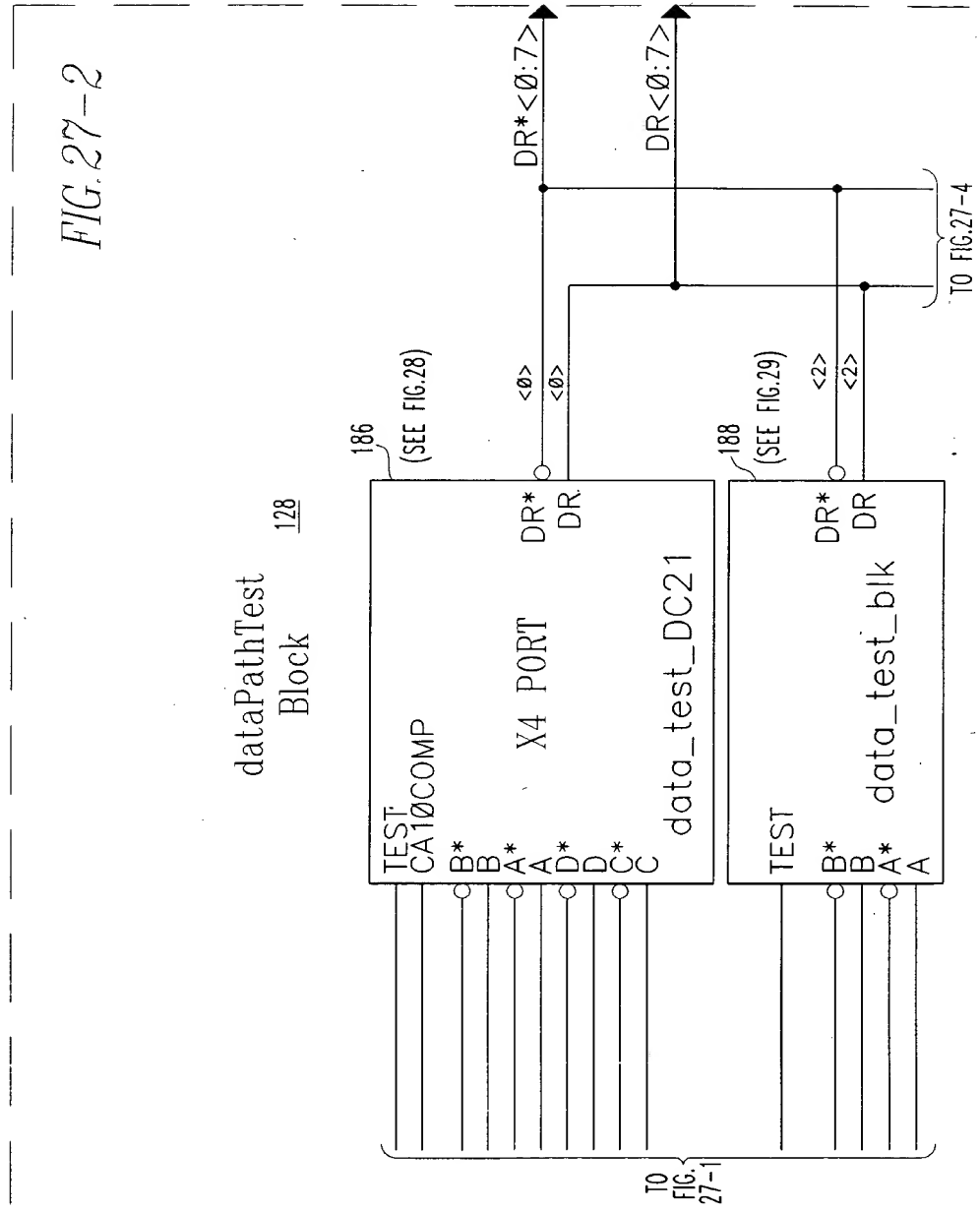

CA1ØCOMP
TEST
TDL<Ø:7>
TDL*<Ø:7>
<Ø>
<Ø>
<1>
<1>
<2>
<2>
<3>
<3>
<4>
<4>
<5>
<5>
<6>
<6>
<7>
<7>
TO FIG. 27-2
TO FIG.27-3

FIG. 27-1

FIG.27-2


dataPathTest
Block
128
186
(SEE FIG.28)
TEST
CA10COMP
B*
B
A*
A
D*
D
C*
C
X4 PORT
DR*
DR
data_test_DC21
<0>
<0>
DR*<0:7>
DR<0:7>
188
(SEE FIG.29)
TEST
B*
B
A*
A
data_test_blk
DR*
DR
<2>
<2>
TO FIG.27-4
TO FIG. 27-1

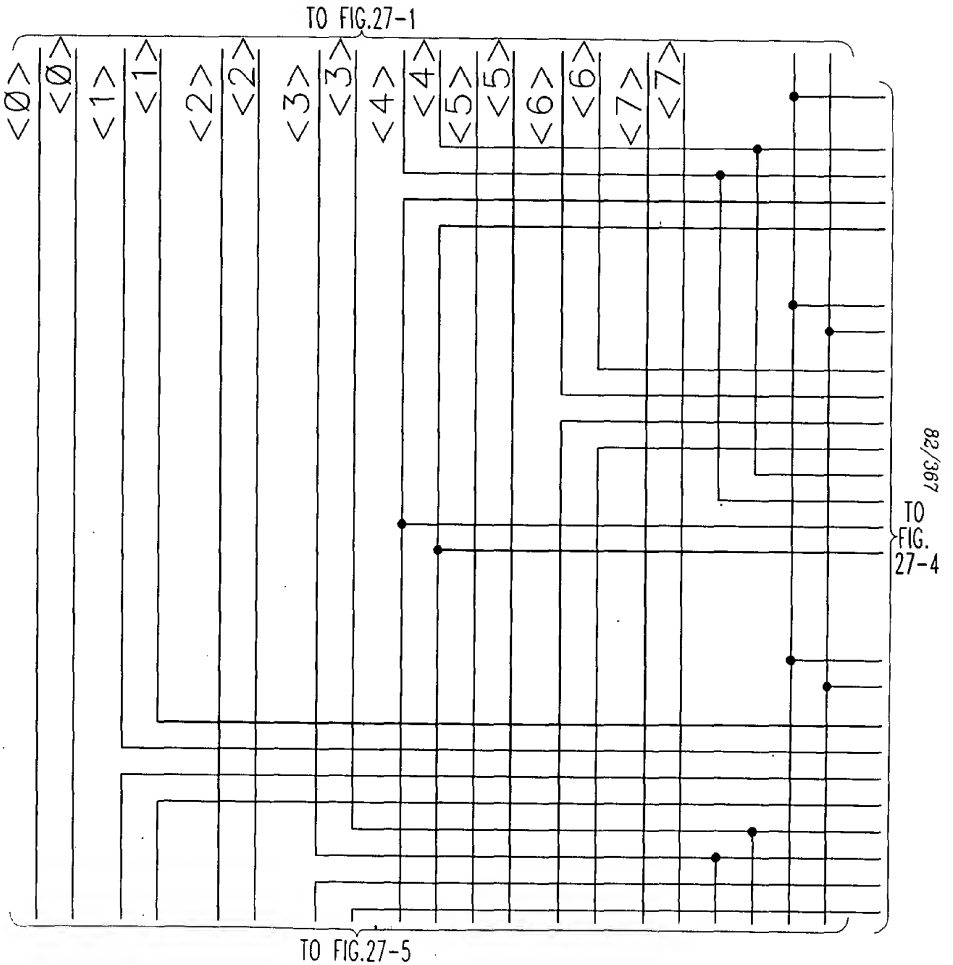


FIG 27-3

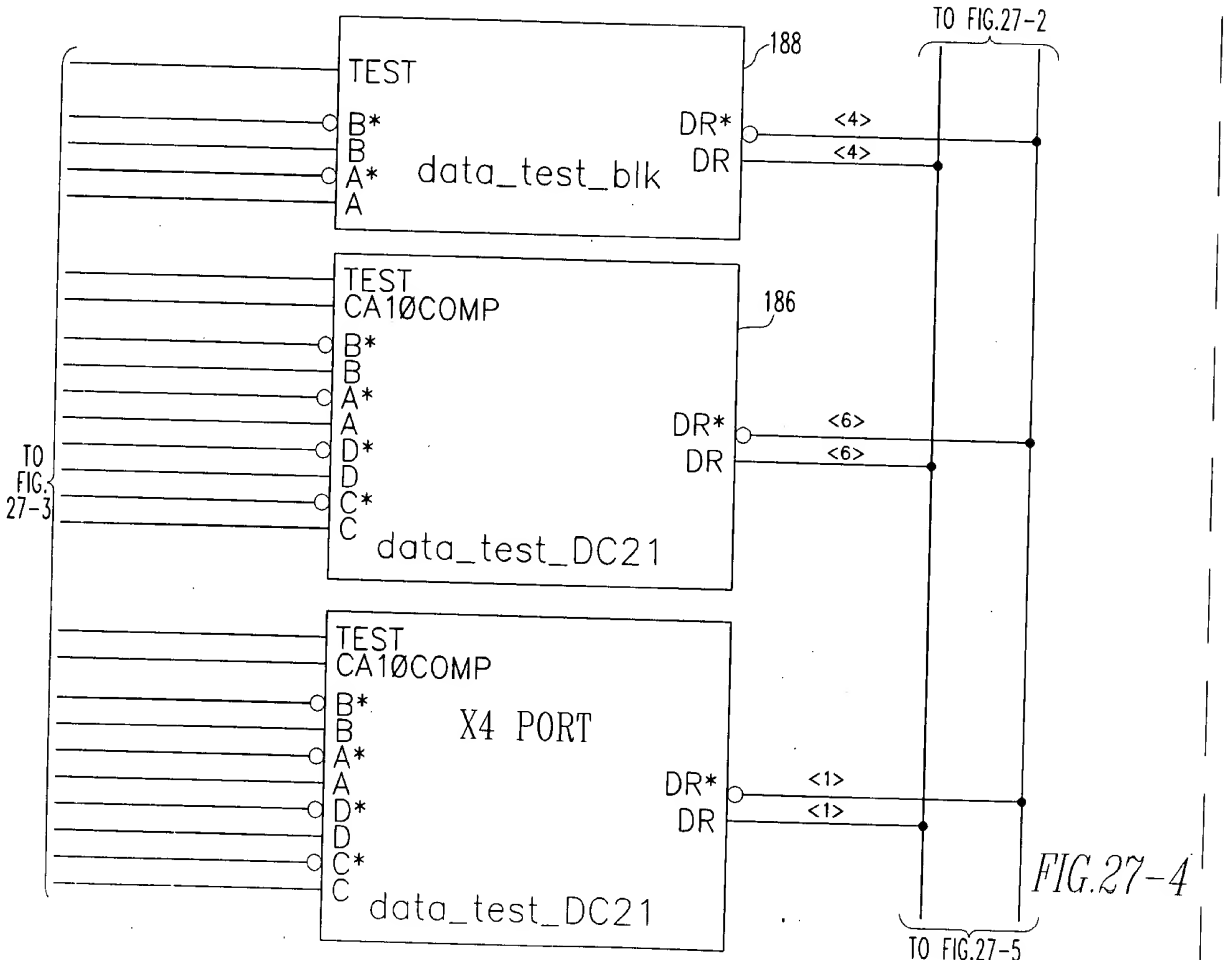
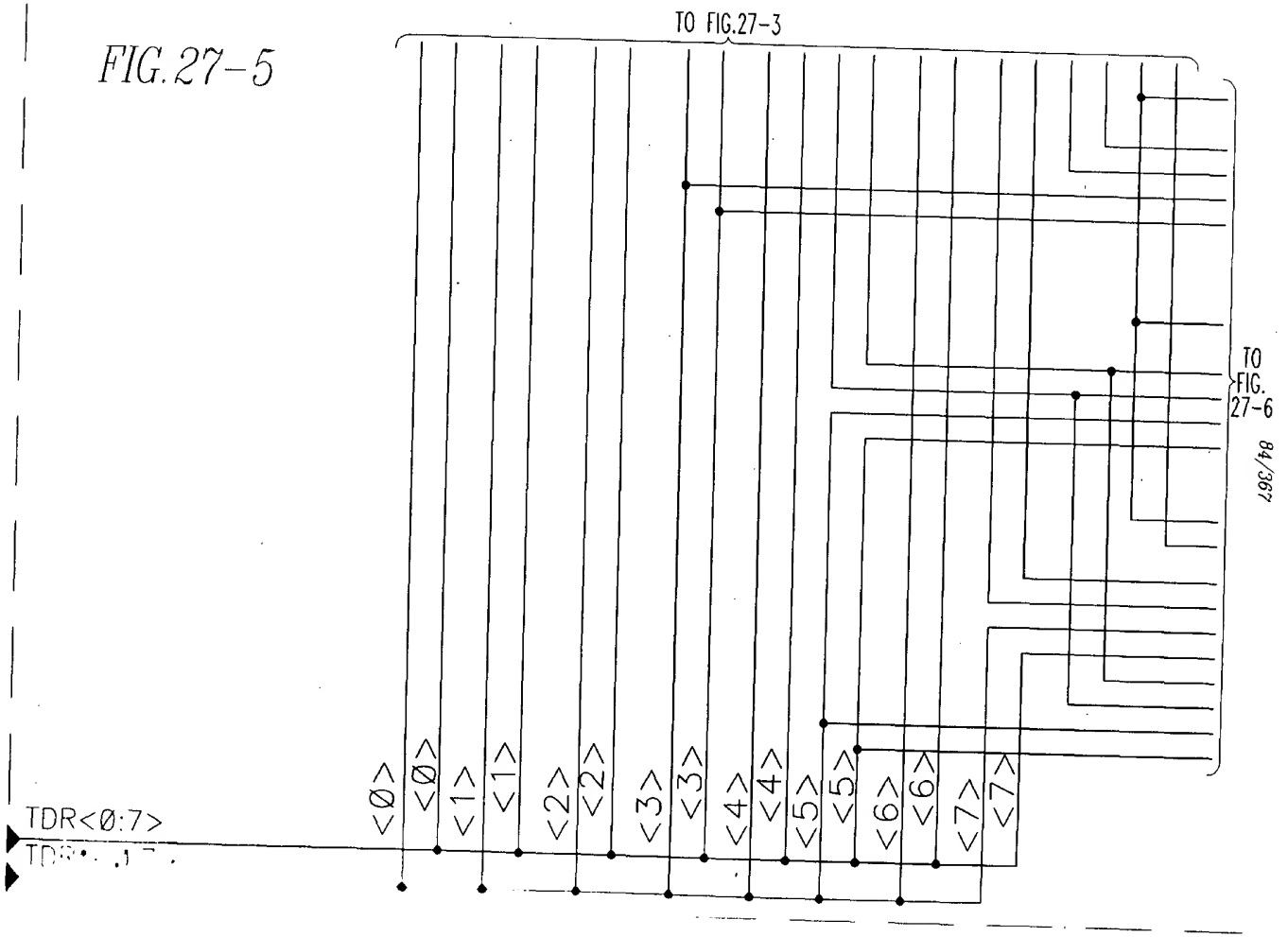

TO FIG.27-2
188
TEST
B*
B
A*
A
data_test_blk
DR*
DR
<4>
<4>
TEST
CA1ØCOMP
186
B*
B
A*
A
D*
D
C*
C
data_test_DC21
DR*
DR
<6>
<6>
TO FIG. 27-3
TEST
CA1ØCOMP
B*
B
A*
A
D*
D
C*
C
X4 PORT
data_test_DC21
DR*
DR
<1>
<1>
TO FIG.27-5

FIG.27-4

FIG. 27-5



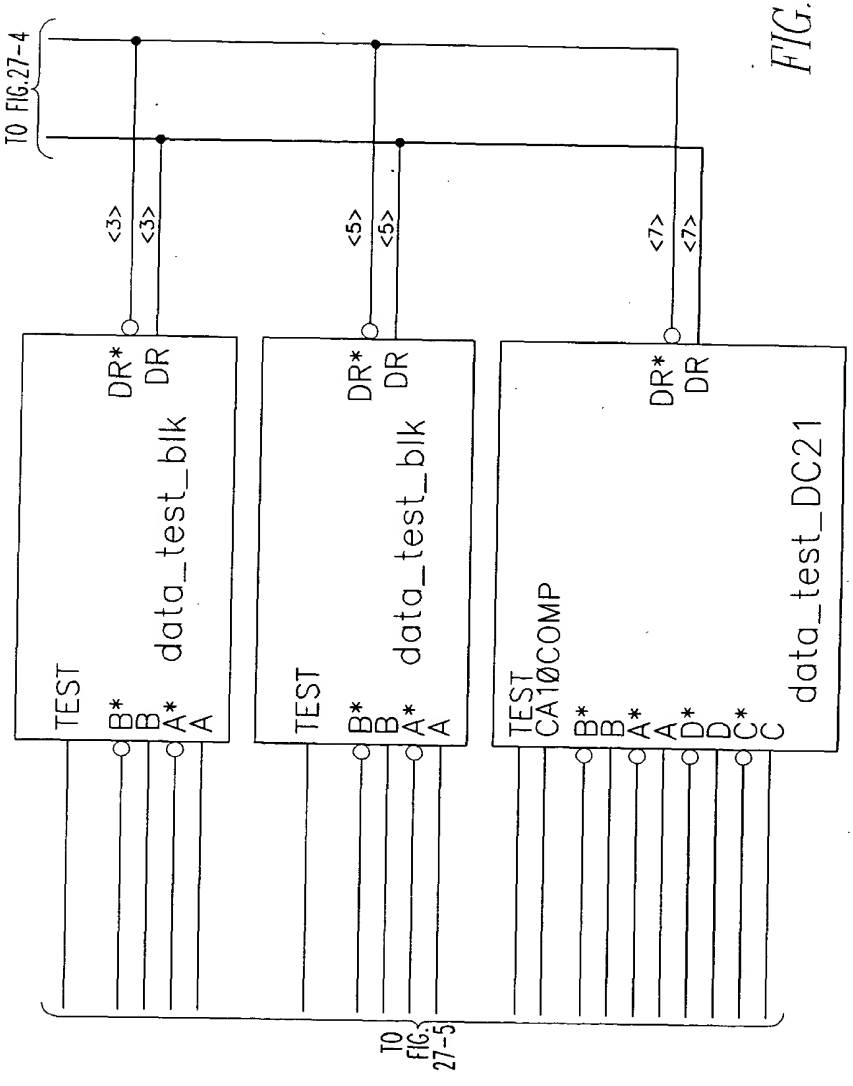

TO FIG.27-4
<3>
<3>
<5>
<5>
<7>
<7>
TEST
B*
B
A*
A
data_test_blk
DR*
DR
TEST
B*
B
A*
A
data_test_blk
DR*
DR
TEST
CA1ØCOMP
B*
B
A*
A
D*
D
C*
C
data_test_DC21
DR*
DR
TO FIG. 27-5

FIG. 27-6

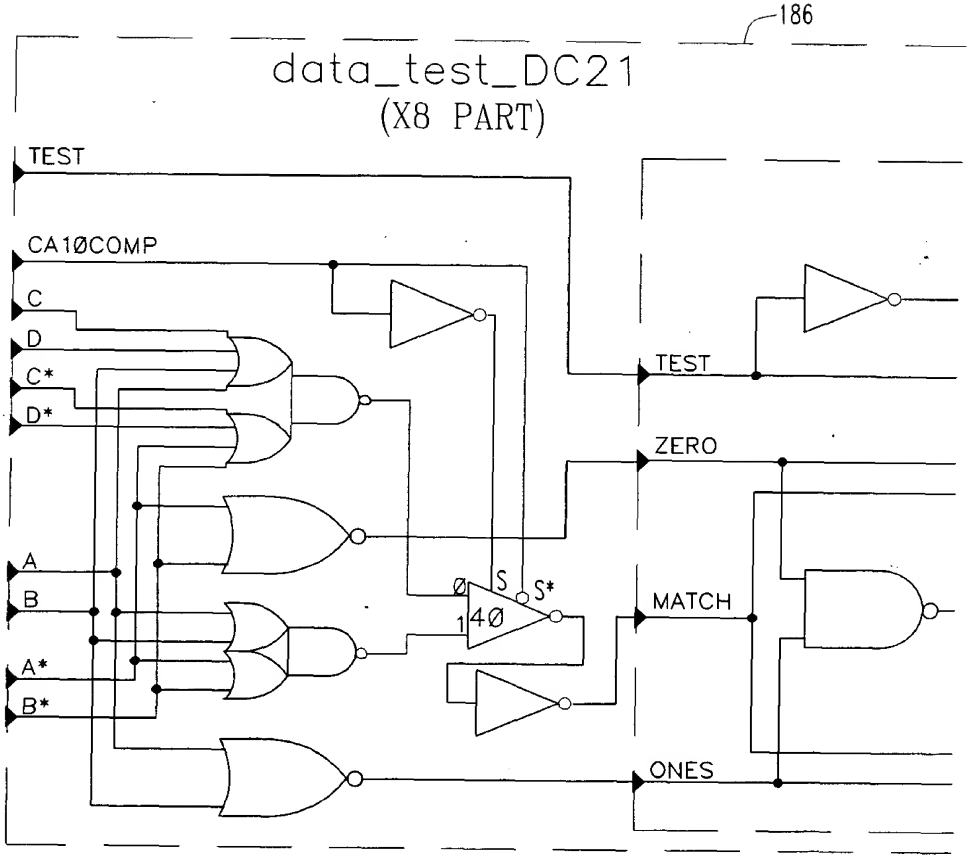

186
data_test_DC21
(X8 PART)
TEST
CA1ØCOMP
C
D
C*
D*
A
B
A*
B*
Ø
S
S*
1
4Ø
TEST
ZERO
MATCH
ONES

FIG. 28-1

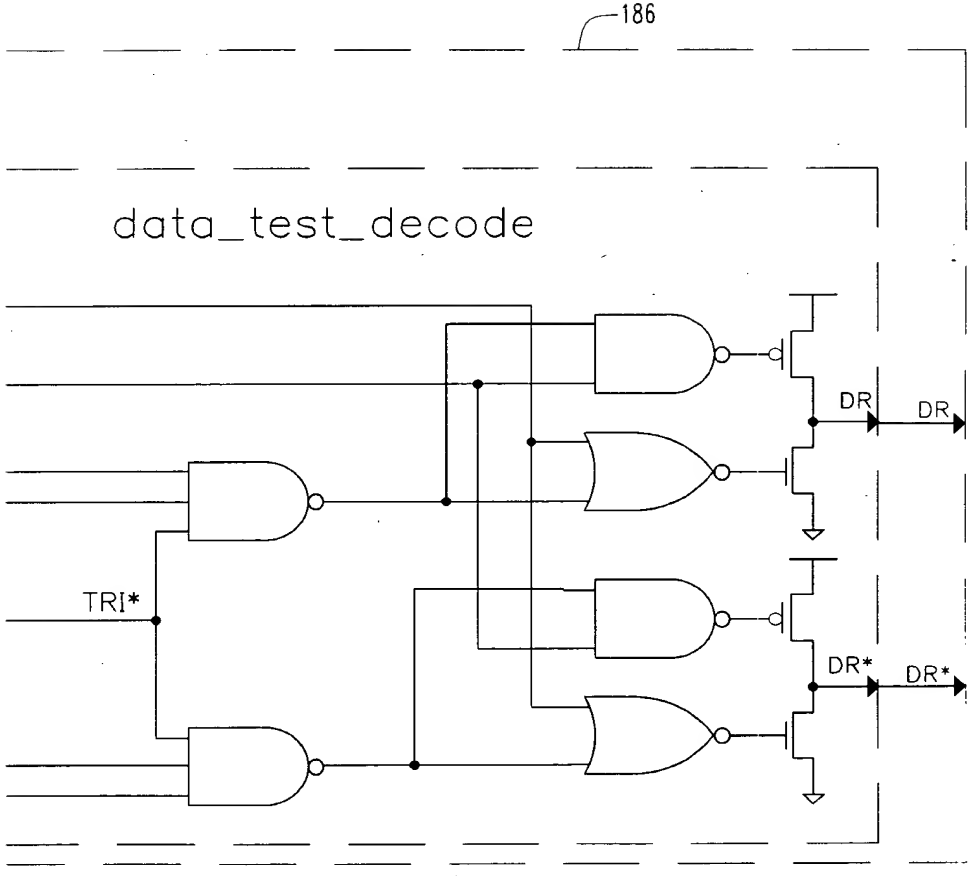


FIG. 28-2

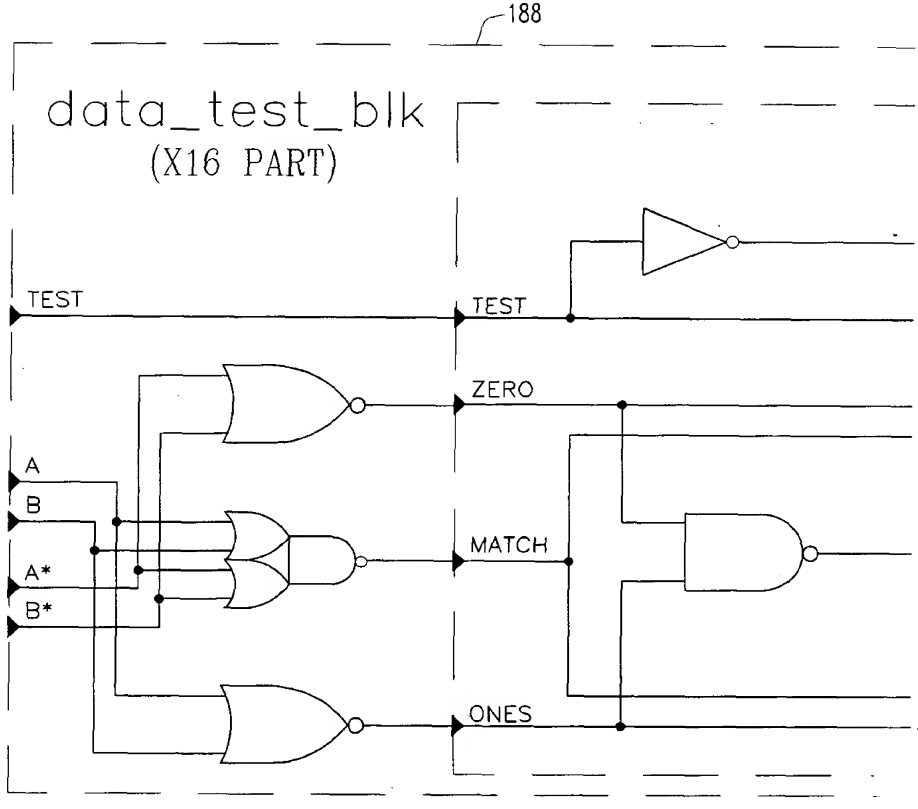


FIG. 29-1

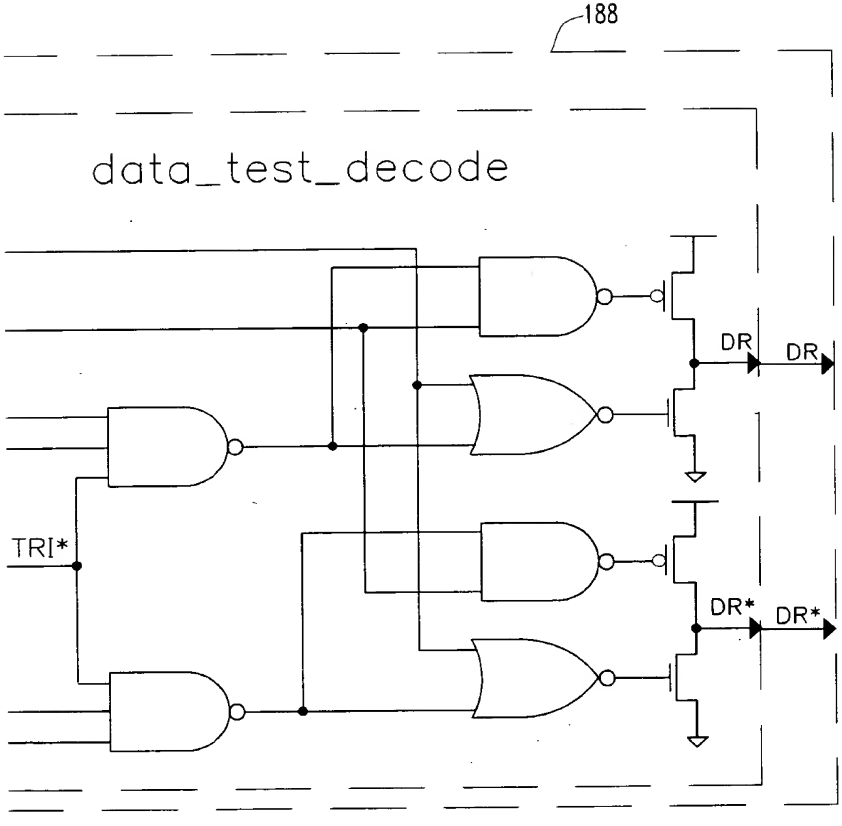


FIG. 29-2

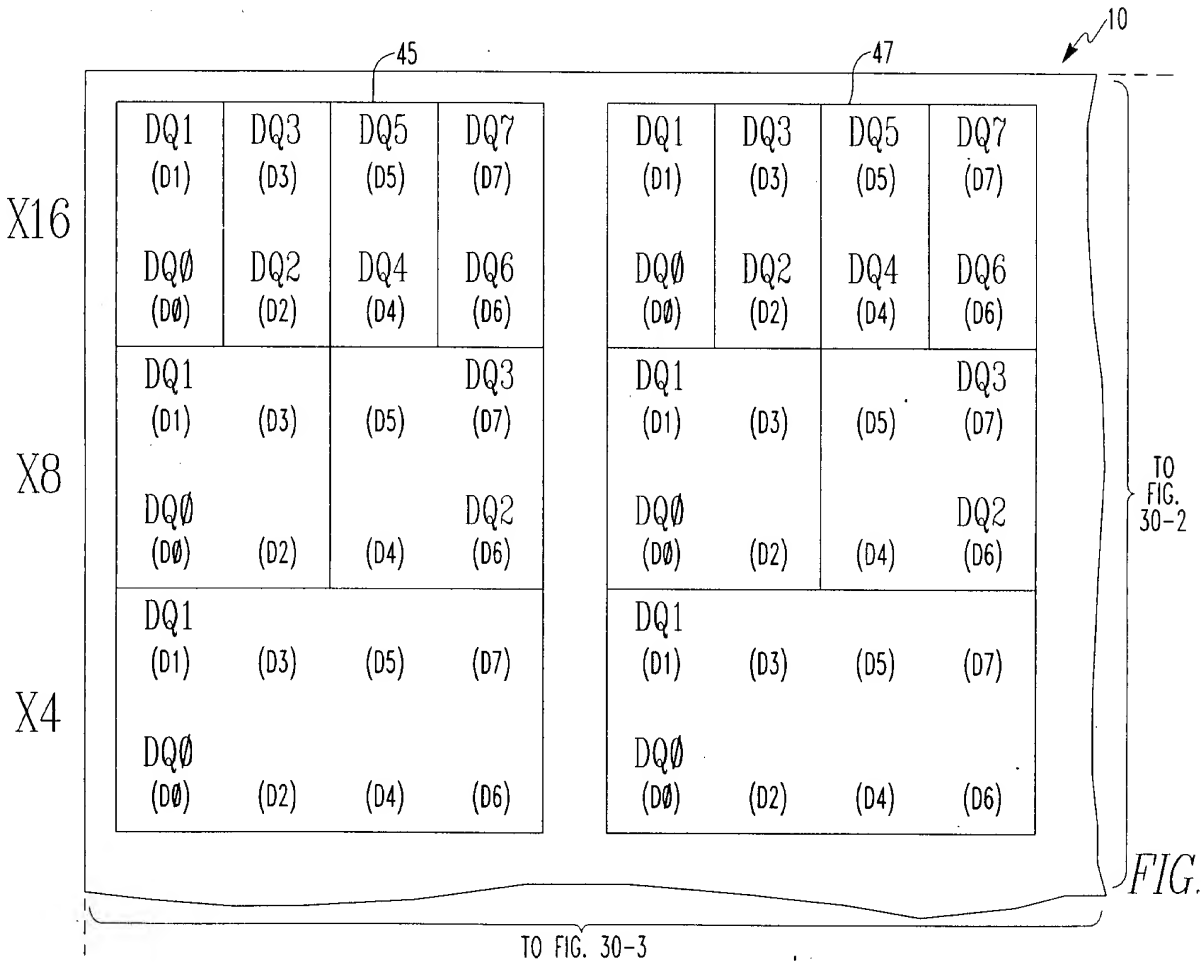

10
45
47
X16
X8
X4
DQ1 (D1) DQ3 (D3) DQ5 (D5) DQ7 (D7)
DQØ (DØ) DQ2 (D2) DQ4 (D4) DQ6 (D6)
DQ1 (D1) (D3) (D5) DQ3 (D7)
DQØ (DØ) (D2) (D4) DQ2 (D6)
DQ1 (D1) (D3) (D5) (D7)
DQØ (DØ) (D2) (D4) (D6)
TO FIG. 30-2
TO FIG. 30-3

FIG. 30-1

TOSHIBA 6257B636

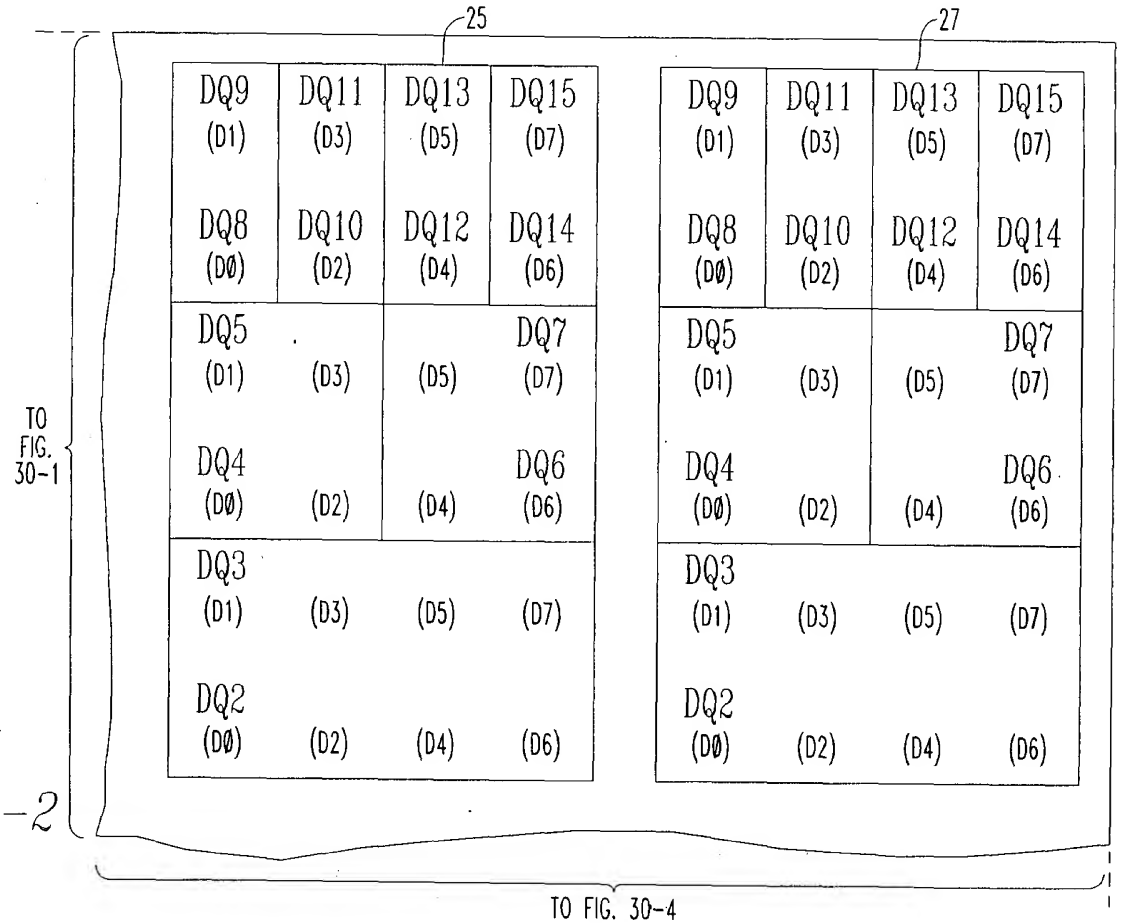


FIG. 30-2

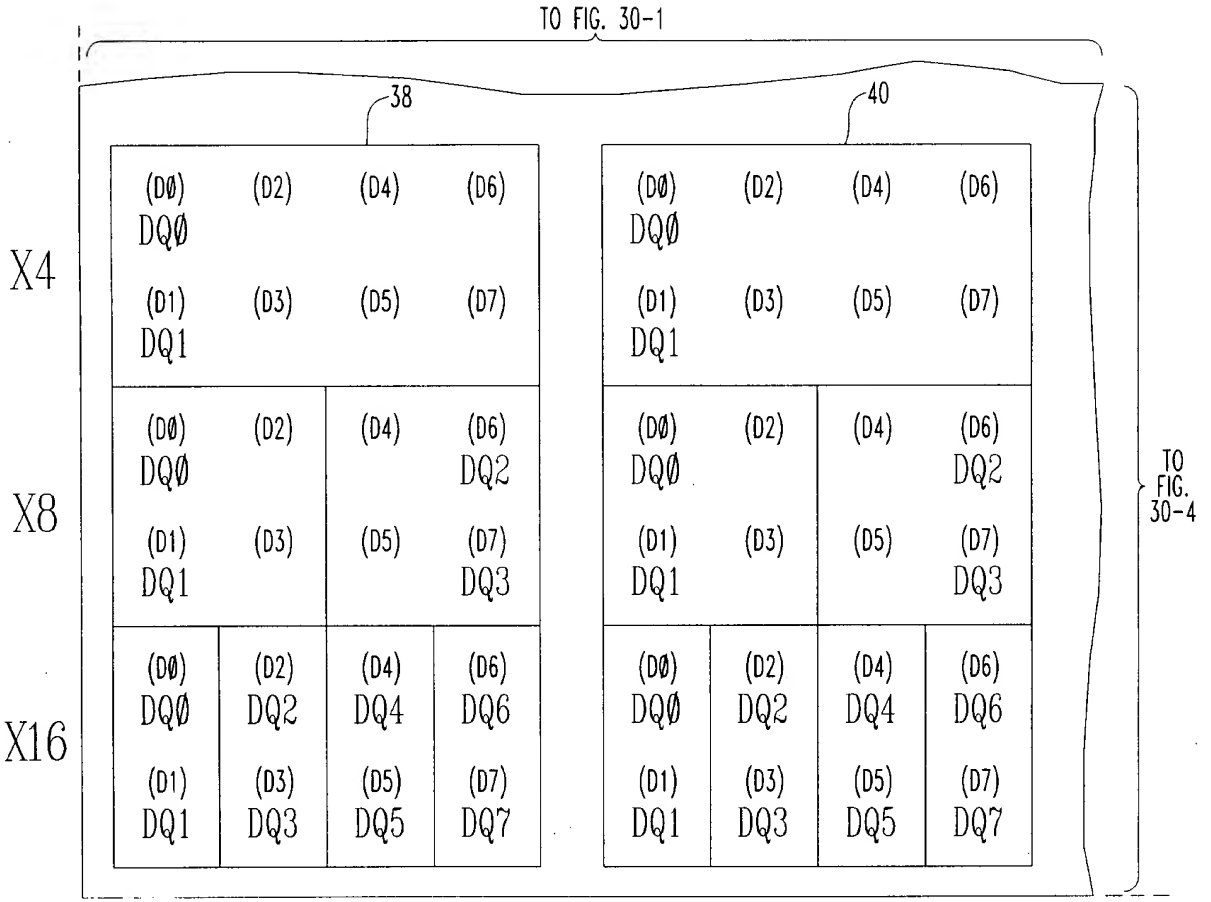

TO FIG. 30-1
38
40
X4
X8
X16
(DØ) DQØ
(D1) DQ1
(D2)
(D3)
(D4)
(D5)
(D6) DQ2
(D7) DQ3
DQ4
DQ5
DQ6
DQ7
TO FIG. 30-4

FIG. 30-3

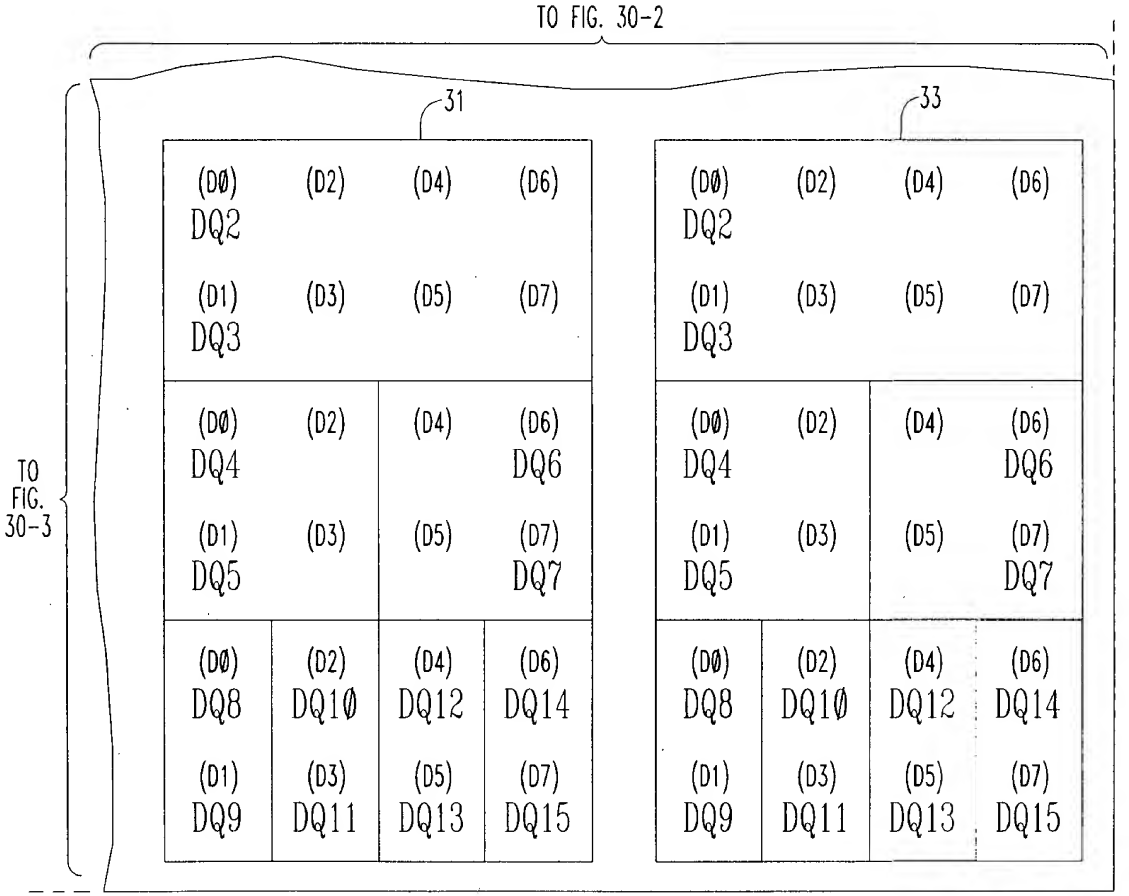

TO FIG. 30-2
31
33
(DØ) DQ2
(D2)
(D4)
(D6)
(D1) DQ3
(D3)
(D5)
(D7)
(DØ) DQ4
(D2)
(D4)
(D6) DQ6
(D1) DQ5
(D3)
(D5)
(D7) DQ7
(DØ) DQ8
(D2) DQ1Ø
(D4) DQ12
(D6) DQ14
(D1) DQ9
(D3) DQ11
(D5) DQ13
(D7) DQ15
TO FIG. 30-3

FIG 30-1

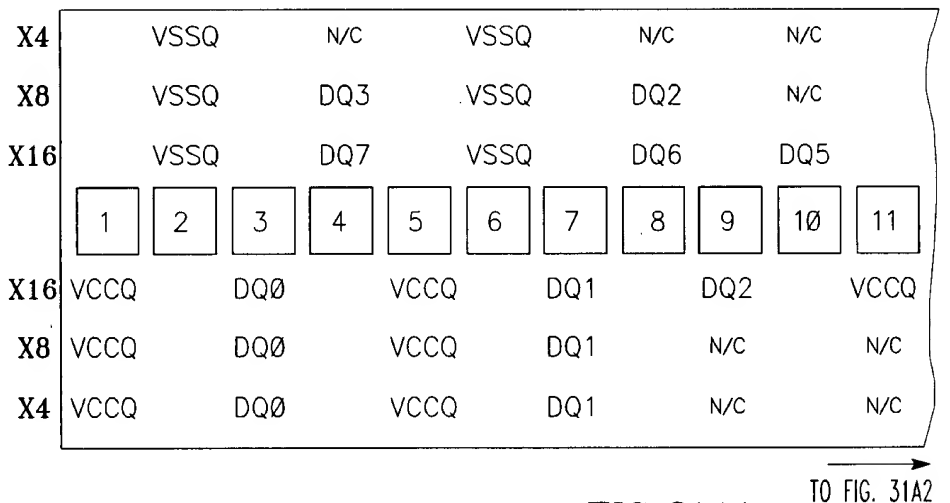

X4 VSSQ N/C VSSQ N/C N/C
X8 VSSQ DQ3 VSSQ DQ2 N/C
X16 VSSQ DQ7 VSSQ DQ6 DQ5
1 2 3 4 5 6 7 8 9 10 11
X16 VCCQ DQ0 VCCQ DQ1 DQ2 VCCQ
X8 VCCQ DQ0 VCCQ DQ1 N/C N/C
X4 VCCQ DQ0 VCCQ DQ1 N/C N/C
TO FIG. 31A2

FIG. 31A1

TO FIG. 31A1

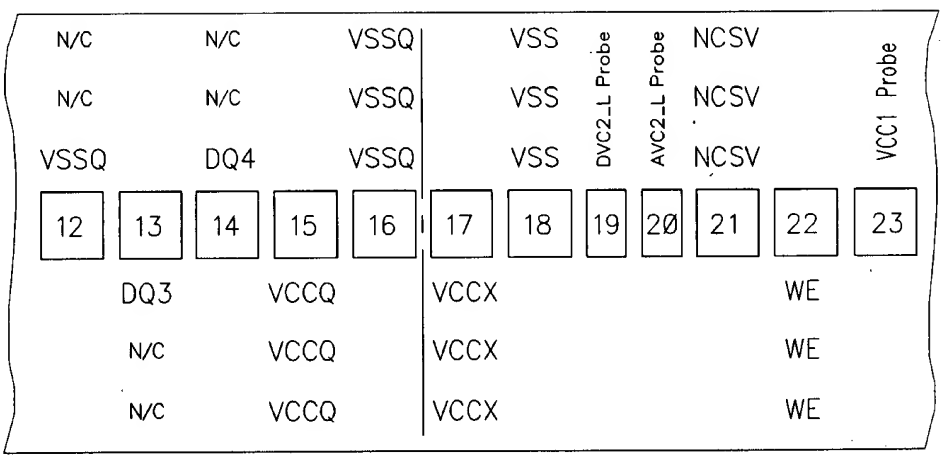


FIG. 31A2

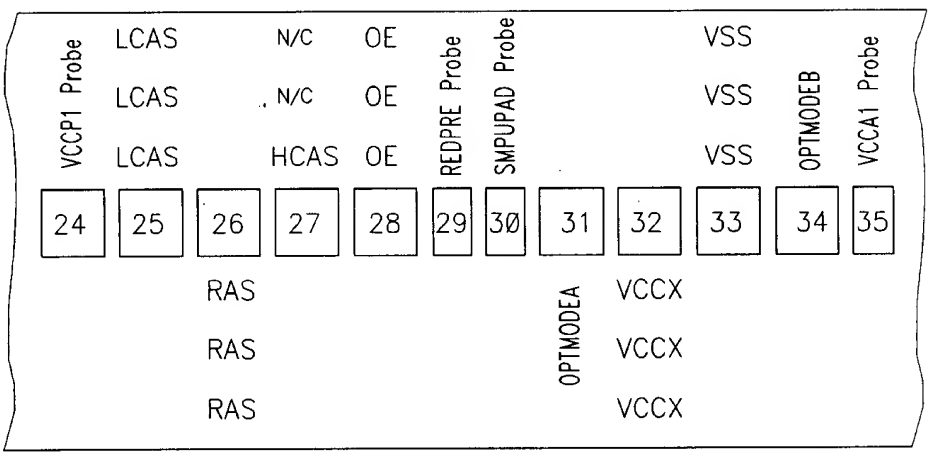

VCCP1 Probe
LCAS
LCAS
LCAS
N/C
N/C
HCAS
OE
OE
OE
REDPRE Probe
SMPUPAD Probe
VSS
VSS
VSS
OPTMODEB
VCCA1 Probe
24
25
26
27
28
29
30
31
32
33
34
35
RAS
RAS
RAS
OPTMODEA
VCCX
VCCX
VCCX
TO FIG. 31B2

FIG. 31B1

Tested: 8257860

TO FIG. 31B1

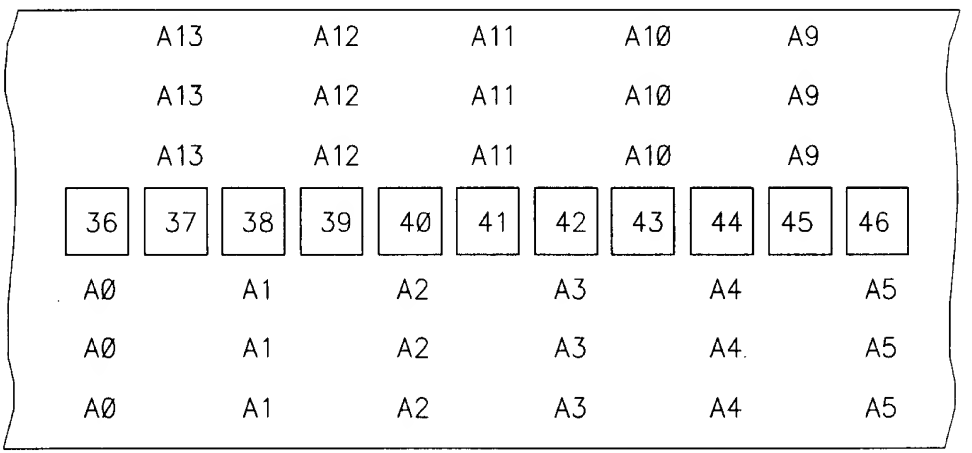


FIG. 31B2

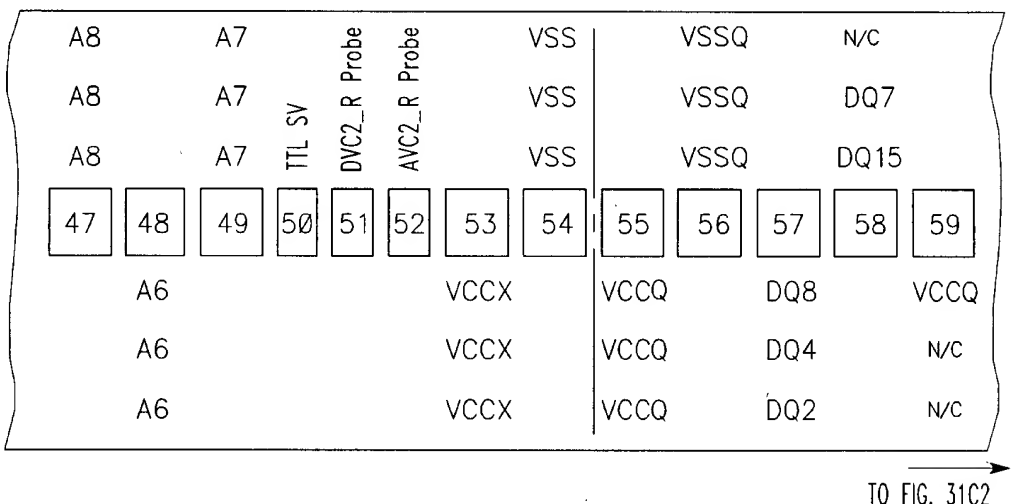

A8
A8
A8
A7
A7
A7
TTL SV
DVC2_R Probe
AVC2_R Probe
VSS
VSS
VSS
VSSQ
VSSQ
VSSQ
N/C
DQ7
DQ15
47
48
49
50
51
52
53
54
55
56
57
58
59
A6
A6
A6
VCCX
VCCX
VCCX
VCCQ
VCCQ
VCCQ
DQ8
DQ4
DQ2
VCCQ
N/C
N/C
TO FIG. 31C2

FIG. 31C1

TO FIG. 31C1

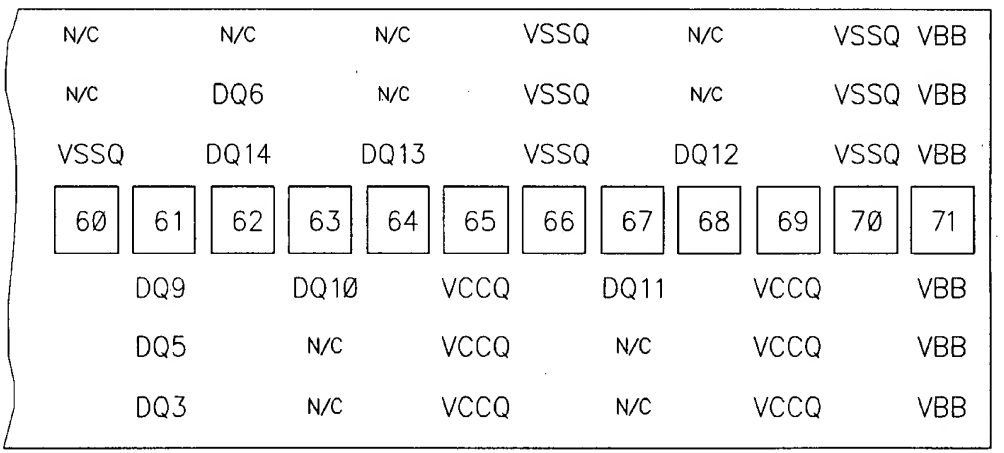


FIG. 31C2

TOSHIBA 8297860

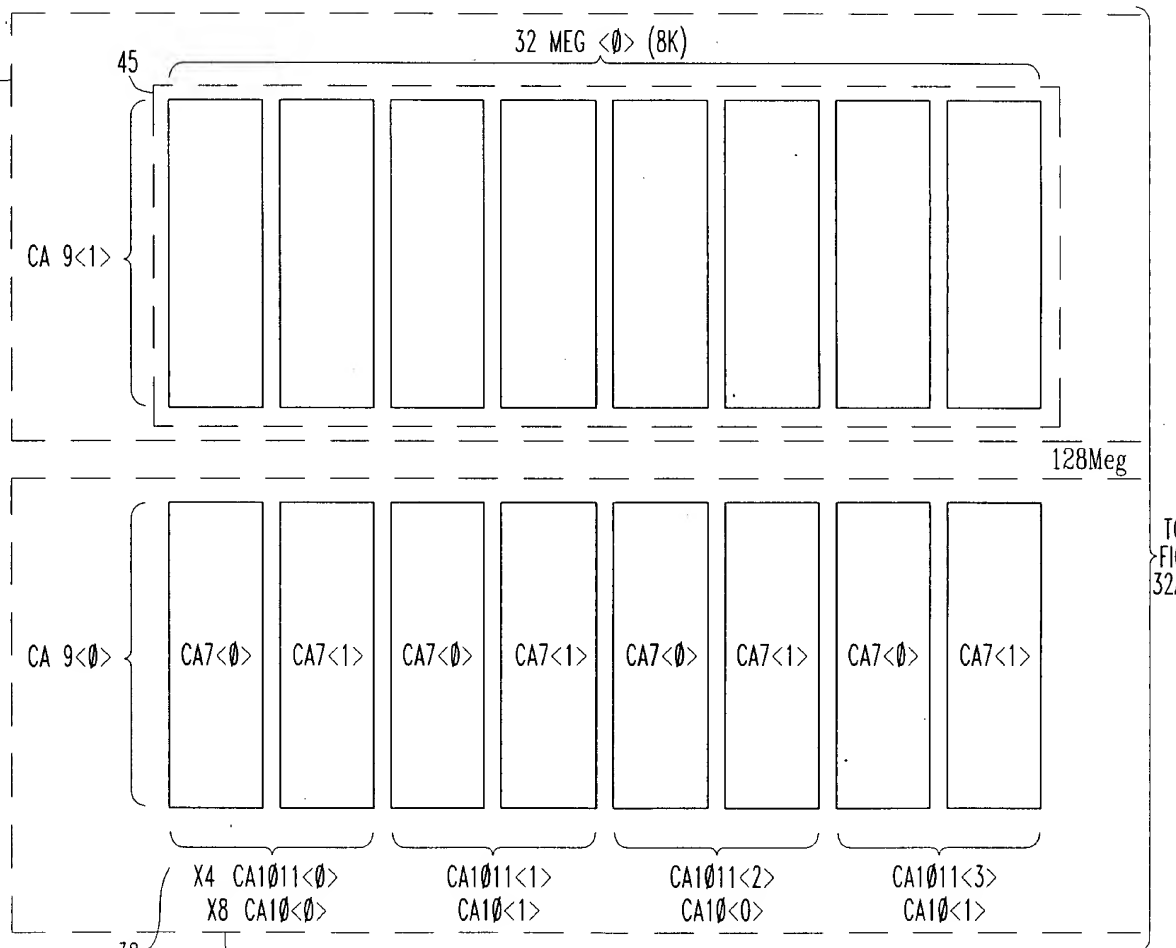
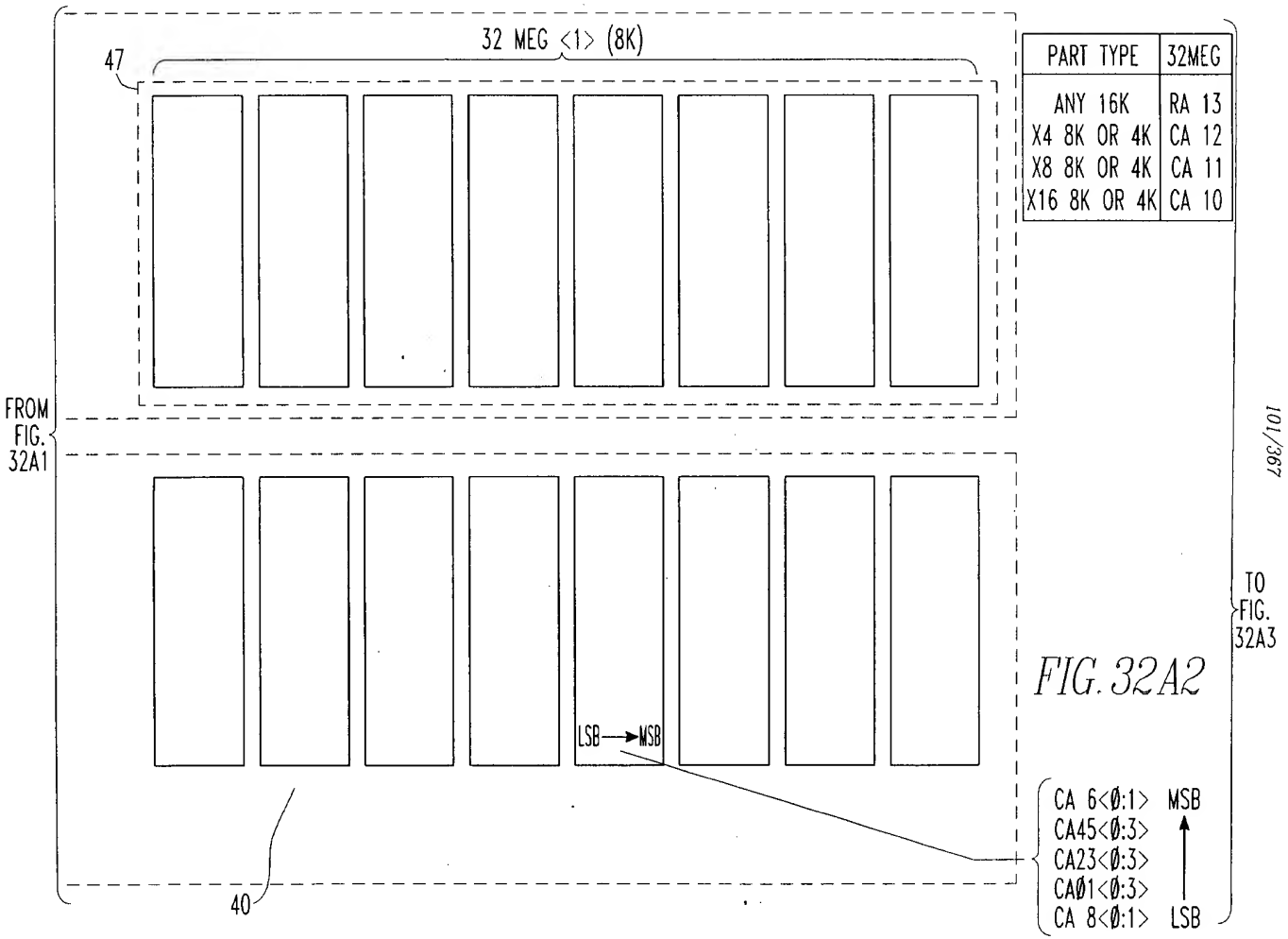


FIG.32A1



PART TYPE	32MEG
ANY 16K	RA 13
X4 8K OR 4K	CA 12
X8 8K OR 4K	CA 11
X16 8K OR 4K	CA 10

FIG. 32A2

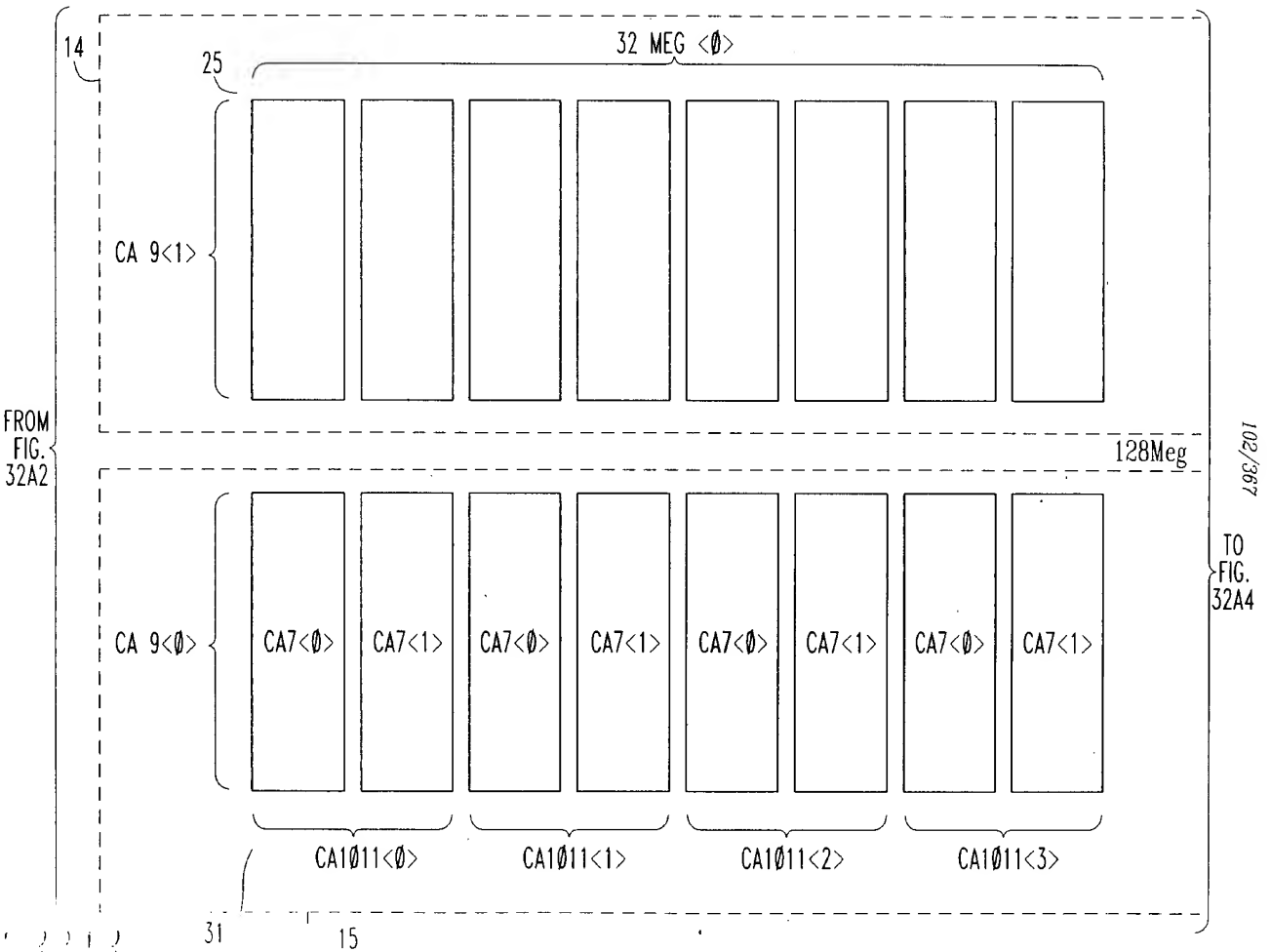

14
25
32 MEG <Ø>
CA 9<1>
FROM FIG. 32A2
128Meg
TO FIG. 32A4
CA 9<Ø>
CA7<Ø>
CA7<1>
CA7<Ø>
CA7<1>
CA7<Ø>
CA7<1>
CA7<Ø>
CA7<1>
CA1Ø11<Ø>
CA1Ø11<1>
CA1Ø11<2>
CA1Ø11<3>
31
15

FIG. 32A3

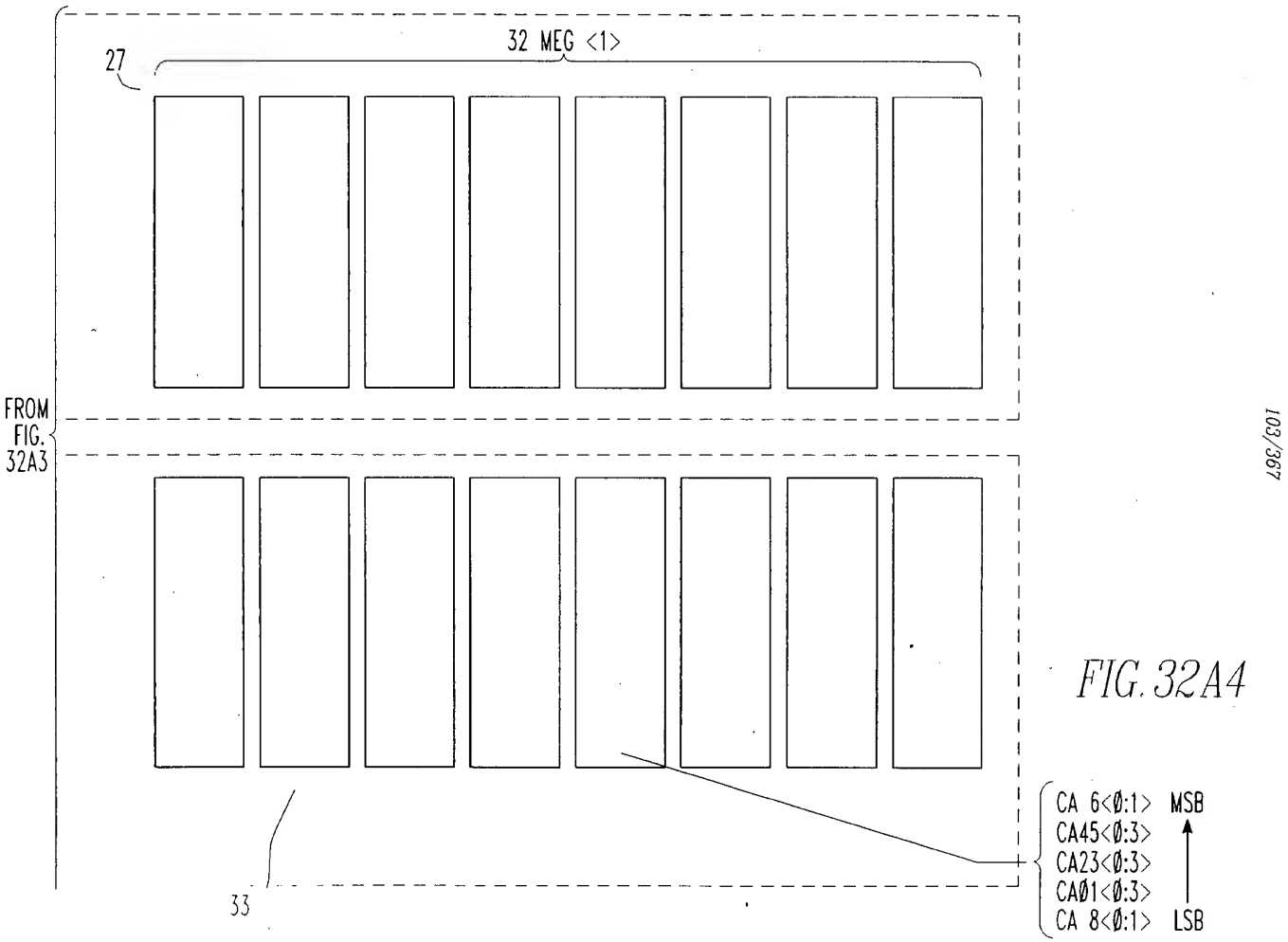

32 MEG <1>
27
FROM FIG. 32A3
33
CA 6<Ø:1> MSB
CA45<Ø:3>
CA23<Ø:3>
CAØ1<Ø:3>
CA 8<Ø:1> LSB

FIG. 32A4

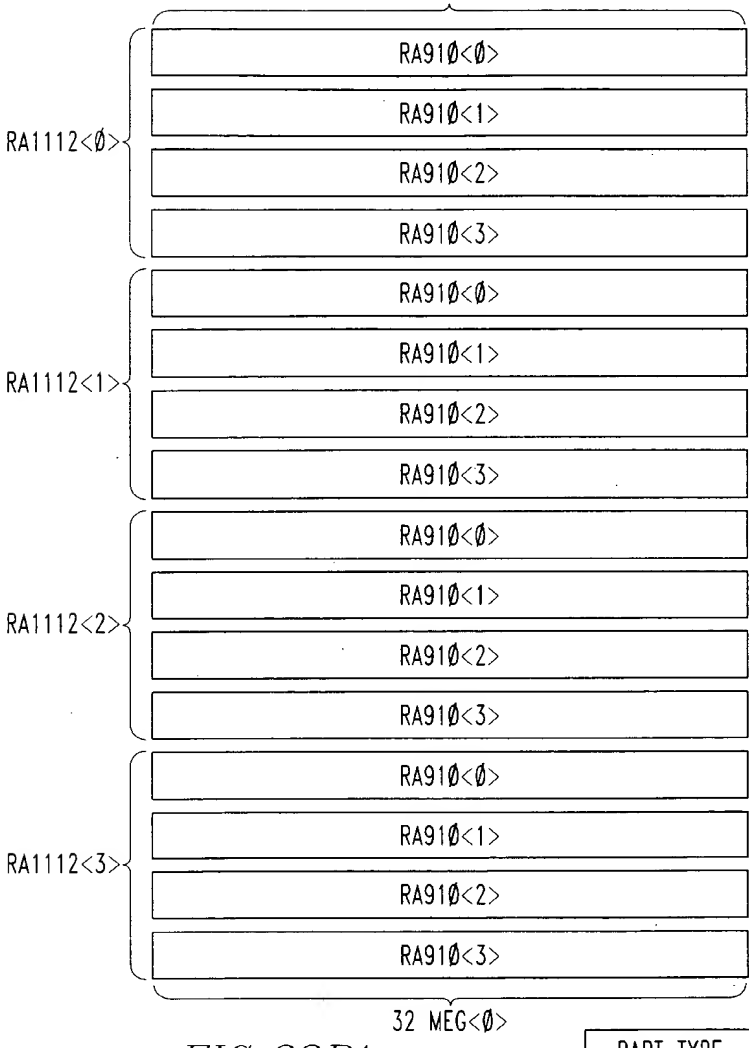


FIG. 32B1

PART TYPE	32MEG
ANY 16K	RA_13
X4 8K OR 4K	CA_12
X8 8K OR 4K	CA_11
X16 8K OR 4K	CA_10

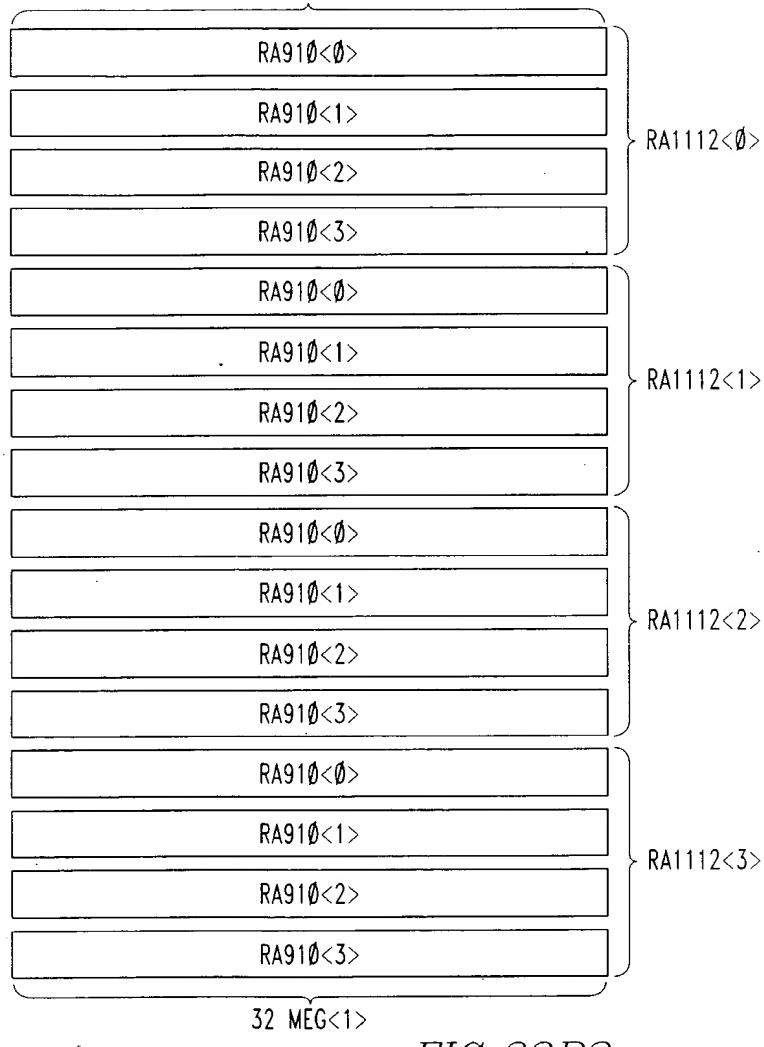

RA910<0>
RA910<1>
RA910<2>
RA910<3>
RA1112<0>
RA910<0>
RA910<1>
RA910<2>
RA910<3>
RA1112<1>
RA910<0>
RA910<1>
RA910<2>
RA910<3>
RA1112<2>
RA910<0>
RA910<1>
RA910<2>
RA910<3>
RA1112<3>
32 MEG<1>

FIG. 32B2

Tosoco Astoso

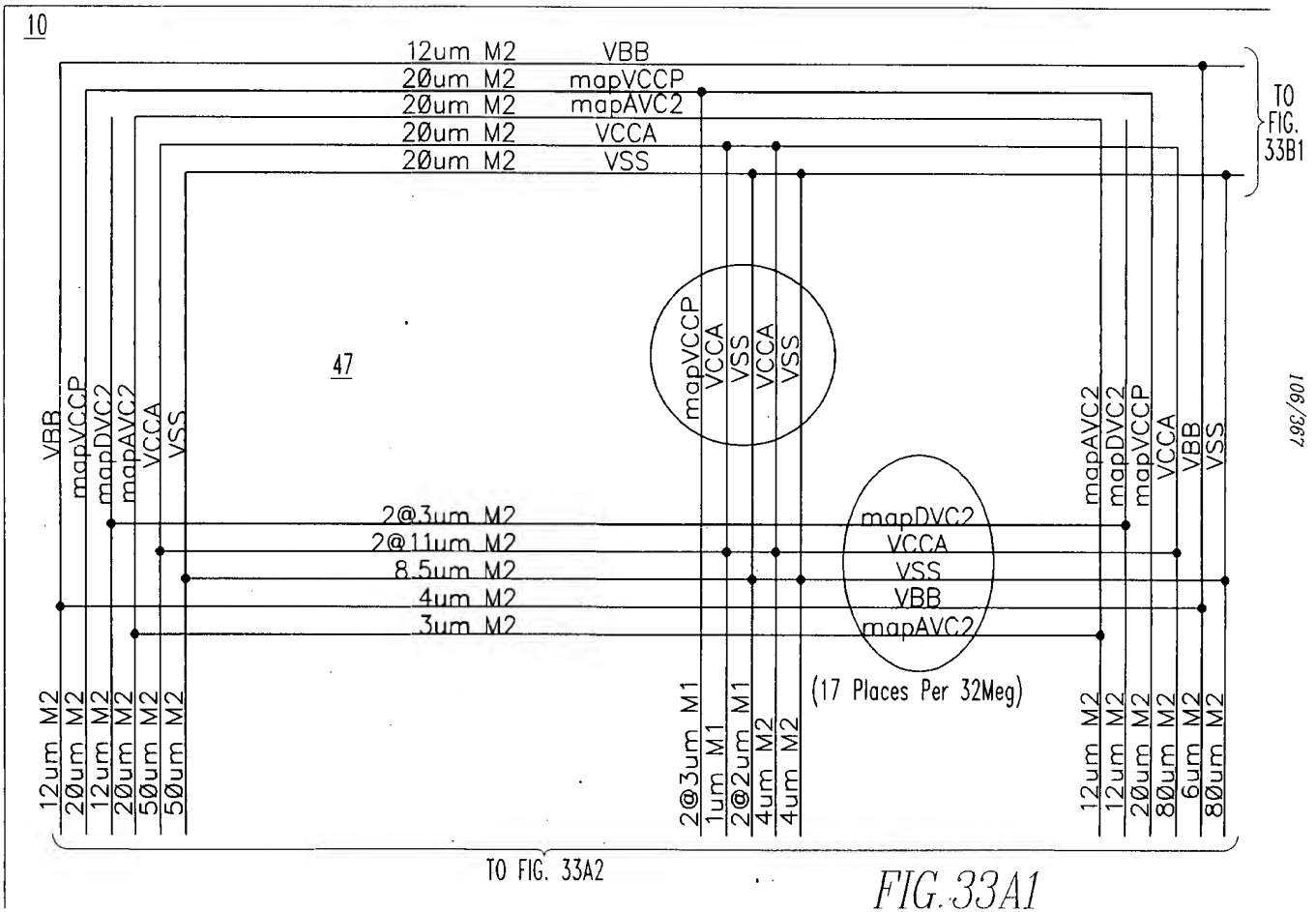


FIG. 33A1

FORGED" 8251686

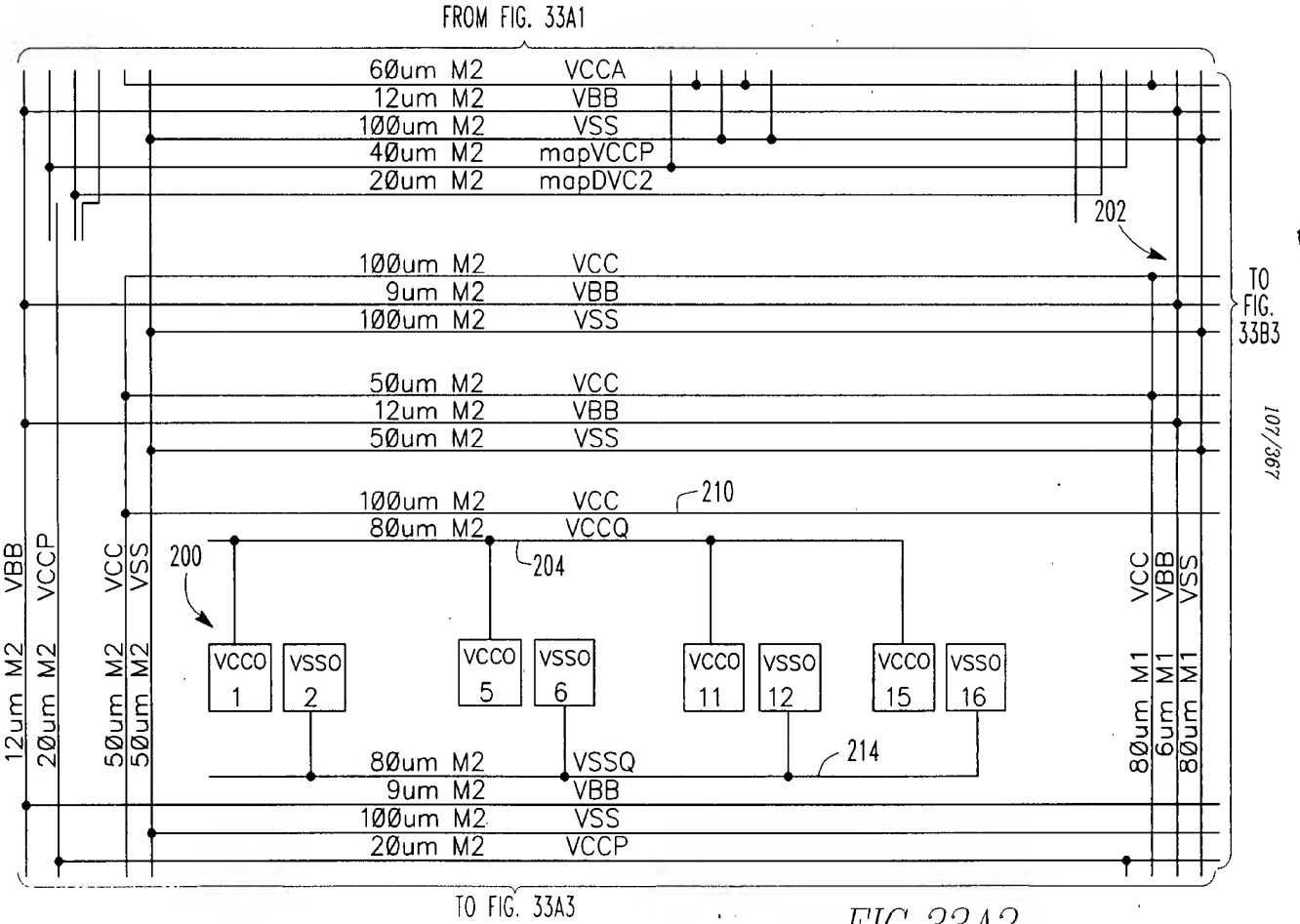


FIG. 33A2

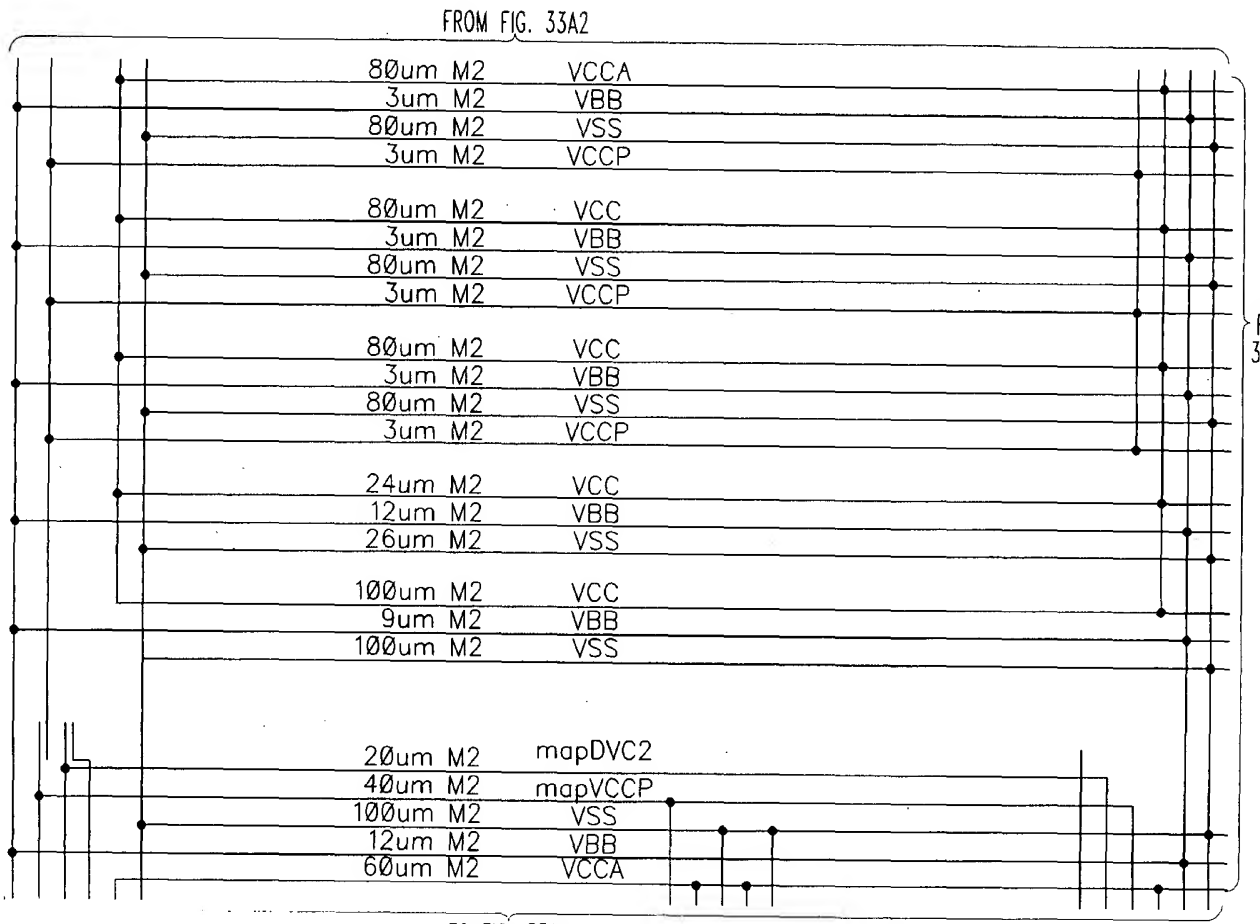

FROM FIG. 33A2
80um M2 VCCA
3um M2 VBB
80um M2 VSS
3um M2 VCCP
80um M2 VCC
3um M2 VBB
80um M2 VSS
3um M2 VCCP
80um M2 VCC
3um M2 VBB
80um M2 VSS
3um M2 VCCP
24um M2 VCC
12um M2 VBB
26um M2 VSS
100um M2 VCC
9um M2 VBB
100um M2 VSS
20um M2 mapDVC2
40um M2 mapVCCP
100um M2 VSS
12um M2 VBB
60um M2 VCCA
TO FIG. 33A4
TO FIG. 33B5

FIG. 33A3

FOUND ARCHIVED

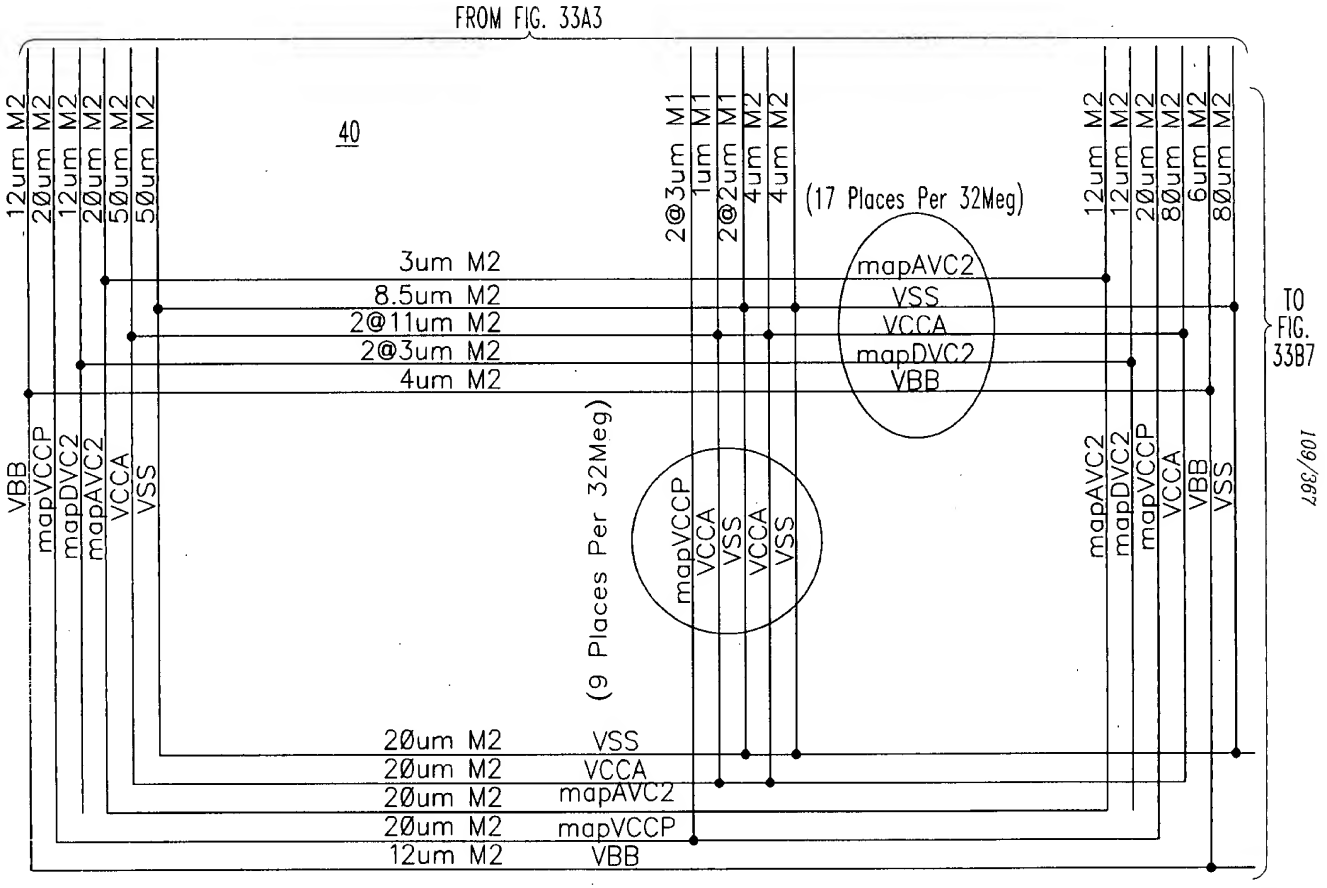


FIG. 33A4

Tossed: 6857860

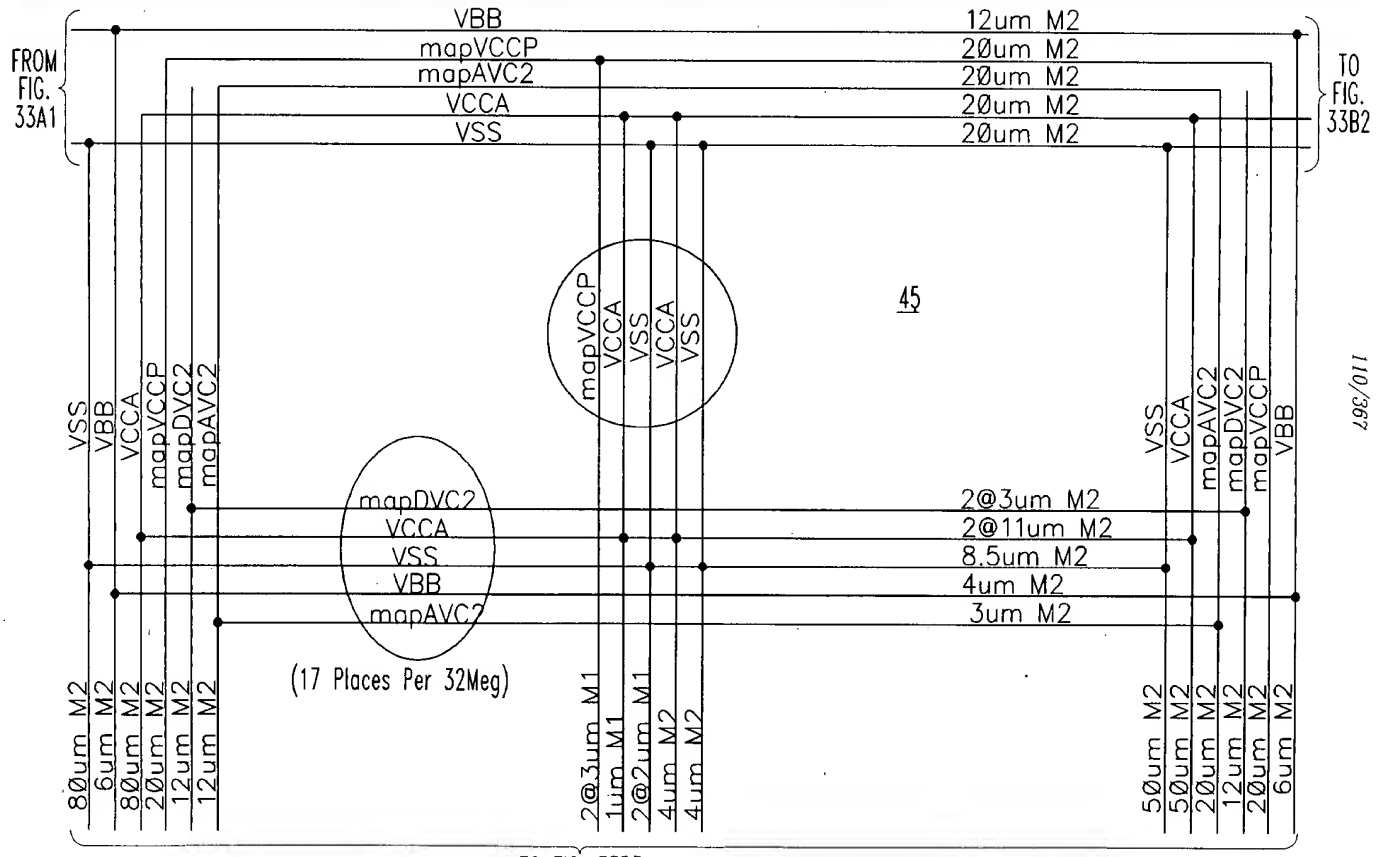


FIG. 33B1

110/367

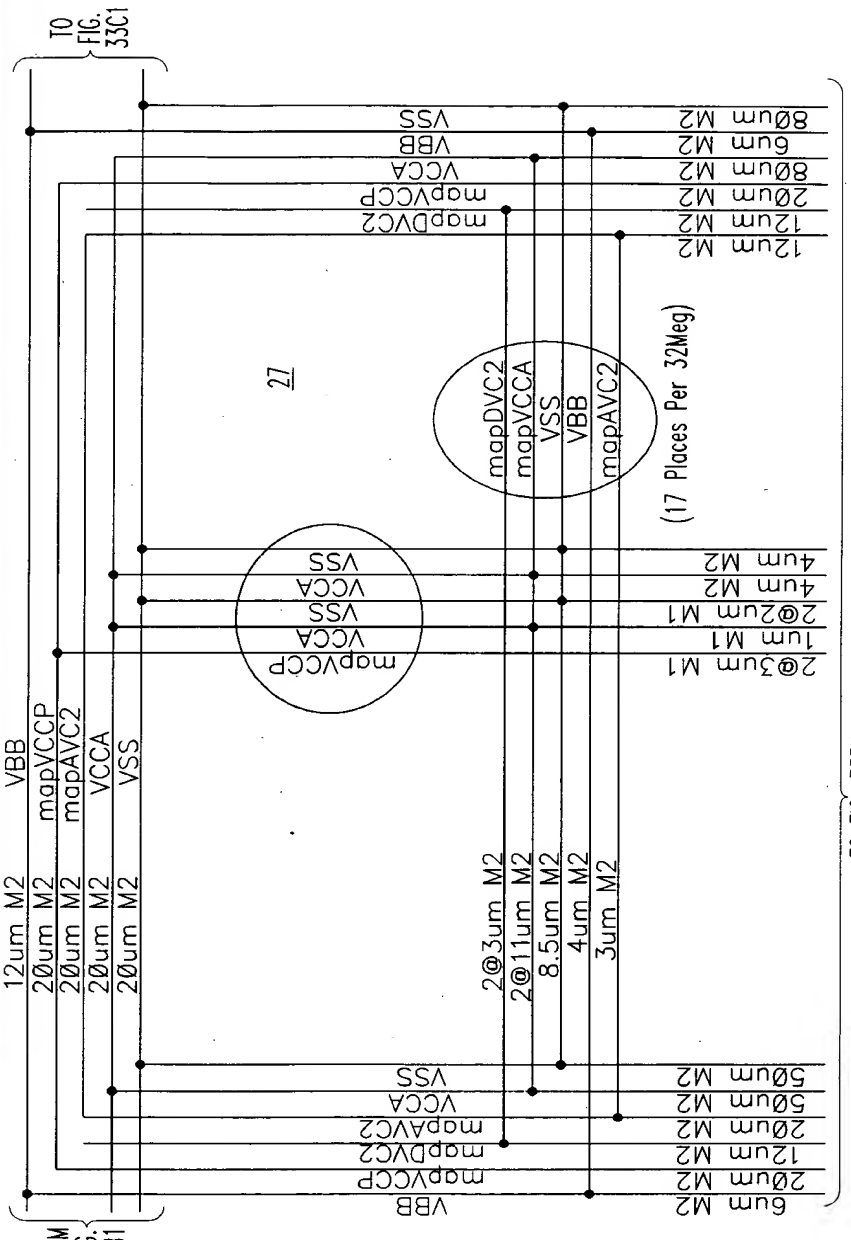

FROM FIG. 33B1
12um M2 VBB
20um M2 mapVCCP
20um M2 mapAVC2
20um M2 VCCA
20um M2 VSS
TO FIG. 33C1
TO FIG. 33B4
6um M2
20um M2
12um M2
50um M2
50um M2
20um M2
80um M2
6um M2
80um M2
2@3um M2
2@11um M2
8.5um M2
4um M2
3um M2
VBB mapVCCP mapDVC2 mapAVC2 VCCA VSS
mapVCCP VCCA VSS VCCA VSS
mapDVC2 mapVCCP VCCA VBB VSS
(17 Places Per 32Meg)
2@3um M1
1um M1
2@2um M1
4um M2
4um M2
12um M2
12um M2
20um M2
80um M2
6um M2
80um M2
27

FIG. 33B2

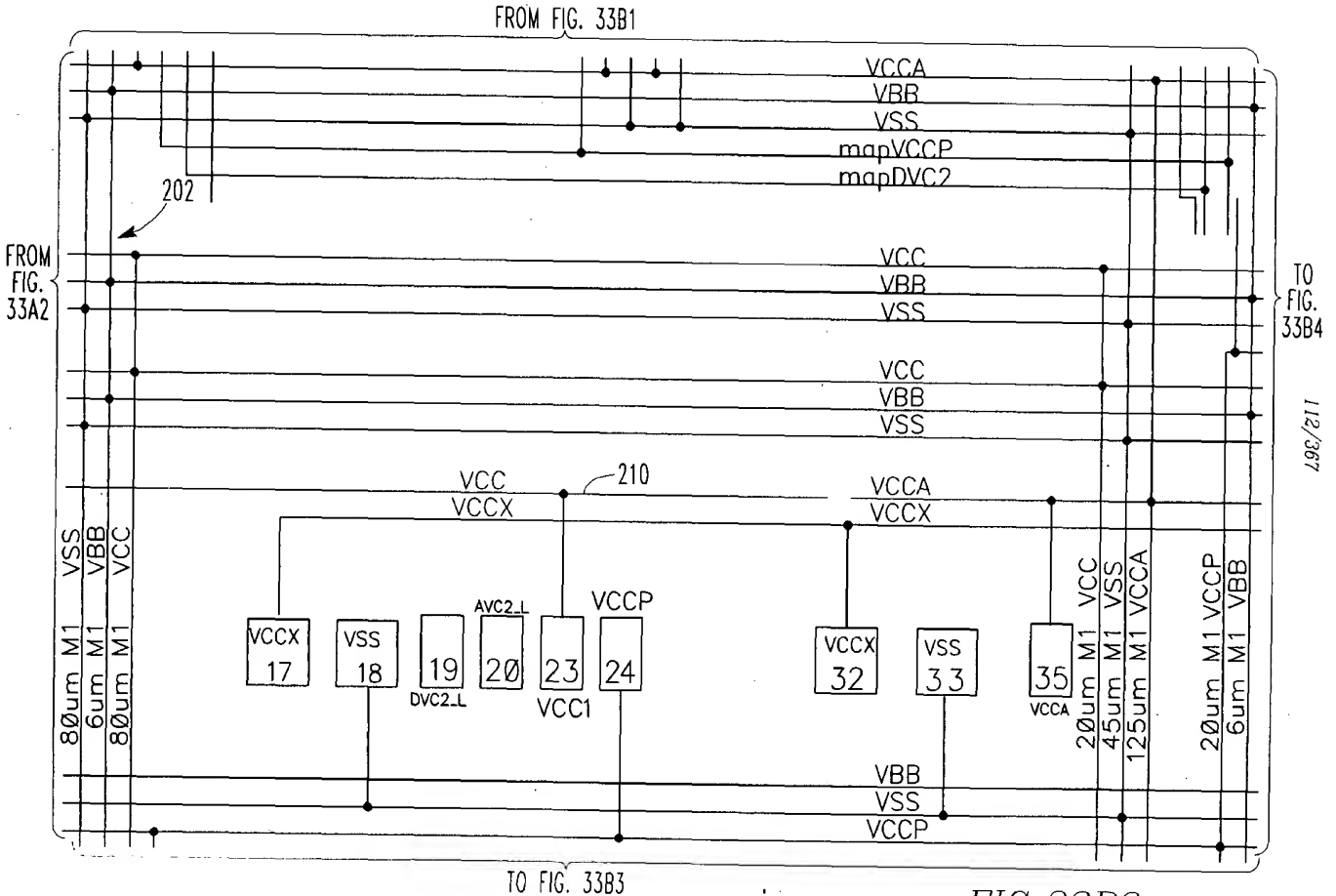

FROM FIG. 33B1
VCCA
VBB
VSS
mapVCCP
mapDVC2
202
FROM FIG. 33A2
VCC
VBB
VSS
VCC
VBB
VSS
TO FIG. 33B4
VCC
VCCX
210
VCCA
VCCX
VSS
VBB
VCC
80um M1
6um M1
80um M1
VCCX 17
VSS 18
19 DVC2_L
AVC2_L 20
23 VCC1
VCCP 24
VCCX 32
VSS 33
35 VCCA
20um M1 VCC
45um M1 VSS
125um M1 VCCA
20um M1 VCCP
6um M1 VBB
VBB
VSS
VCCP
TO FIG. 33B3

FIG. 33B3

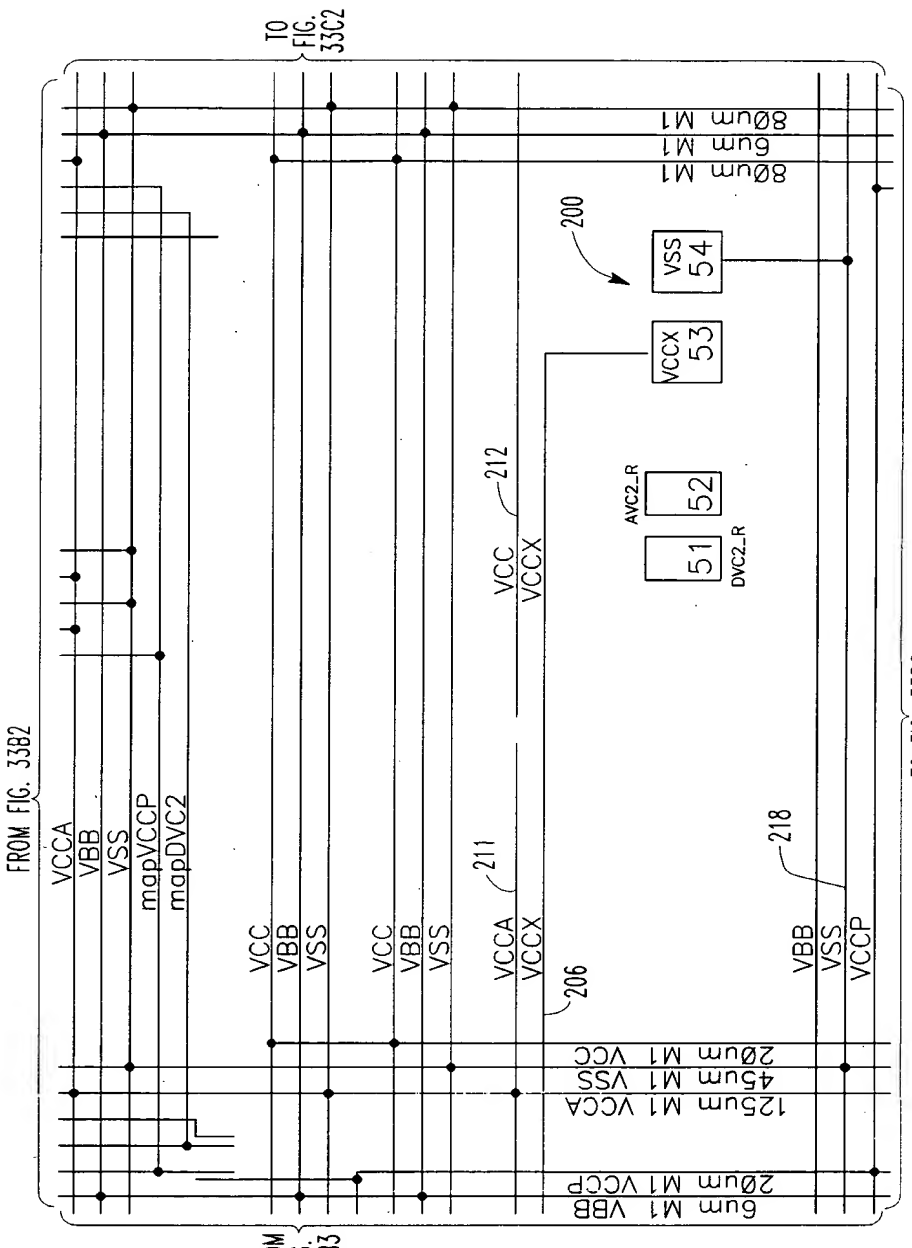

FROM FIG. 33B2
VCCA
VBB
VSS
mapVCCP
mapDVC2
TO FIG. 33C2
VCC
VBB
VSS
VCC
VBB
VSS
VCCA
VCCX
211
212
206
218
200
VCCX 53
VSS 54
AVC2_R
DVC2_R
51
52
VCC
VCCX
VBB
VSS
VCCP
80um M1
60um M1
80um M1
6um M1 VBB
20um M1 VCCP
125um M1 VCCA
45um M1 VSS
20um M1 VCC
FROM FIG. 33B3
TO FIG. 33B6

FIG. 33B4

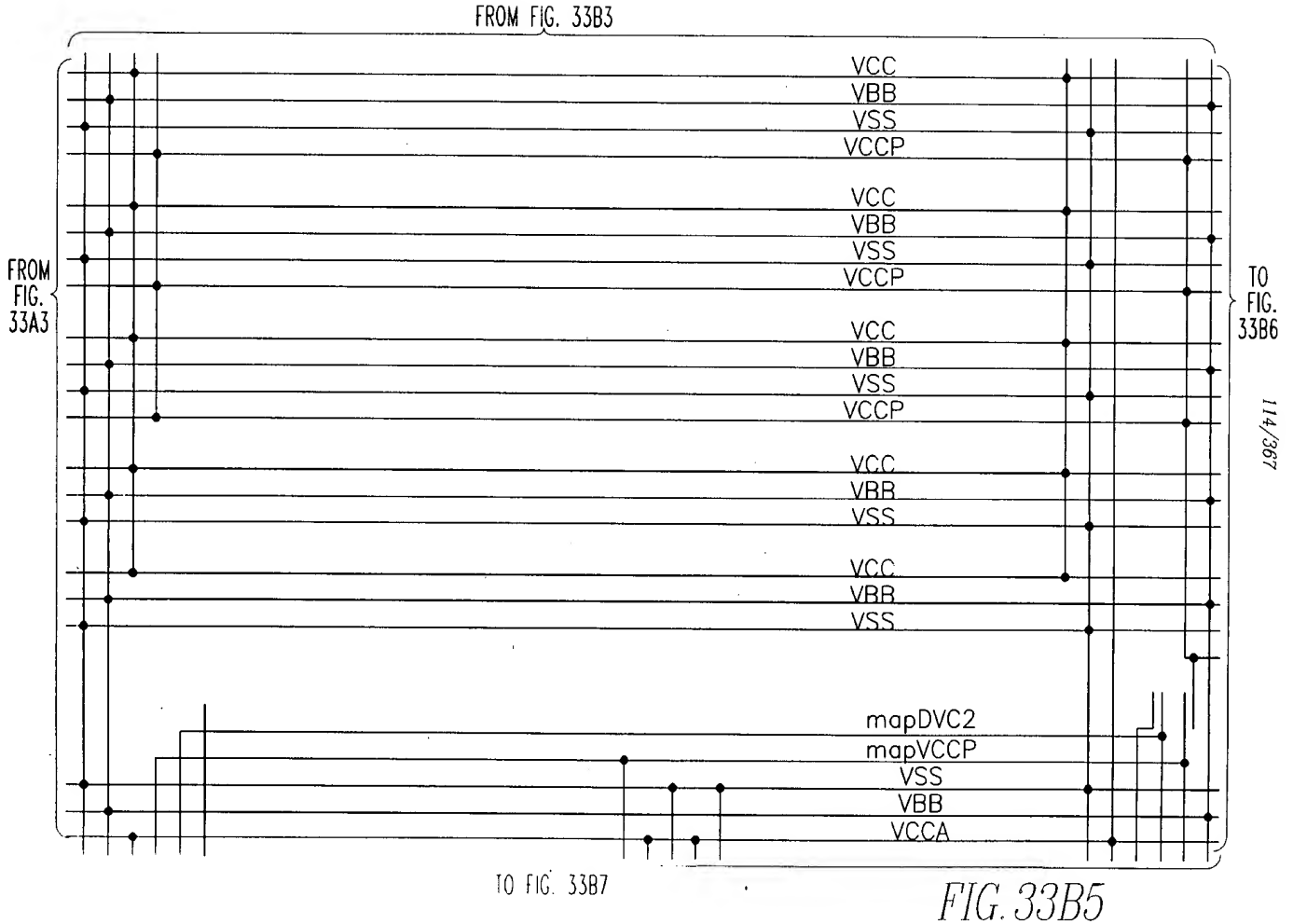

FROM FIG. 33B3
FROM FIG. 33A3
TO FIG. 33B6
TO FIG. 33B7
VCC
VBB
VSS
VCCP
VCC
VBB
VSS
VCCP
VCC
VBB
VSS
VCCP
VCC
VBB
VSS
VCC
VBB
VSS
mapDVC2
mapVCCP
VSS
VBB
VCCA

FIG. 33B5

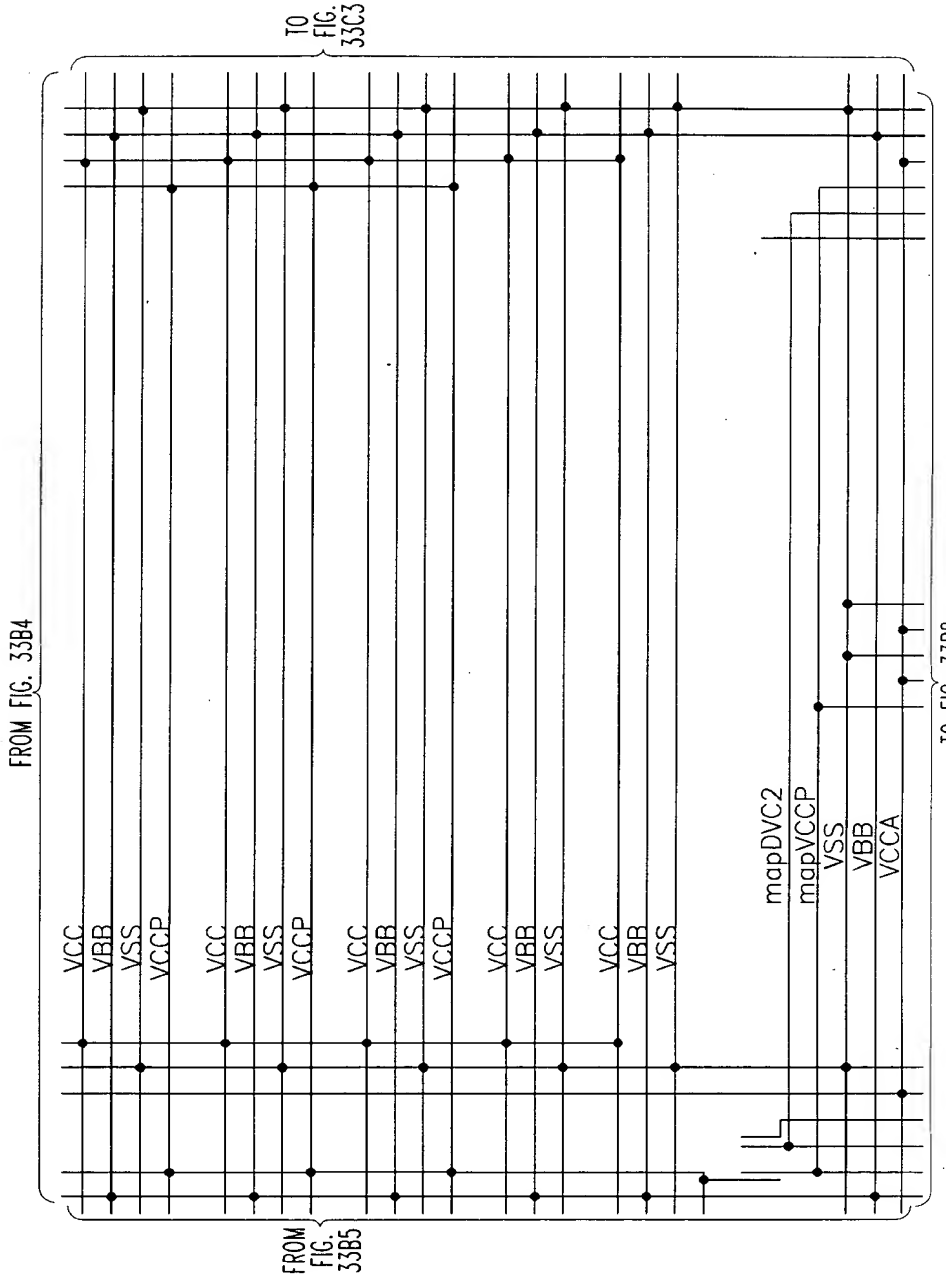

FROM FIG. 33B4
FROM FIG. 33B5
TO FIG. 33C3
TO FIG. 33B8
VCC
VBB
VSS
VCCP
mapDVC2
mapVCCP
VSS
VBB
VCCA

FIG. 33B6

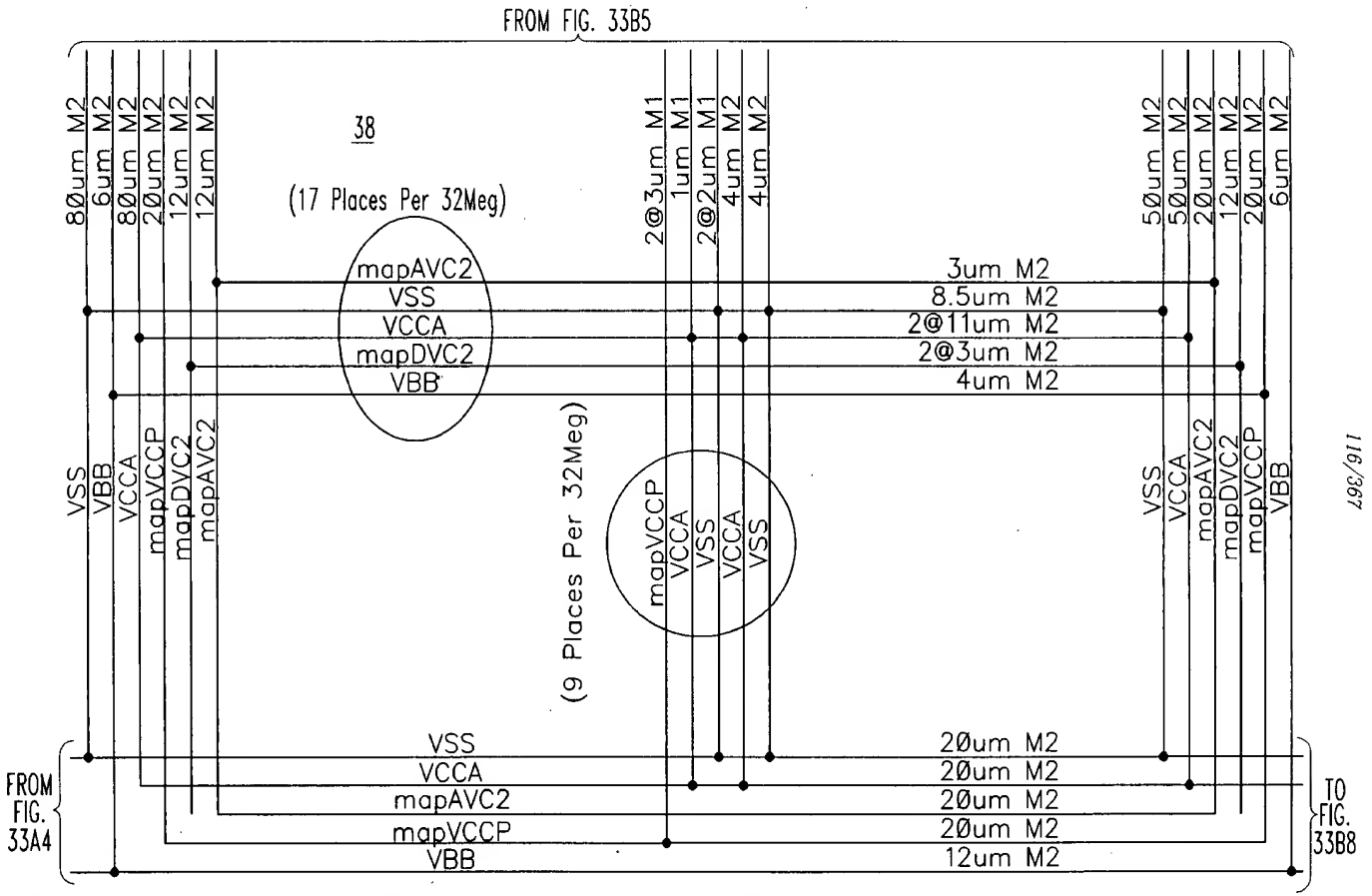

FROM FIG. 33B5
38
(17 Places Per 32Meg)
(9 Places Per 32Meg)
80um M2
6um M2
80um M2
20um M2
12um M2
12um M2
2@3um M1
1um M1
2@2um M1
4um M2
4um M2
50um M2
50um M2
20um M2
12um M2
20um M2
6um M2
mapAVC2
VSS
VCCA
mapDVC2
VBB
3um M2
8.5um M2
2@11um M2
2@3um M2
4um M2
VSS
VBB
VCCA
mapVCCP
mapDVC2
mapAVC2
mapVCCP
VCCA
VSS
VCCA
VSS
VSS
VCCA
mapAVC2
mapDVC2
mapVCCP
VBB
FROM FIG. 33A4
VSS
VCCA
mapAVC2
mapVCCP
VBB
20um M2
20um M2
20um M2
20um M2
12um M2
TO FIG. 33B8

FIG. 33B7

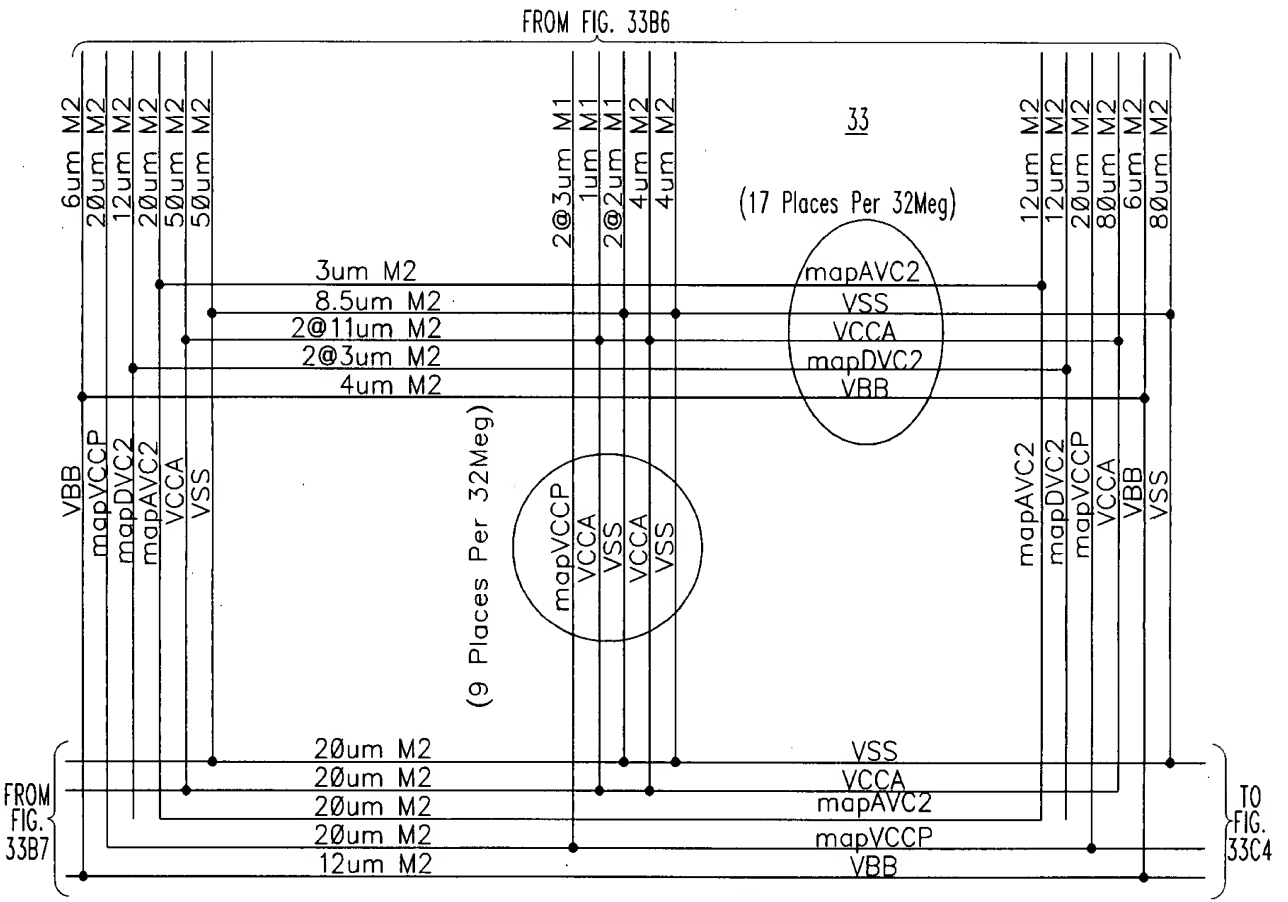

FROM FIG. 33B6
6um M2
20um M2
12um M2
20um M2
50um M2
50um M2
2@3um M1
1um M1
2@2um M1
4um M2
4um M2
33
(17 Places Per 32Meg)
12um M2
12um M2
20um M2
80um M2
6um M2
80um M2
3um M2
8.5um M2
2@11um M2
2@3um M2
4um M2
mapAVC2
VSS
VCCA
mapDVC2
VBB
VBB
mapVCCP
mapDVC2
mapAVC2
VCCA
VSS
(9 Places Per 32Meg)
mapVCCP
VCCA
VSS
VCCA
VSS
mapAVC2
mapDVC2
mapVCCP
VCCA
VBB
VSS
FROM FIG. 33B7
20um M2
20um M2
20um M2
20um M2
12um M2
VSS
VCCA
mapAVC2
mapVCCP
VBB
TO FIG. 33C4

FIG. 33B8

Tosca 99TC868

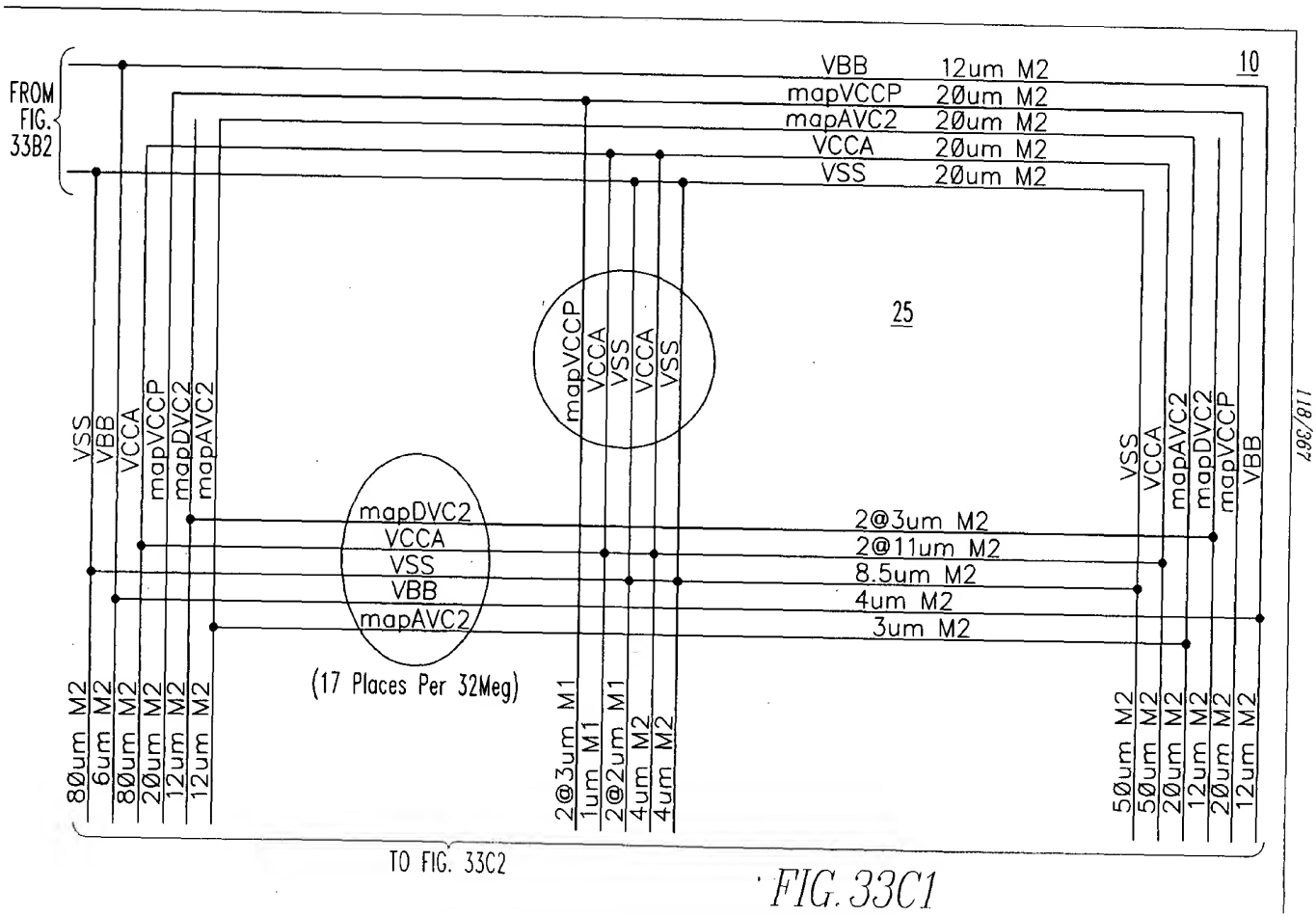


FIG. 33C1

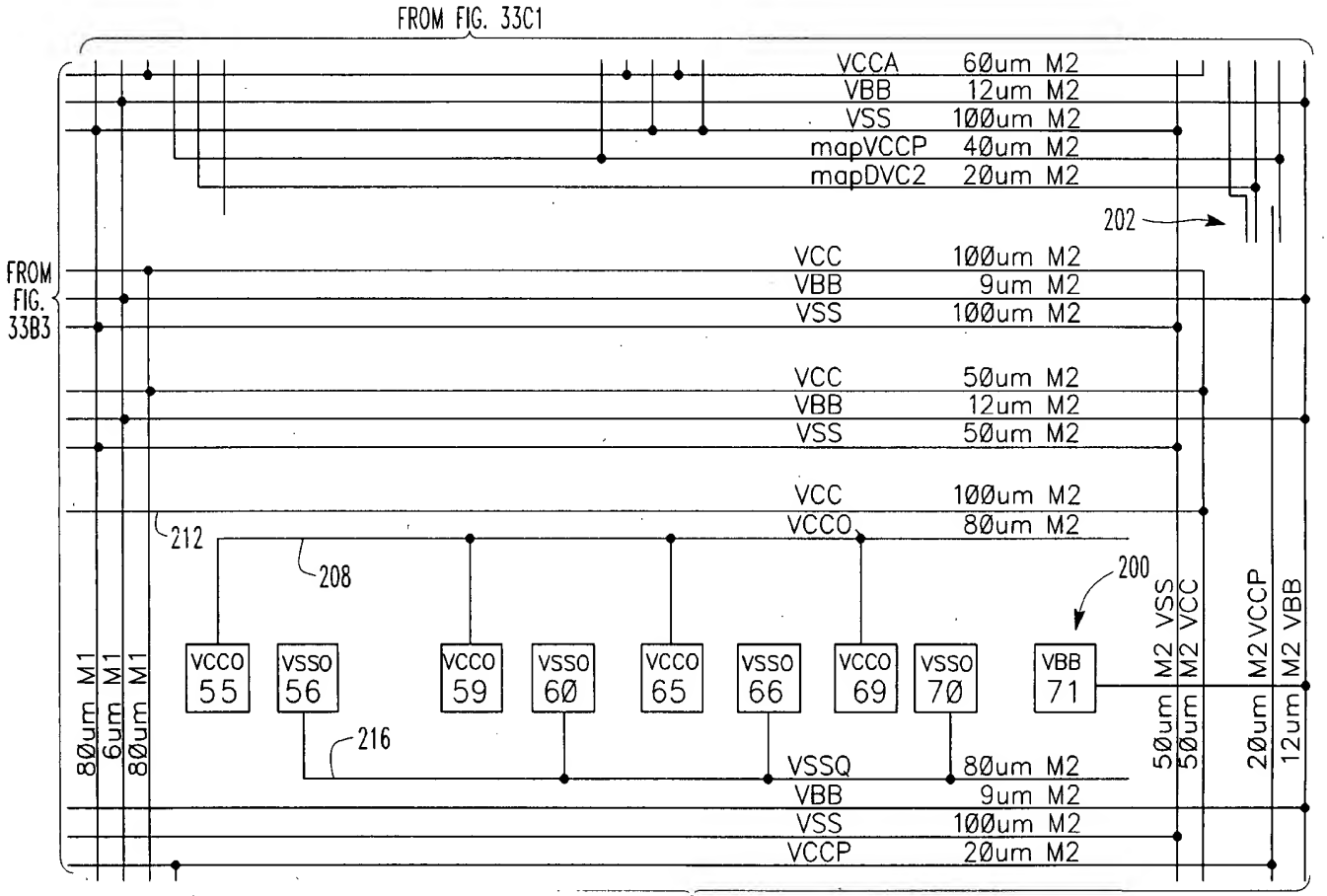

FROM FIG. 33C1
VCCA 60um M2
VBB 12um M2
VSS 100um M2
mapVCCP 40um M2
mapDVC2 20um M2
202
FROM FIG. 33B3
VCC 100um M2
VBB 9um M2
VSS 100um M2
VCC 50um M2
VBB 12um M2
VSS 50um M2
VCC 100um M2
VCCO 80um M2
212
208
200
VCCO 55
VSSO 56
VCCO 59
VSSO 60
VCCO 65
VSSO 66
VCCO 69
VSSO 70
VBB 71
216
VSSQ 80um M2
VBB 9um M2
VSS 100um M2
VCCP 20um M2
80um M1
6um M1
80um M1
50um M2 VSS
50um M2 VCC
20um M2 VCCP
12um M2 VBB
TO FIG. 33C3

FIG. 33C2

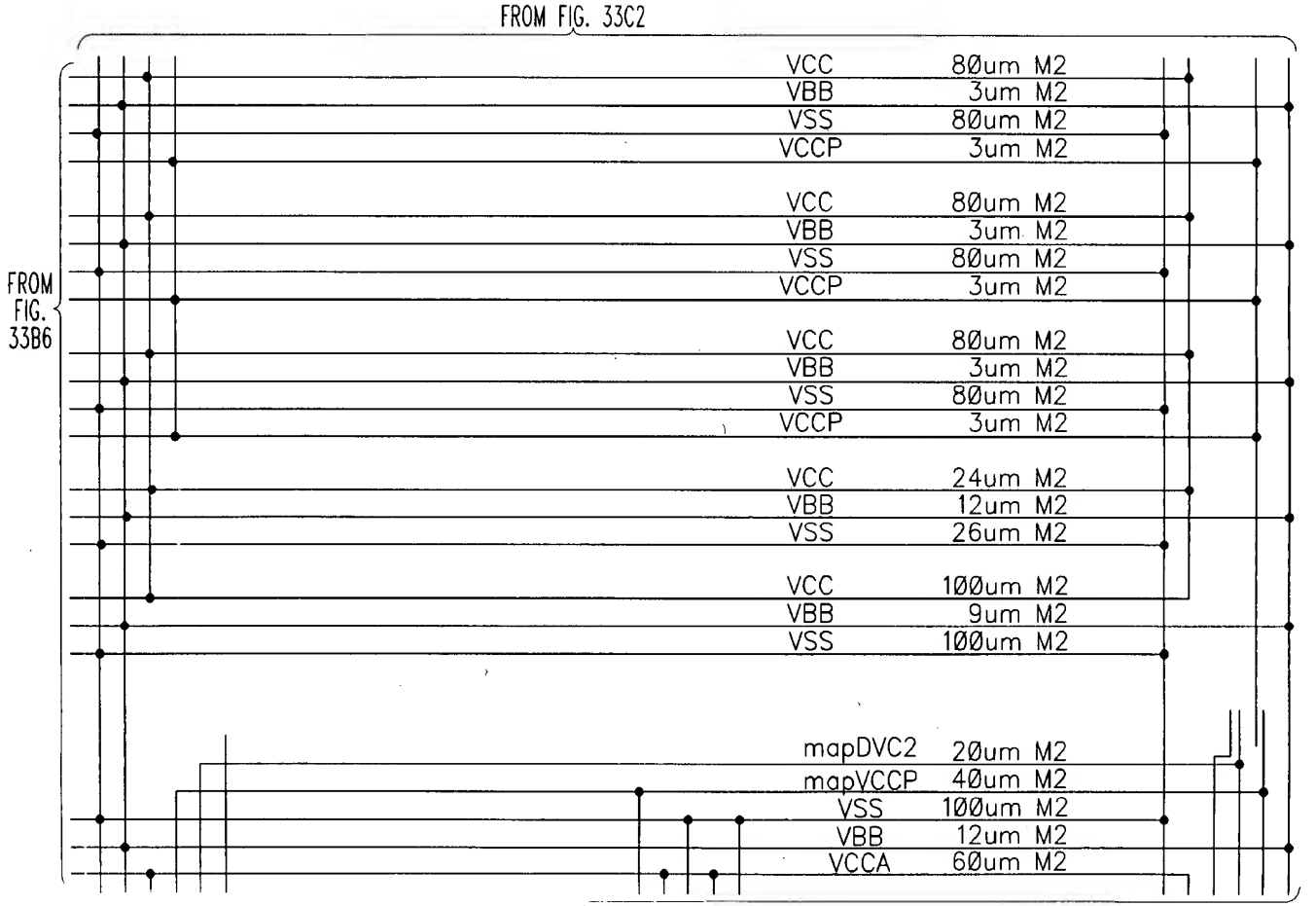

FROM FIG. 33C2
FROM FIG. 33B6
VCC 80um M2
VBB 3um M2
VSS 80um M2
VCCP 3um M2
VCC 80um M2
VBB 3um M2
VSS 80um M2
VCCP 3um M2
VCC 80um M2
VBB 3um M2
VSS 80um M2
VCCP 3um M2
VCC 24um M2
VBB 12um M2
VSS 26um M2
VCC 100um M2
VBB 9um M2
VSS 100um M2
mapDVC2 20um M2
mapVCCP 40um M2
VSS 100um M2
VBB 12um M2
VCCA 60um M2
TO FIG. 33C4

FIG. 33C3

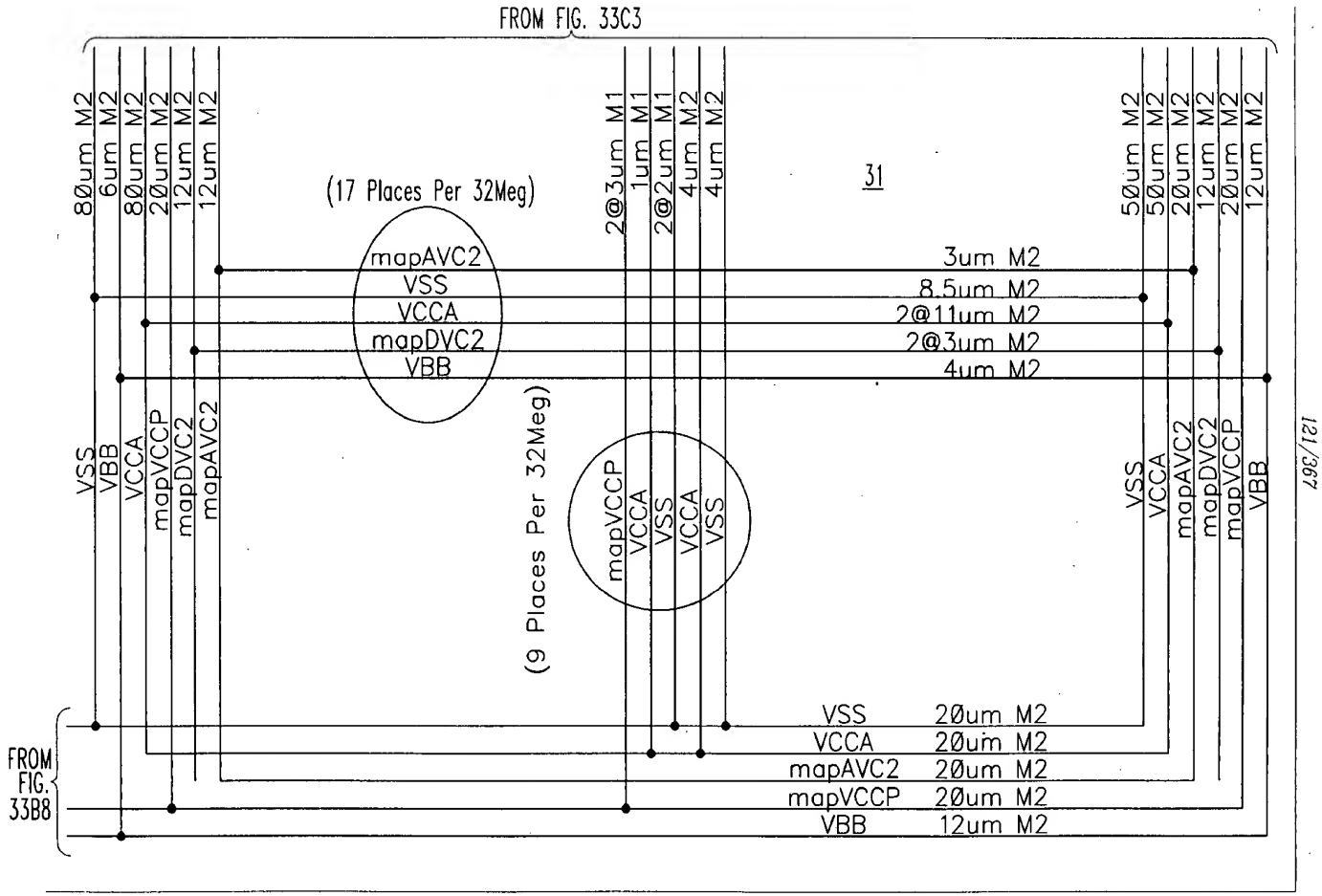

FROM FIG. 33C3
80um M2
6um M2
80um M2
20um M2
12um M2
12um M2
(17 Places Per 32Meg)
mapAVC2
VSS
VCCA
mapDVC2
VBB
2@3um M1
1um M1
2@2um M1
4um M2
4um M2
31
50um M2
50um M2
20um M2
12um M2
20um M2
12um M2
3um M2
8.5um M2
2@11um M2
2@3um M2
4um M2
VSS
VBB
VCCA
mapVCCP
mapDVC2
mapAVC2
(9 Places Per 32Meg)
mapVCCP
VCCA
VSS
VCCA
VSS
VSS
VCCA
mapAVC2
mapDVC2
mapVCCP
VBB
FROM FIG. 33B8
VSS 20um M2
VCCA 20um M2
mapAVC2 20um M2
mapVCCP 20um M2
VBB 12um M2

FIG. 33C4

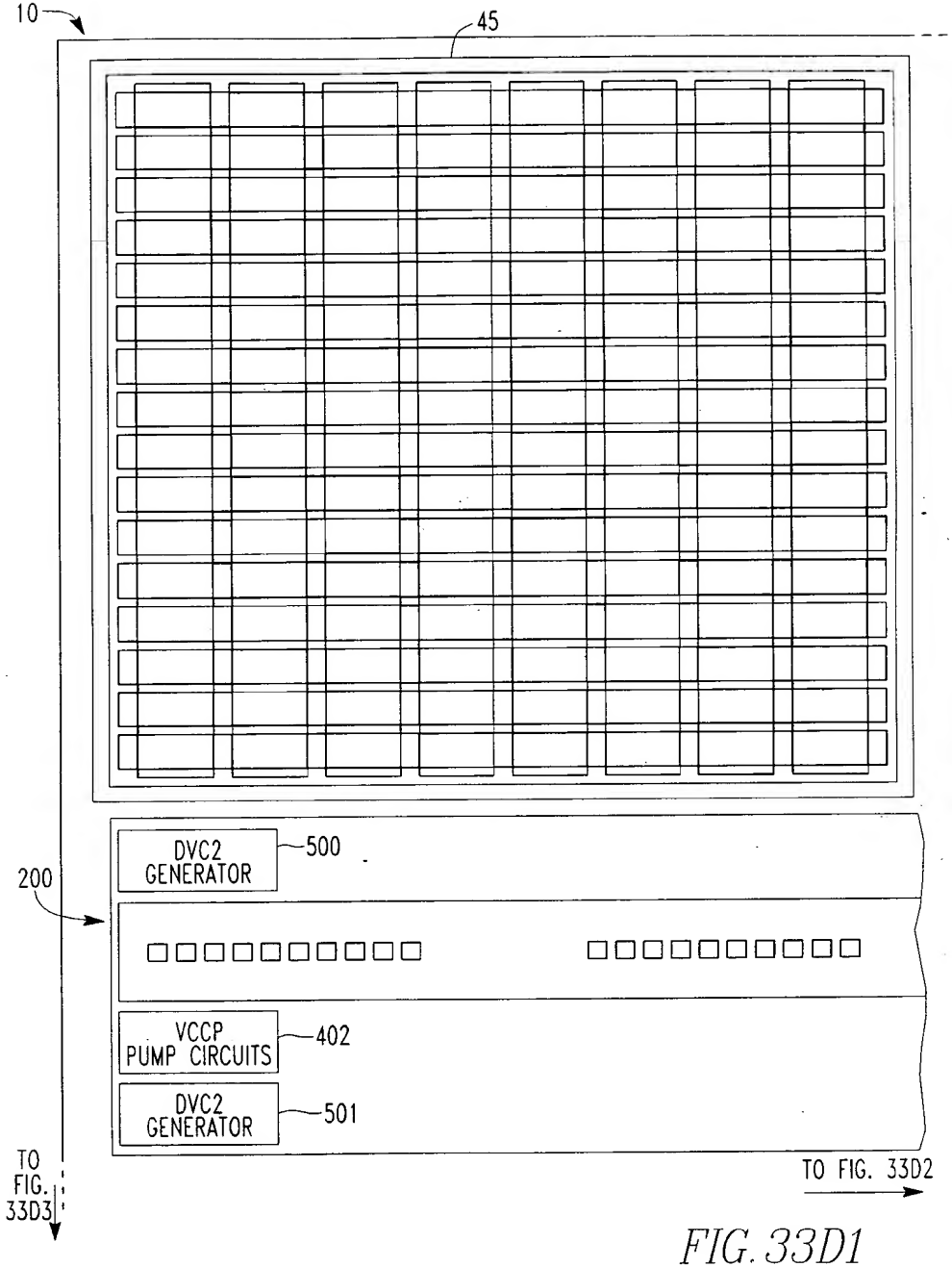

10
45
200
DVC2 GENERATOR
500
VCCP PUMP CIRCUITS
402
DVC2 GENERATOR
501
TO FIG. 33D3
TO FIG. 33D2

FIG. 33D1

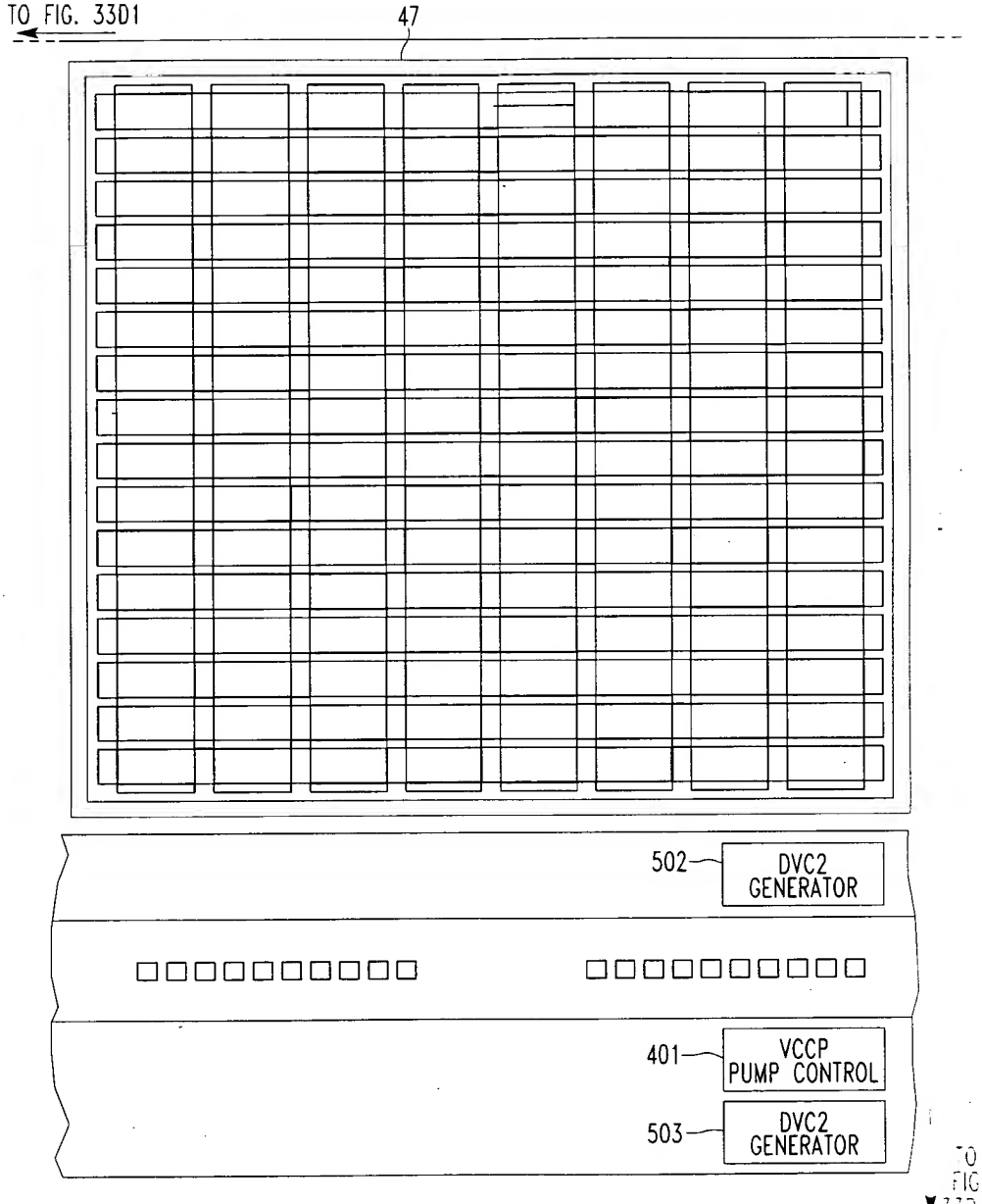

TO FIG. 33D1
47
502
DVC2 GENERATOR
401
VCCP PUMP CONTROL
503
DVC2 GENERATOR
TO FIG. 33D4

FIG. 33D2

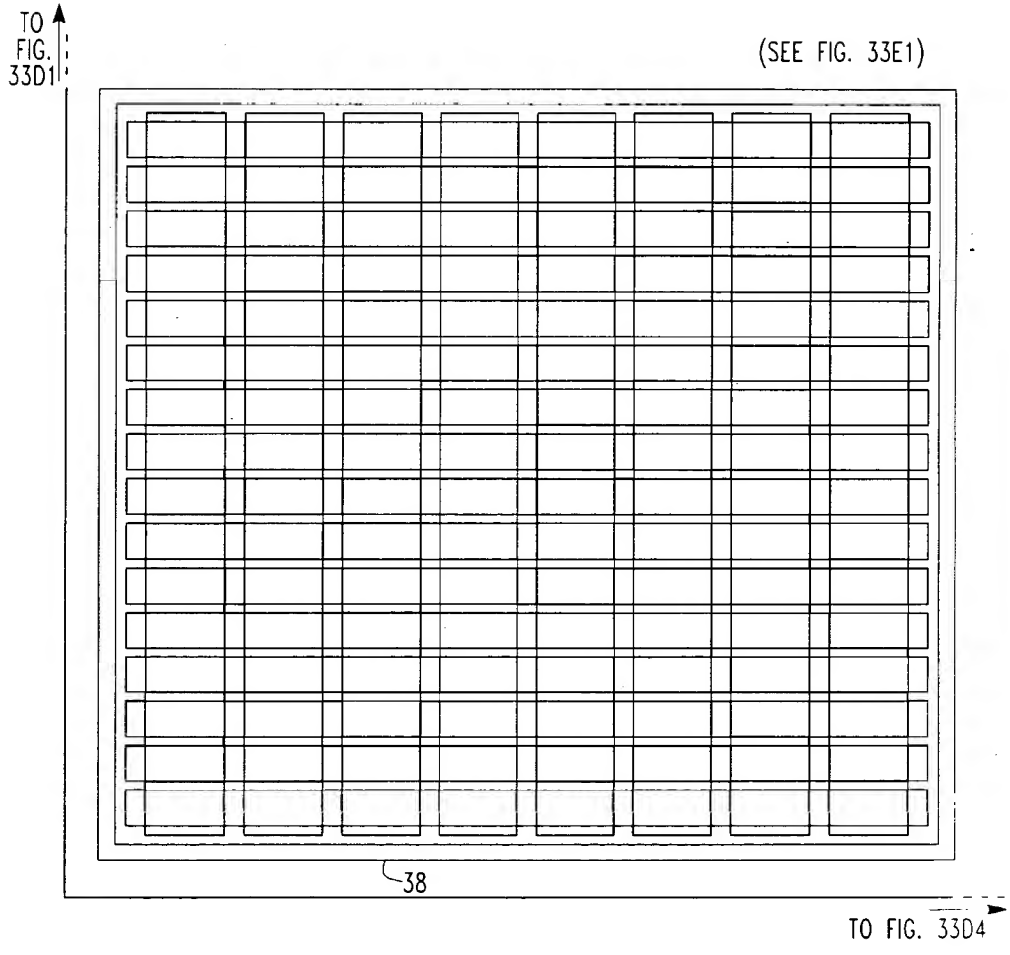


FIG. 33D3

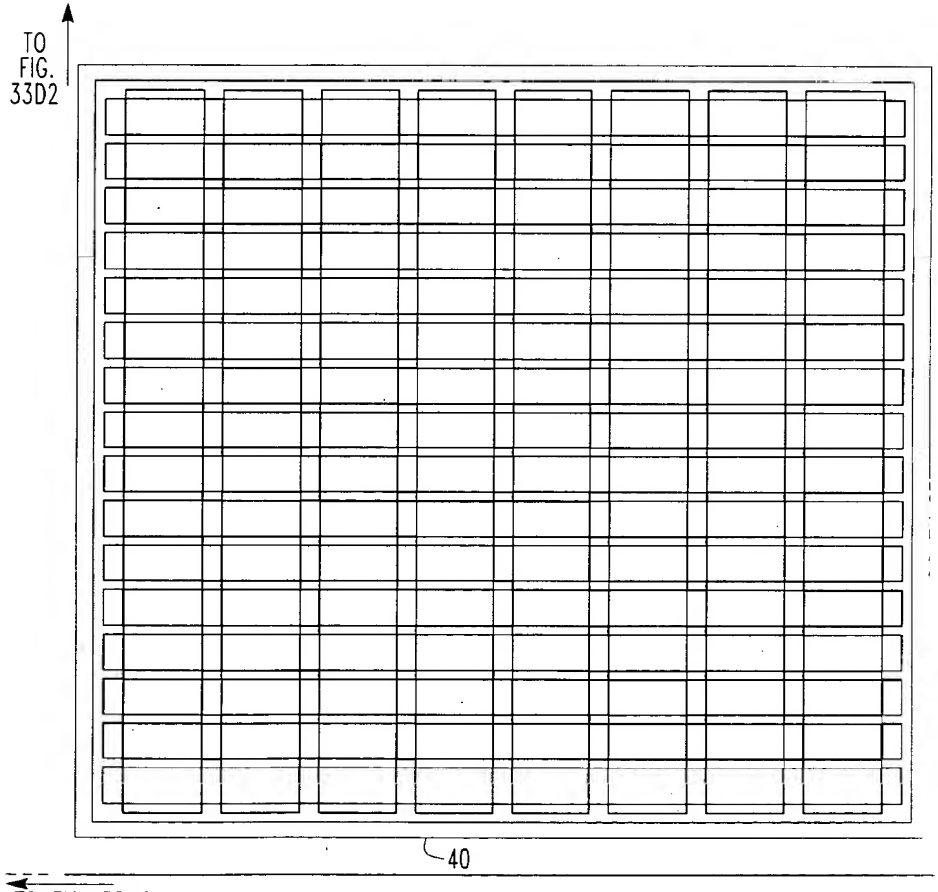


FIG. 33D4

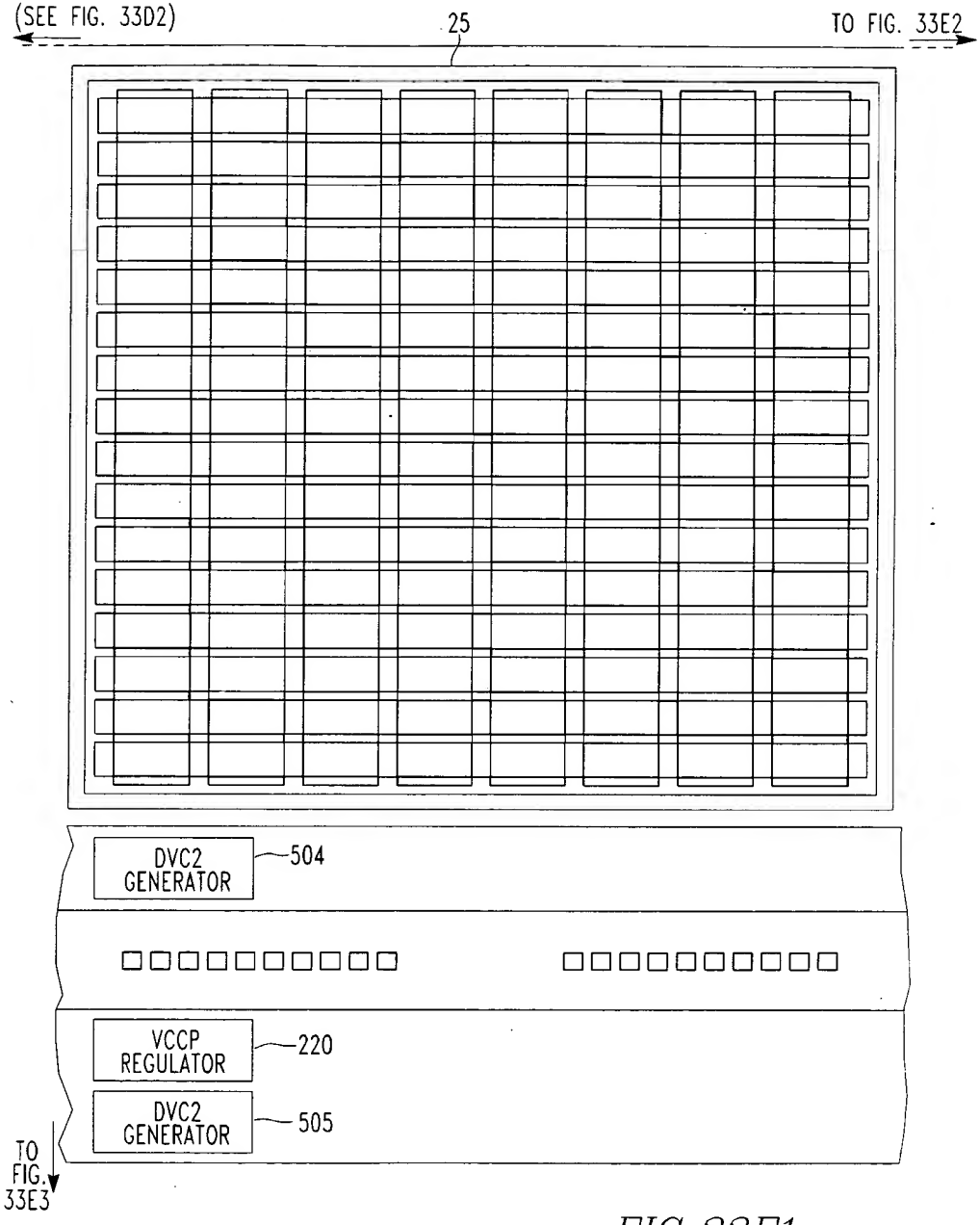

(SEE FIG. 33D2)
25
TO FIG. 33E2
DVC2 GENERATOR
504
VCCP REGULATOR
220
DVC2 GENERATOR
505
TO FIG. 33E3

FIG. 33E1

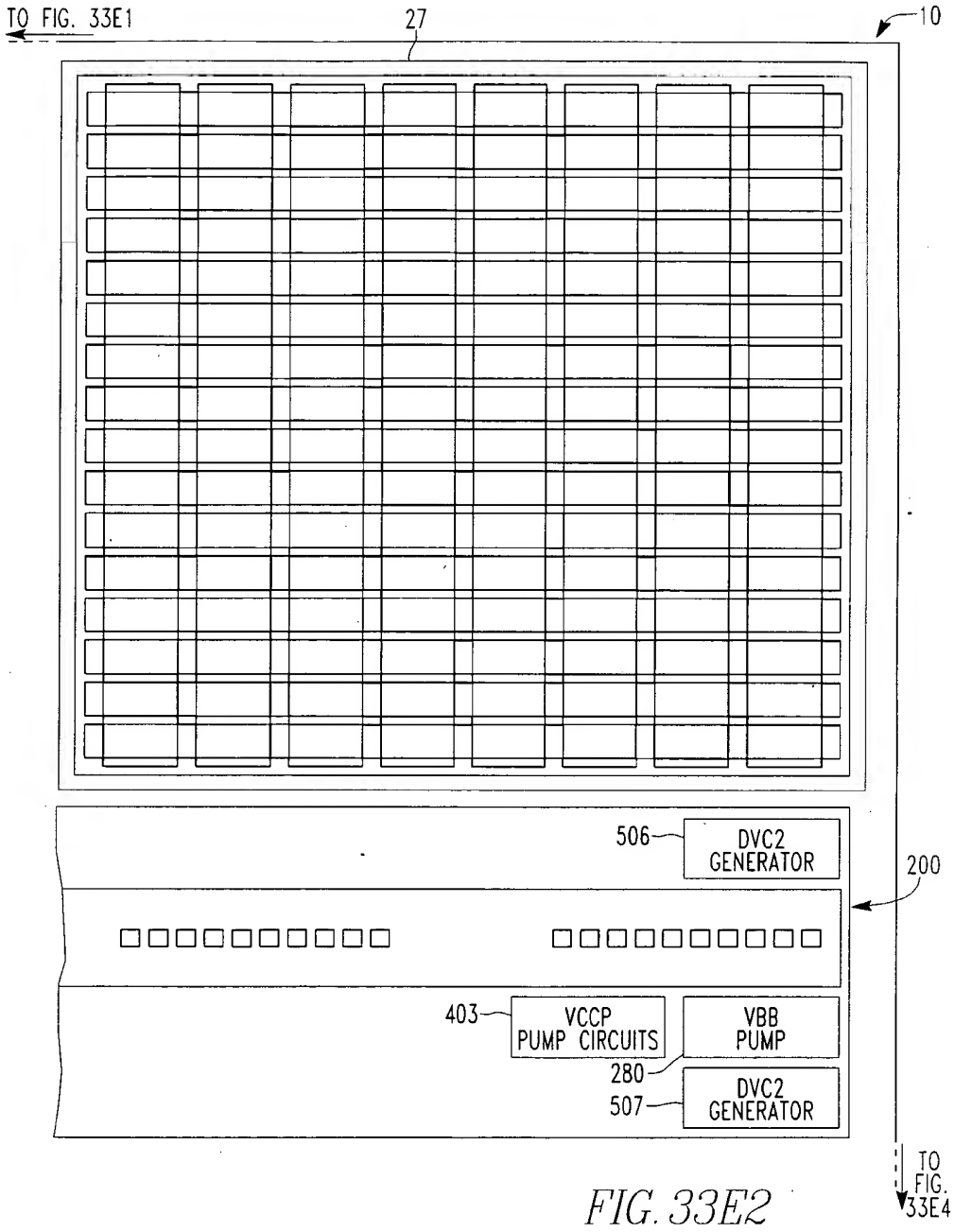

TO FIG. 33E1
27
10
506
DVC2 GENERATOR
200
403
VCCP PUMP CIRCUITS
VBB PUMP
280
507
DVC2 GENERATOR
TO FIG. 33E4

FIG. 33E2

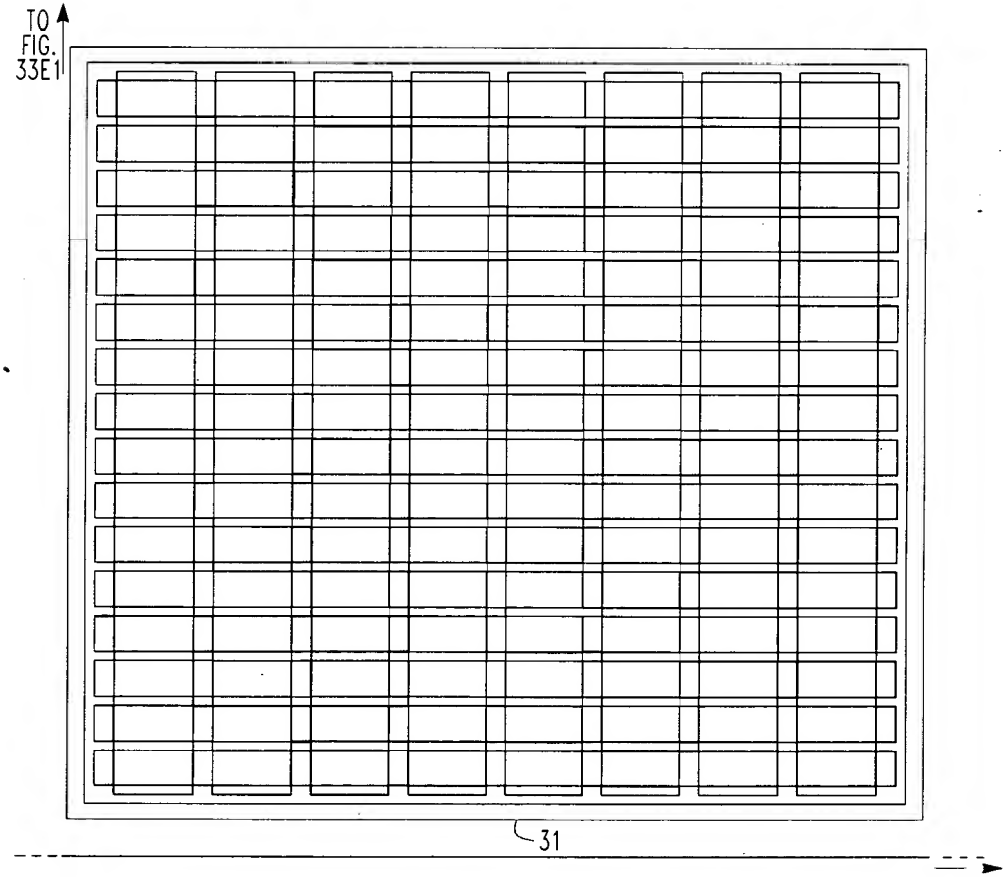


FIG. 33E3

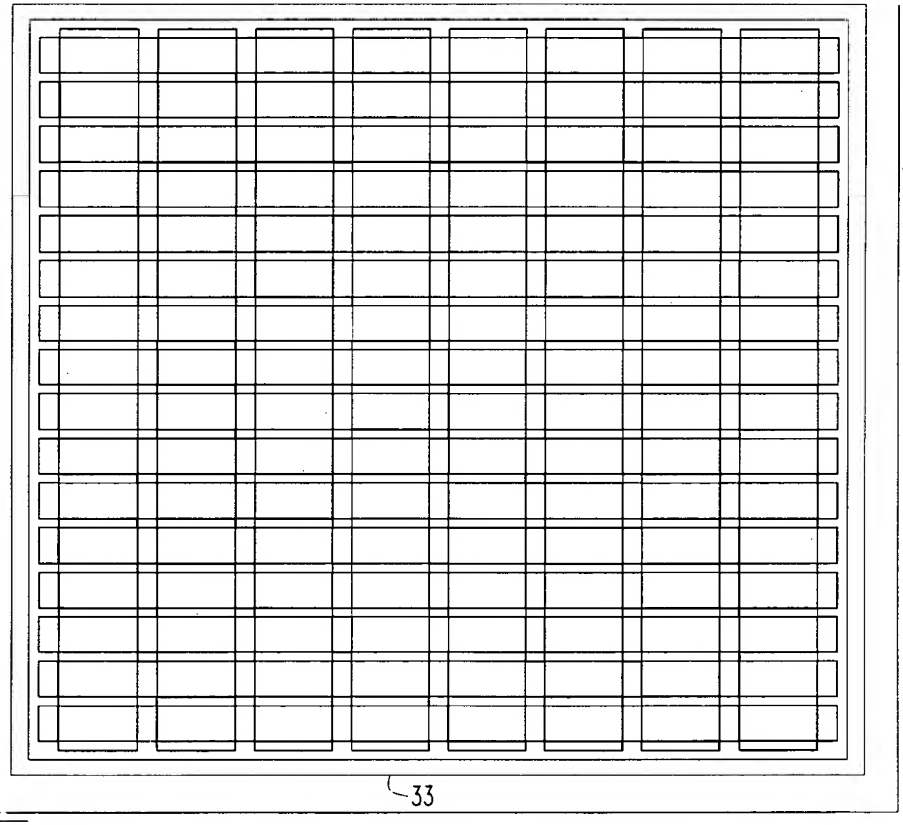


FIG. 33E4

Tosoco 02370860

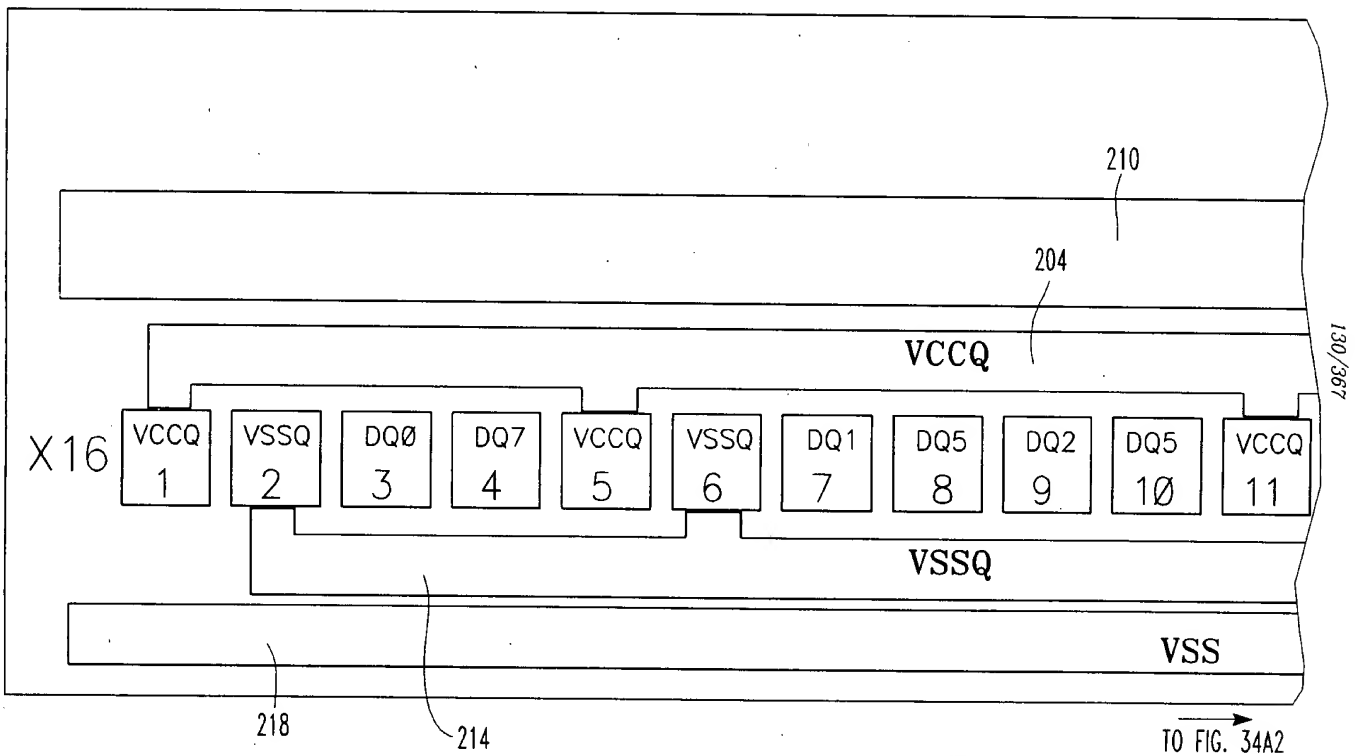


FIG. 34A1

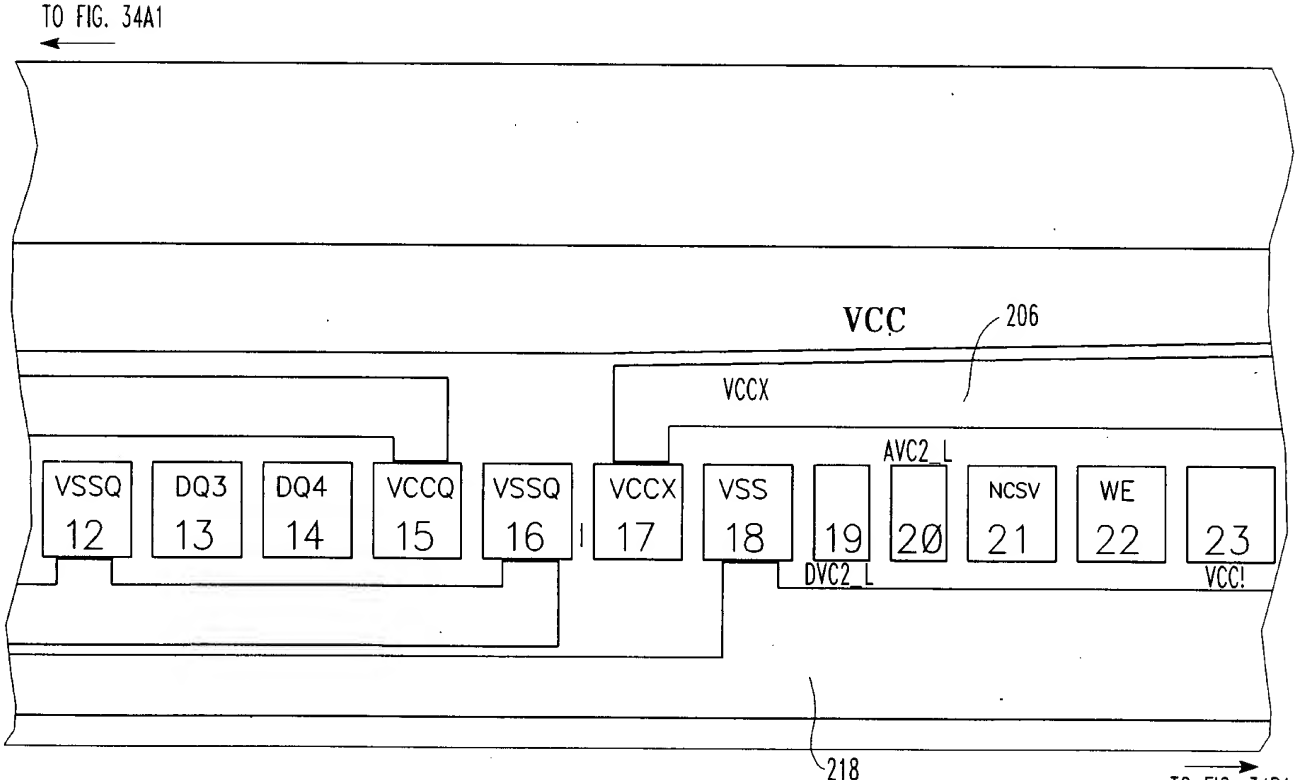

TO FIG. 34A1
VCC
206
VCCX
AVC2_L
VSSQ
12
DQ3
13
DQ4
14
VCCQ
15
VSSQ
16
VCCX
17
VSS
18
19
20
NCSV
21
WE
22
23
DVC2_L
VCC!
218
TO FIG. 34B1

FIG. 34A2

Tossed 02370660

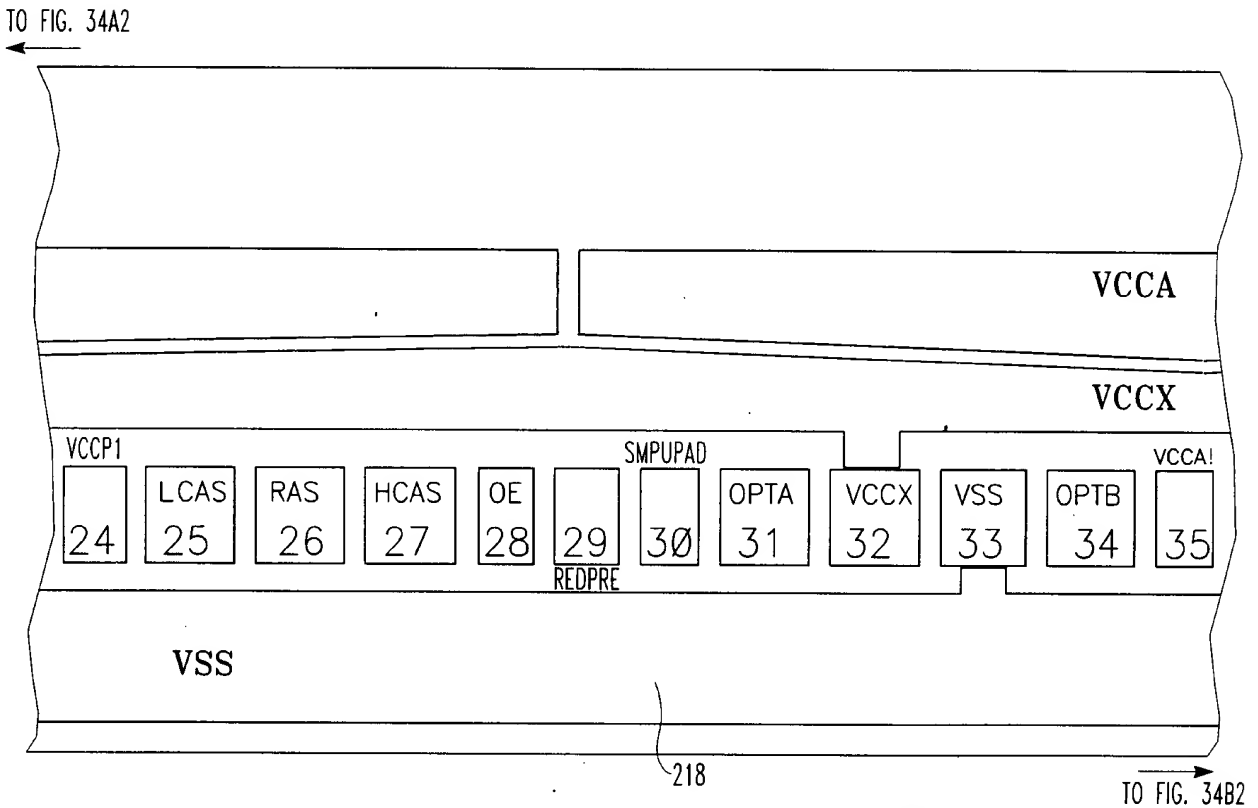


FIG. 34B1

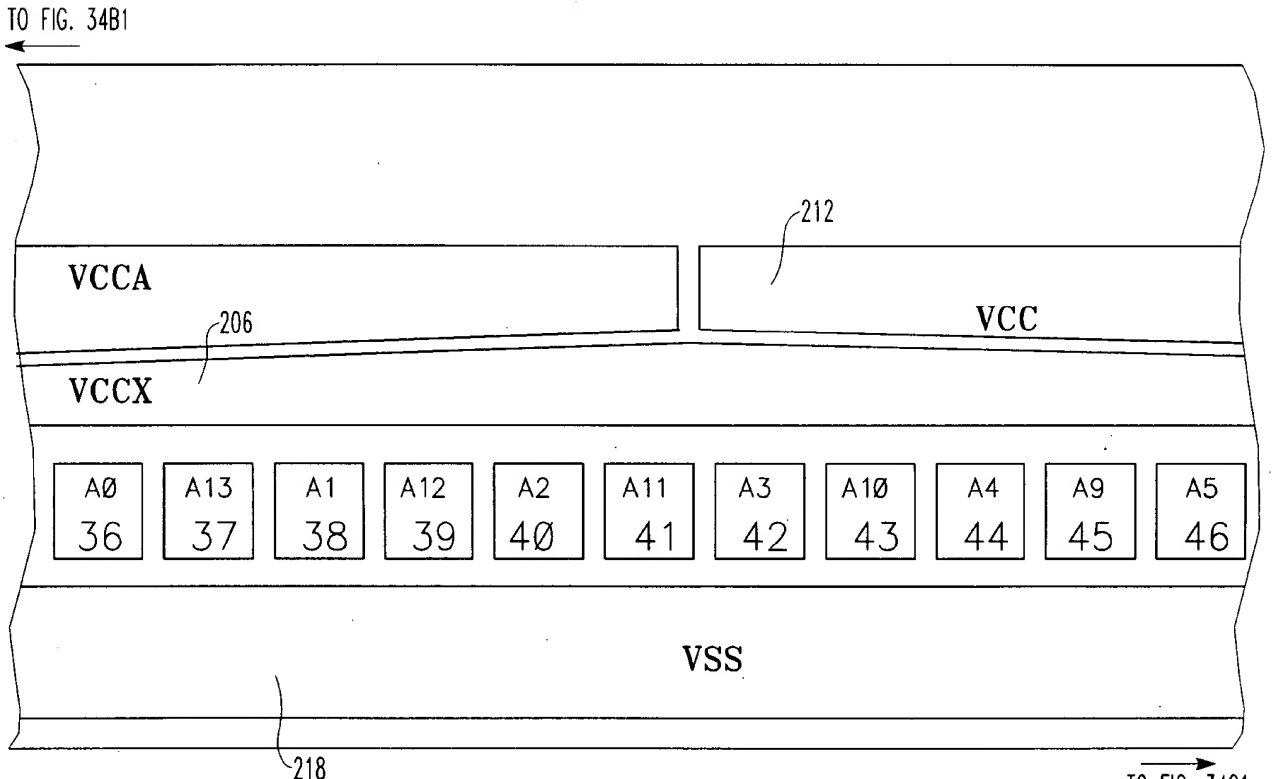

TO FIG. 34B1
212
VCCA
VCC
206
VCCX
A0
36
A13
37
A1
38
A12
39
A2
40
A11
41
A3
42
A10
43
A4
44
A9
45
A5
46
VSS
218
TO FIG. 34C1

FIG. 34B2

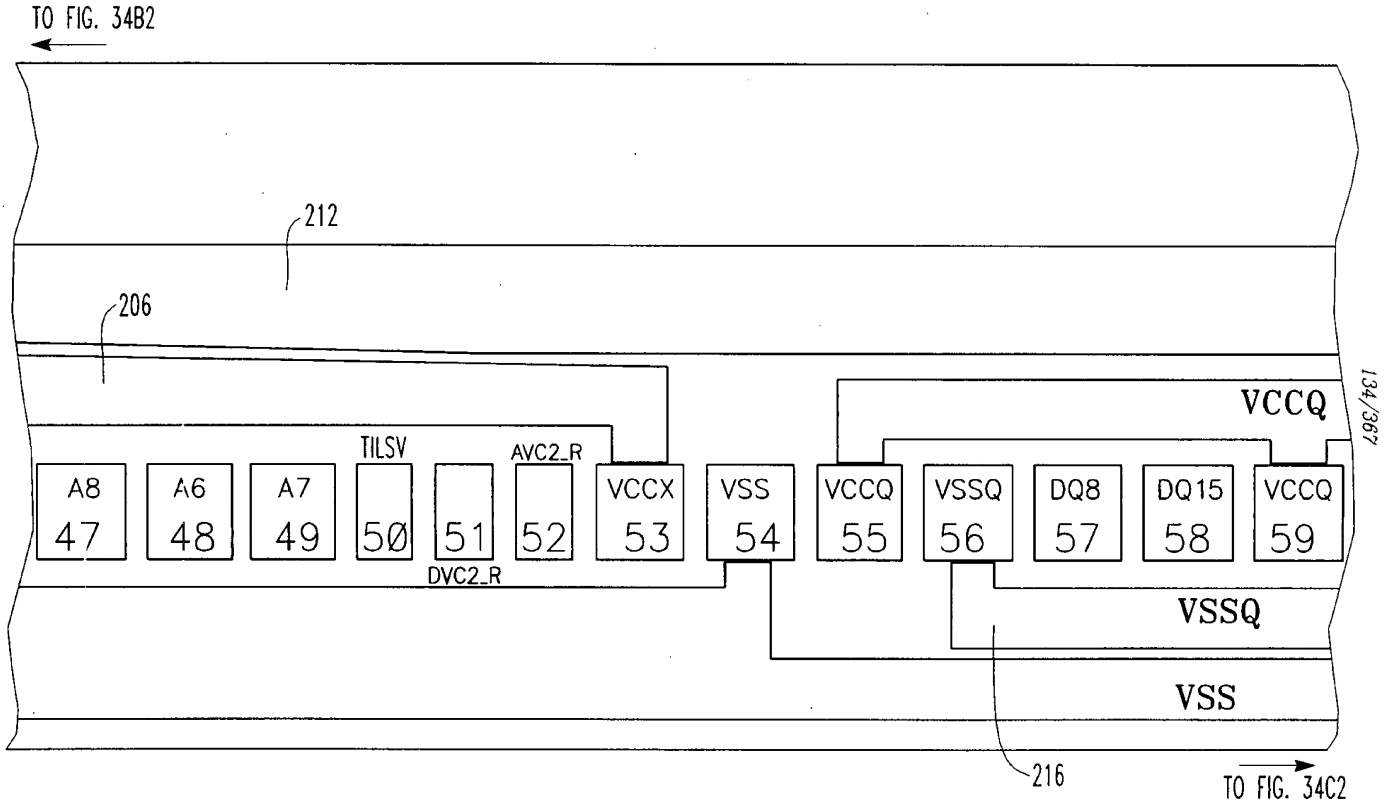

TO FIG. 34B2
212
206
VCCQ
TILSV
AVC2_R
A8
47
A6
48
A7
49
50
51
52
VCCX
53
VSS
54
VCCQ
55
VSSQ
56
DQ8
57
DQ15
58
VCCQ
59
DVC2_R
VSSQ
VSS
216
TO FIG. 34C2

FIG. 34C1

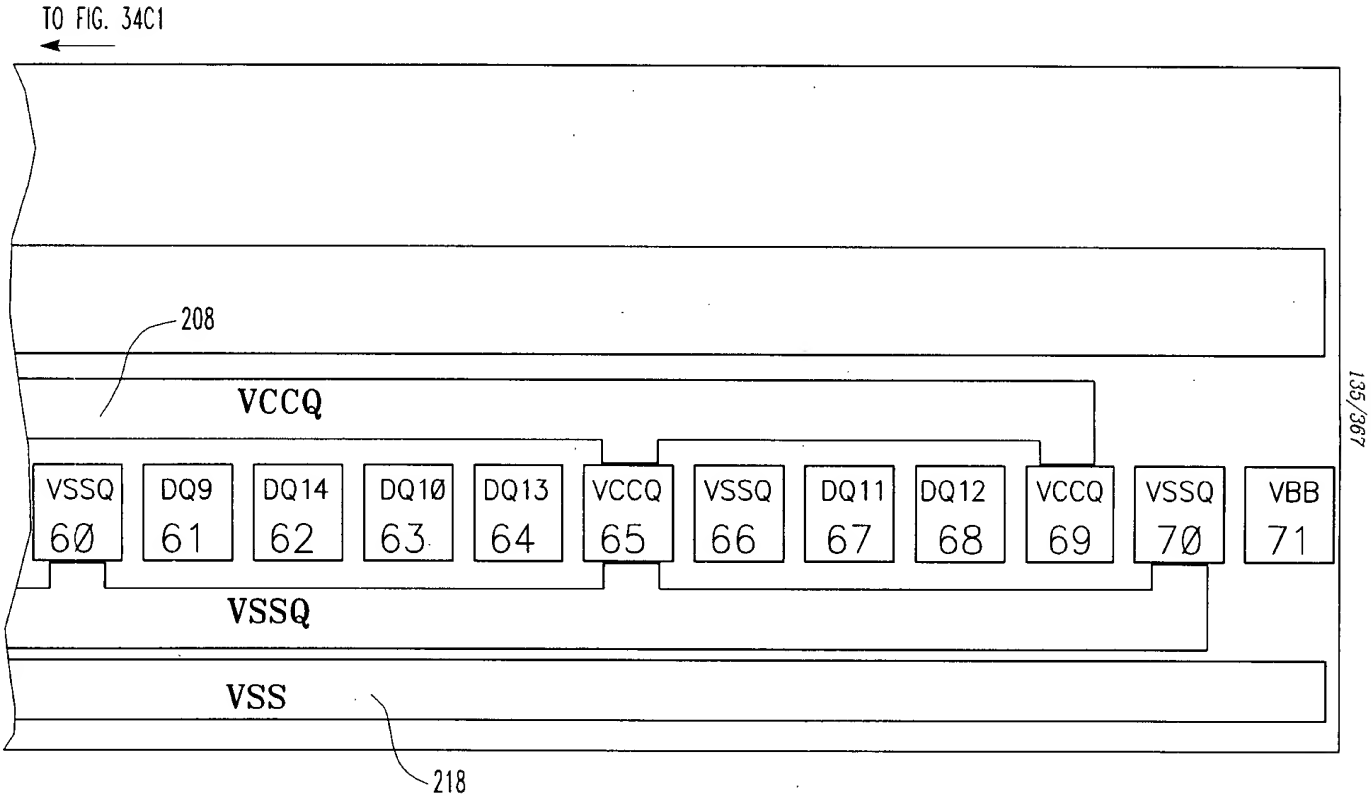

TO FIG. 34C1
208
VCCQ
VSSQ 60
DQ9 61
DQ14 62
DQ10 63
DQ13 64
VCCQ 65
VSSQ 66
DQ11 67
DQ12 68
VCCQ 69
VSSQ 70
VBB 71
VSSQ
VSS
218

FIG. 34C2

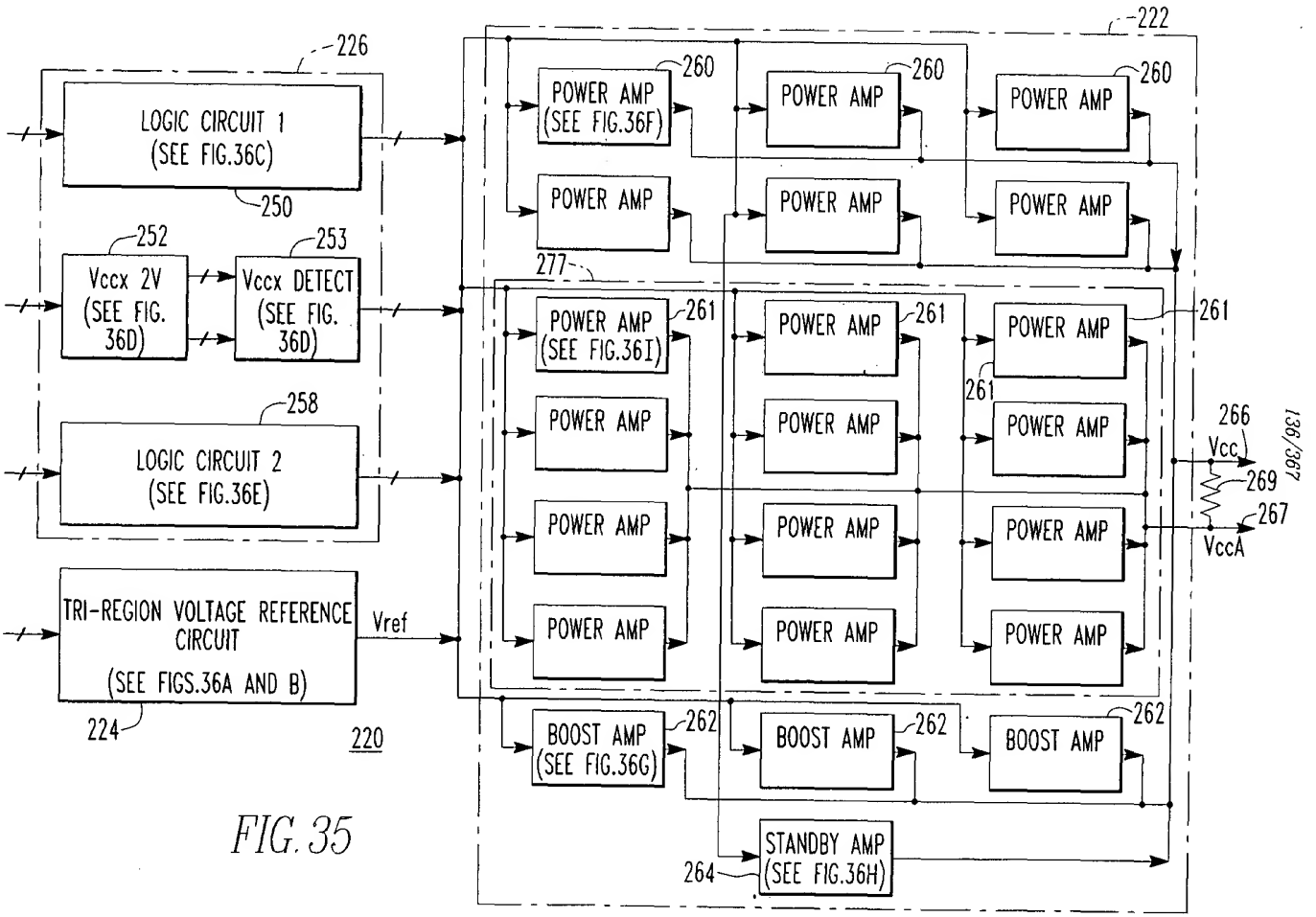

222
226
LOGIC CIRCUIT 1
(SEE FIG.36C)
250
252
Vccx 2V
(SEE FIG. 36D)
253
Vccx DETECT
(SEE FIG. 36D)
258
LOGIC CIRCUIT 2
(SEE FIG.36E)
TRI-REGION VOLTAGE REFERENCE CIRCUIT
(SEE FIGS.36A AND B)
Vref
224
220
POWER AMP
(SEE FIG.36F)
260
POWER AMP
277
POWER AMP
(SEE FIG.36I)
261
BOOST AMP
(SEE FIG.36G)
262
STANDBY AMP
(SEE FIG.36H)
264
266
Vcc
269
267
VccA

FIG. 35

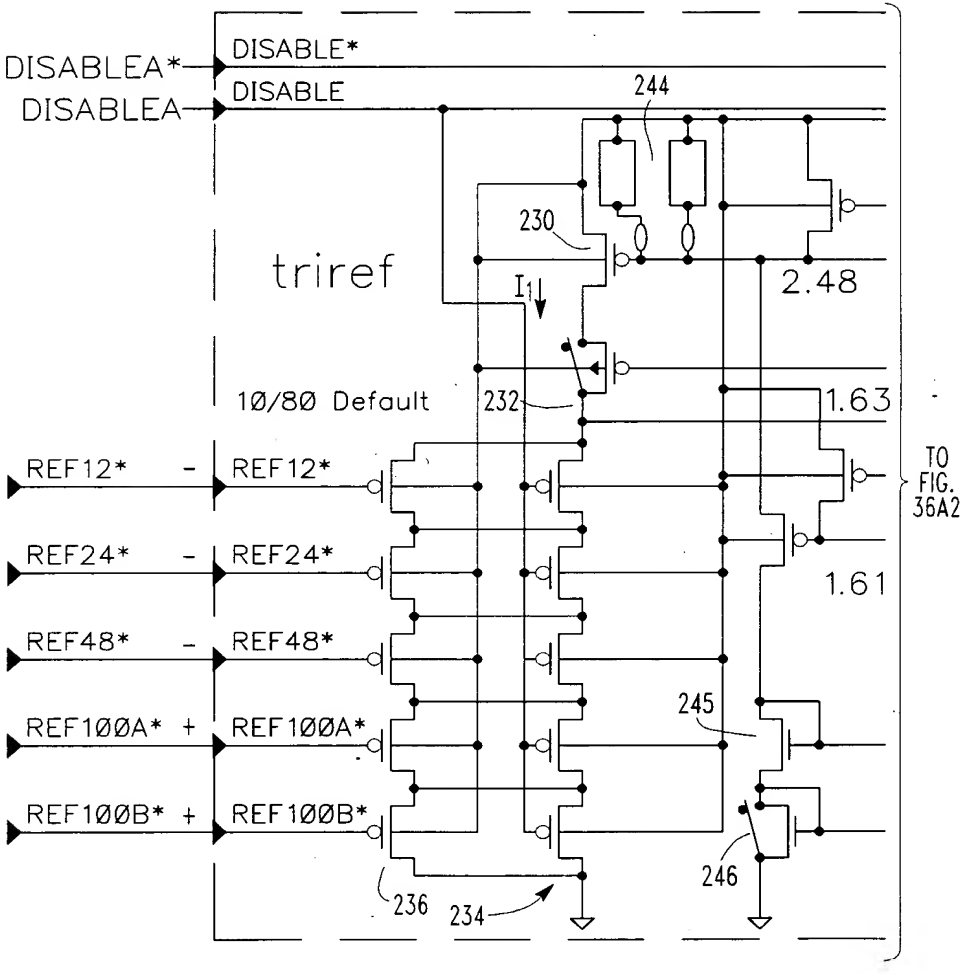

DISABLEA*
DISABLEA
DISABLE*
DISABLE
244
230
triref
I1
2.48
10/80 Default
232
1.63
REF12*
REF12*
REF24*
REF24*
REF48*
REF48*
REF100A*
REF100A*
REF100B*
REF100B*
TO FIG. 36A2
1.61
245
246
236
234

FIG. 36A1

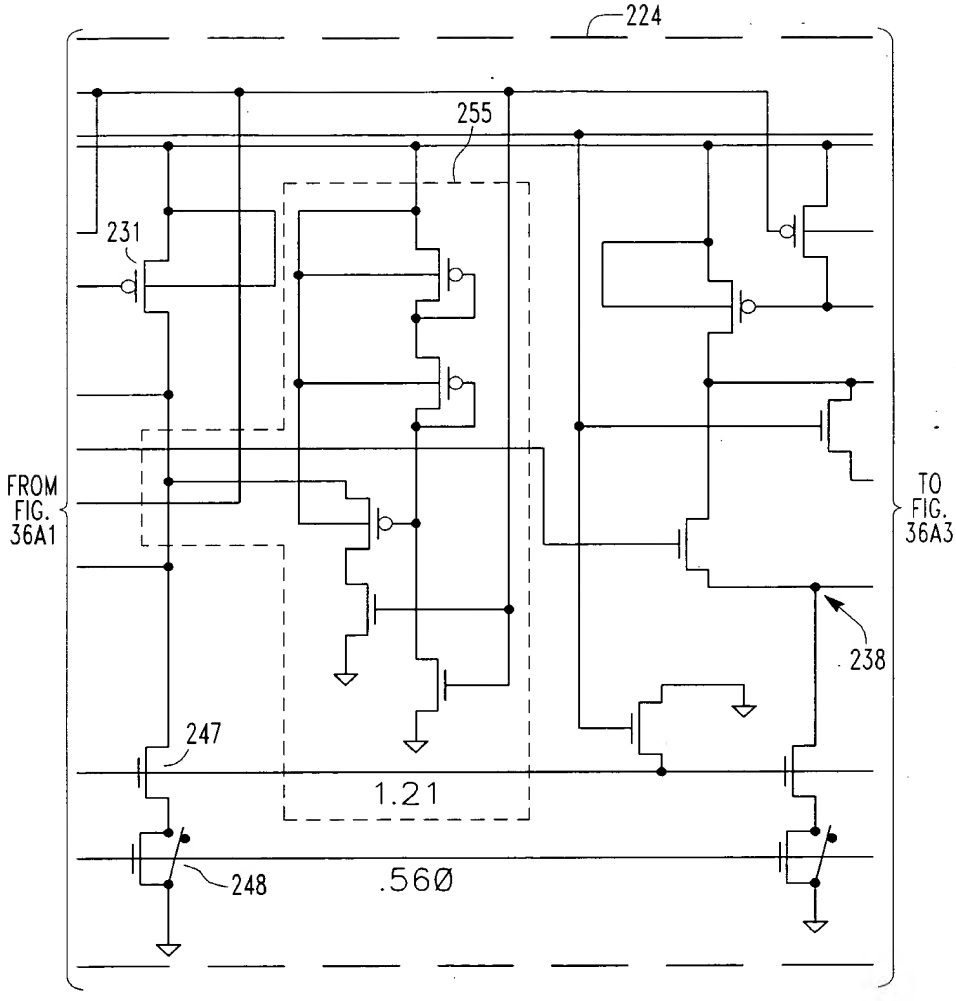


FIG. 36A2

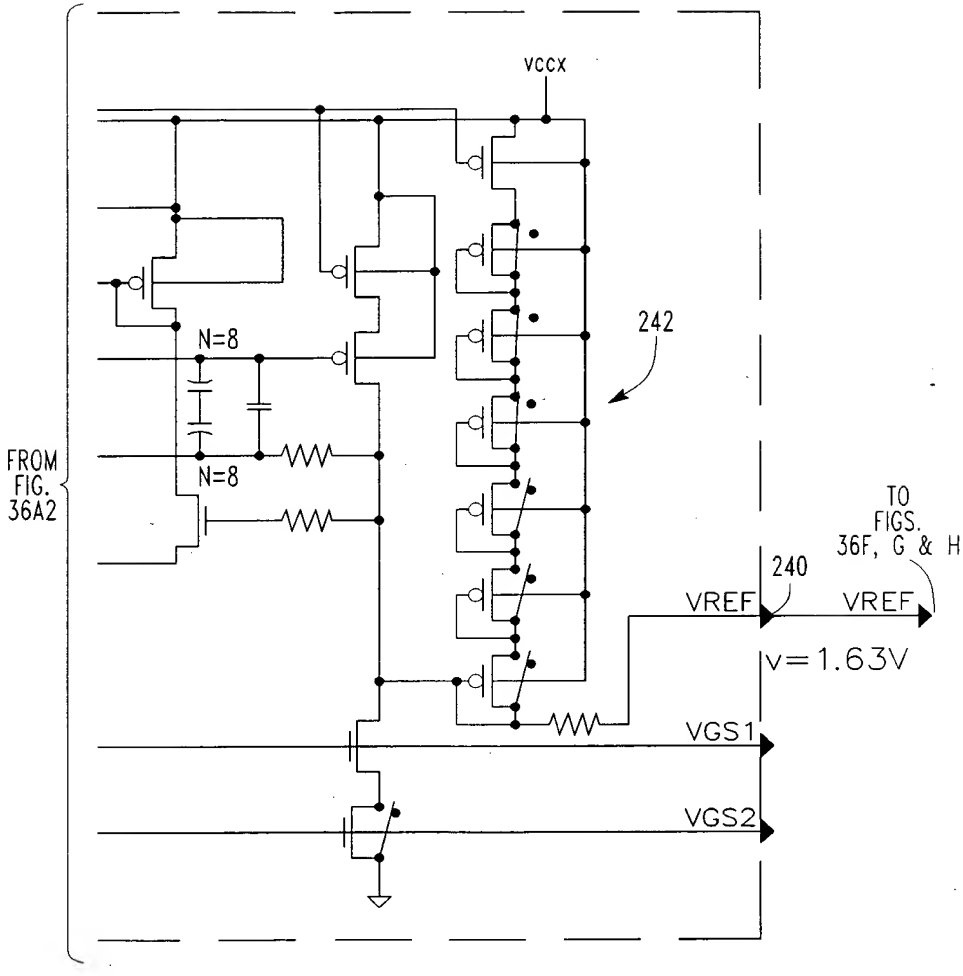

VCCX
242
N=8
N=8
FROM
FIG.
36A2
TO
FIGS.
36F, G & H
240
VREF
VREF
v=1.63V
VGS1
VGS2

FIG. 36A3

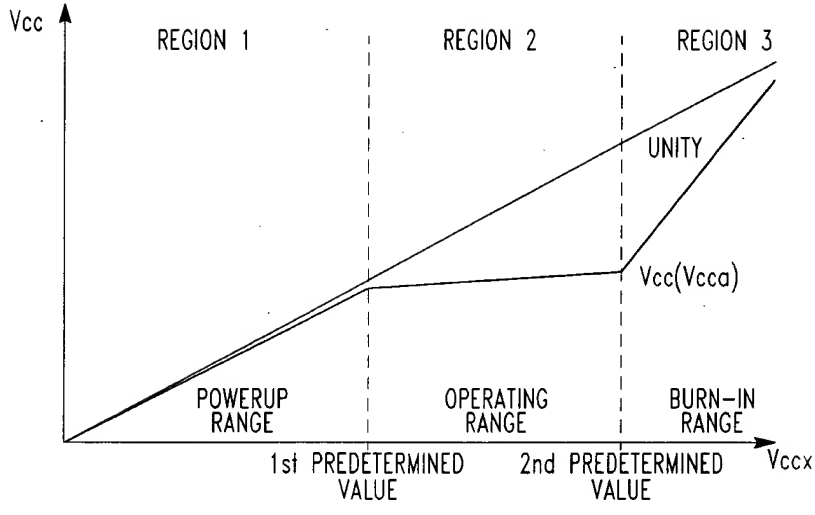

Vcc
REGION 1
REGION 2
REGION 3
UNITY
Vcc(Vcca)
POWERUP RANGE
OPERATING RANGE
BURN-IN RANGE
1st PREDETERMINED VALUE
2nd PREDETERMINED VALUE
Vccx

FIG. 36B

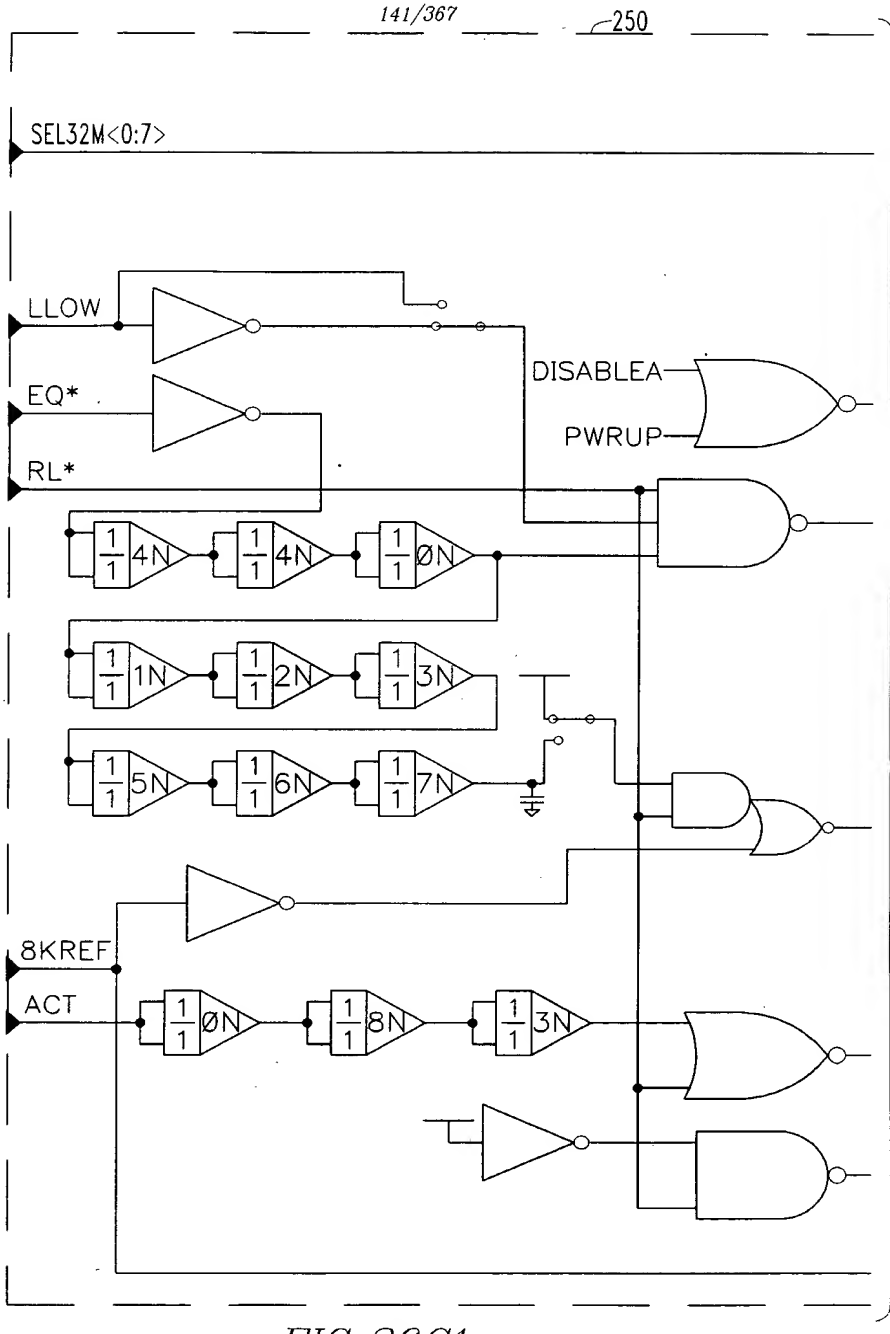

250
SEL32M<0:7>
LLOW
EQ*
RL*
DISABLEA
PWRUP
4N
4N
ØN
1N
2N
3N
5N
6N
7N
8KREF
ACT
ØN
8N
3N
TO FIG. 36C2

FIG. 36C1

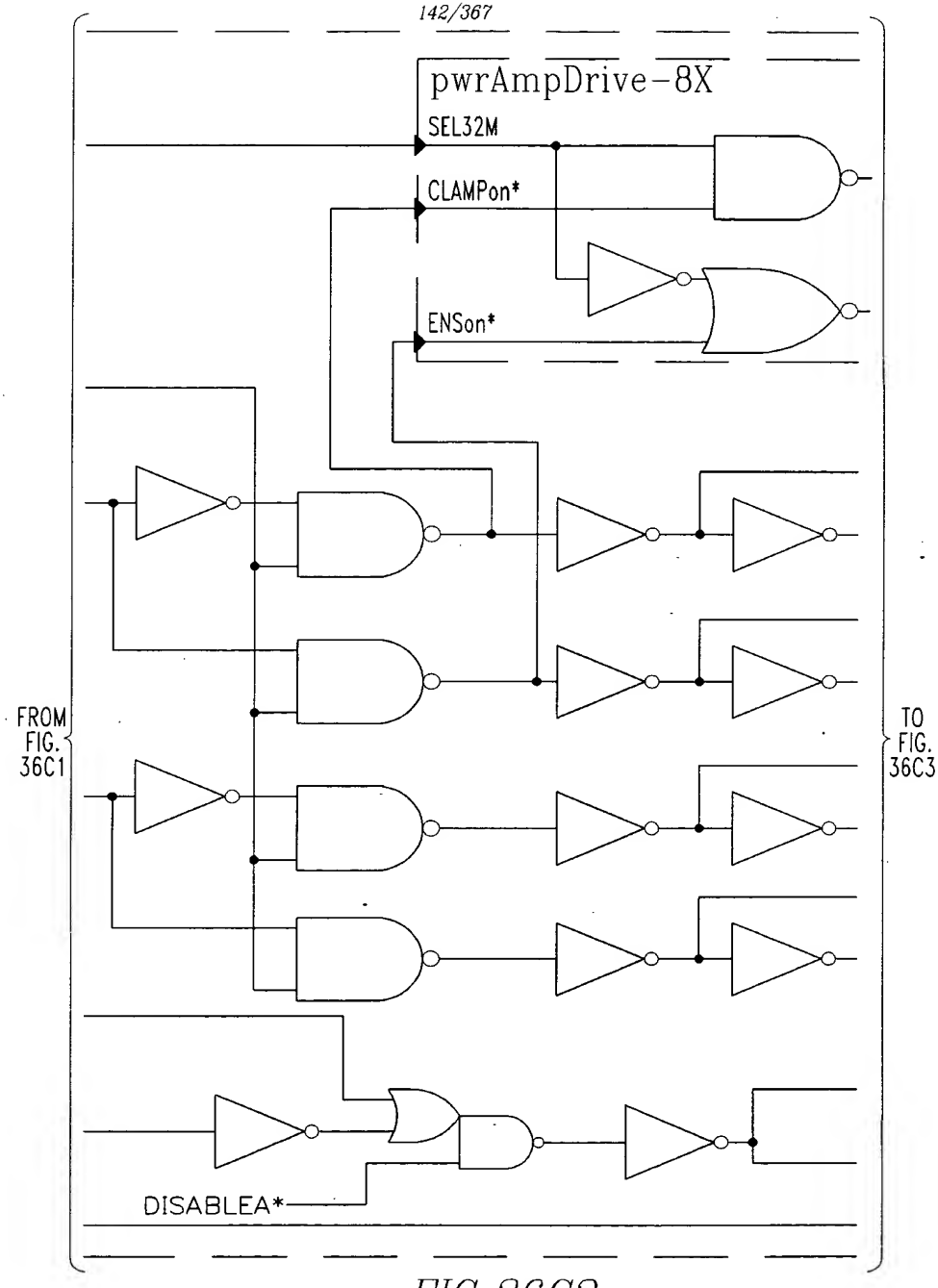


FIG. 36C2

Patent Application Publication Aug. 31, 2006 Sheet 142 of 367 US 2006/0195809 A1

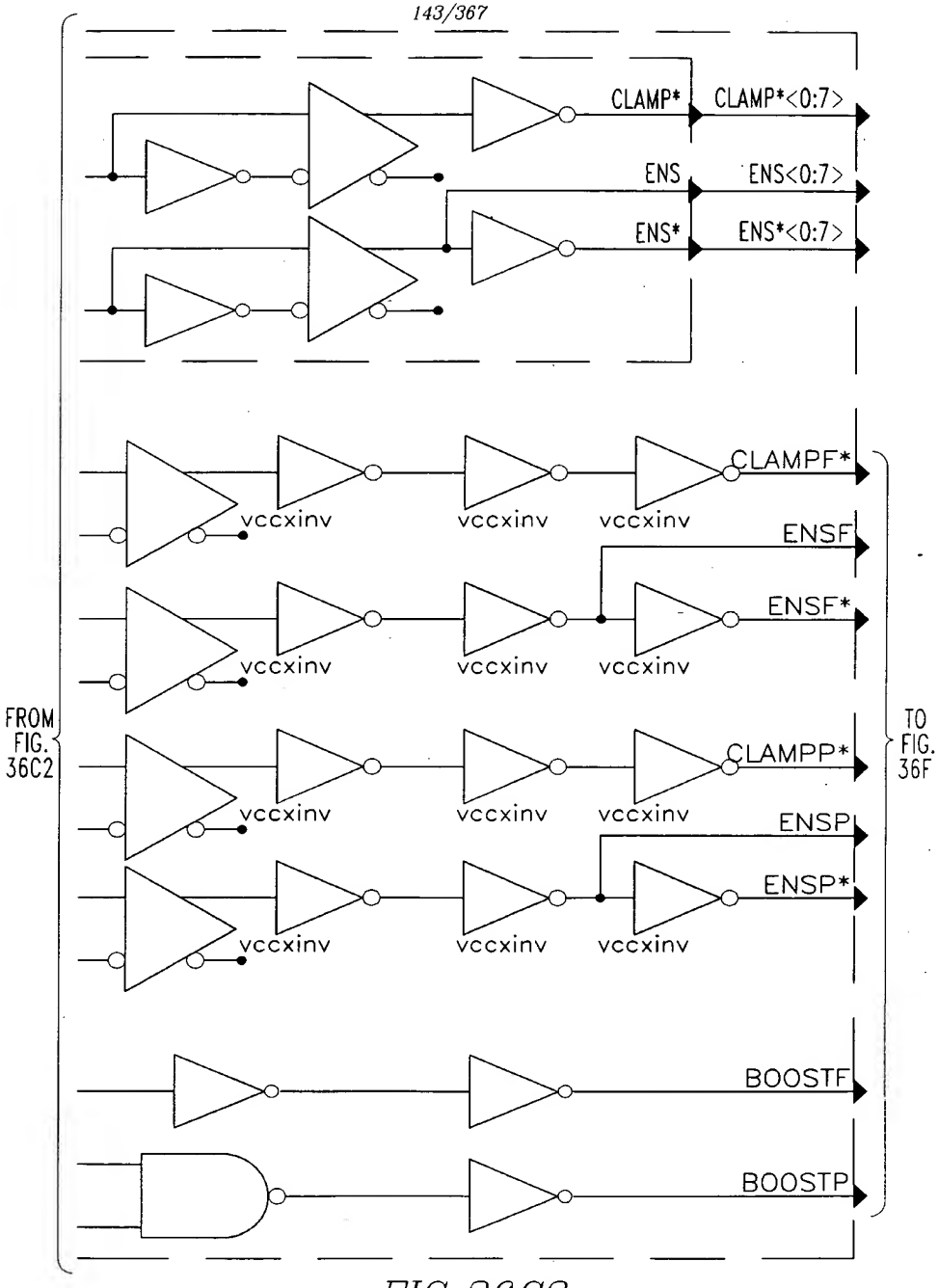

CLAMP*
CLAMP*<0:7>
ENS
ENS<0:7>
ENS*
ENS*<0:7>
FROM FIG. 36C2
vccxinv
CLAMPF*
ENSF
ENSF*
CLAMPP*
ENSP
ENSP*
TO FIG. 36F
BOOSTF
BOOSTP

FIG. 36C3

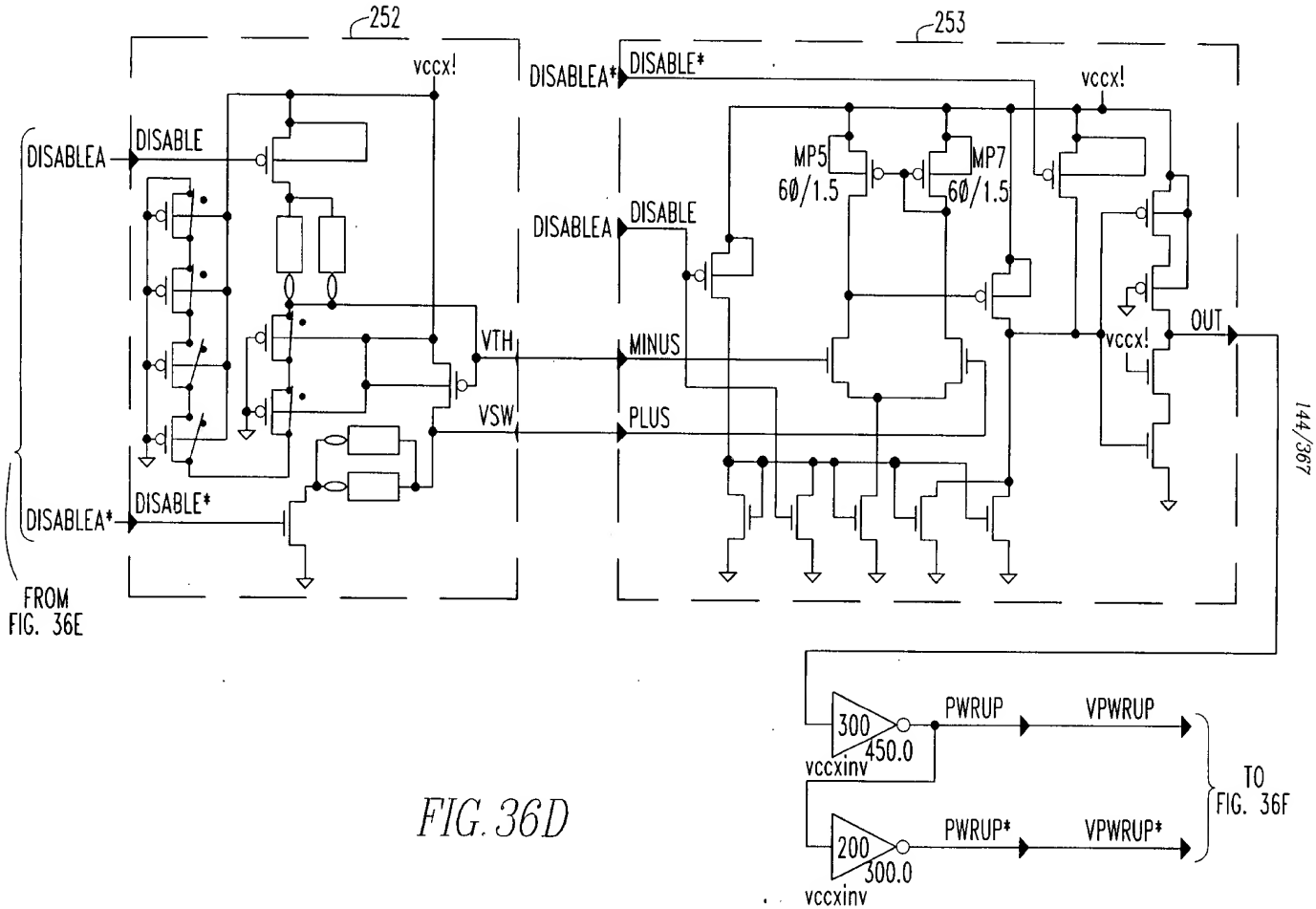

252
253
vccx!
DISABLEA*
DISABLE*
DISABLEA
DISABLE
MP5
60/1.5
MP7
60/1.5
VTH
MINUS
VSW
PLUS
OUT
DISABLE*
DISABLEA*
FROM
FIG. 36E
144/867
300
450.0
vccxinv
PWRUP
VPWRUP
200
300.0
PWRUP*
VPWRUP*
TO
FIG. 36F

FIG. 36D

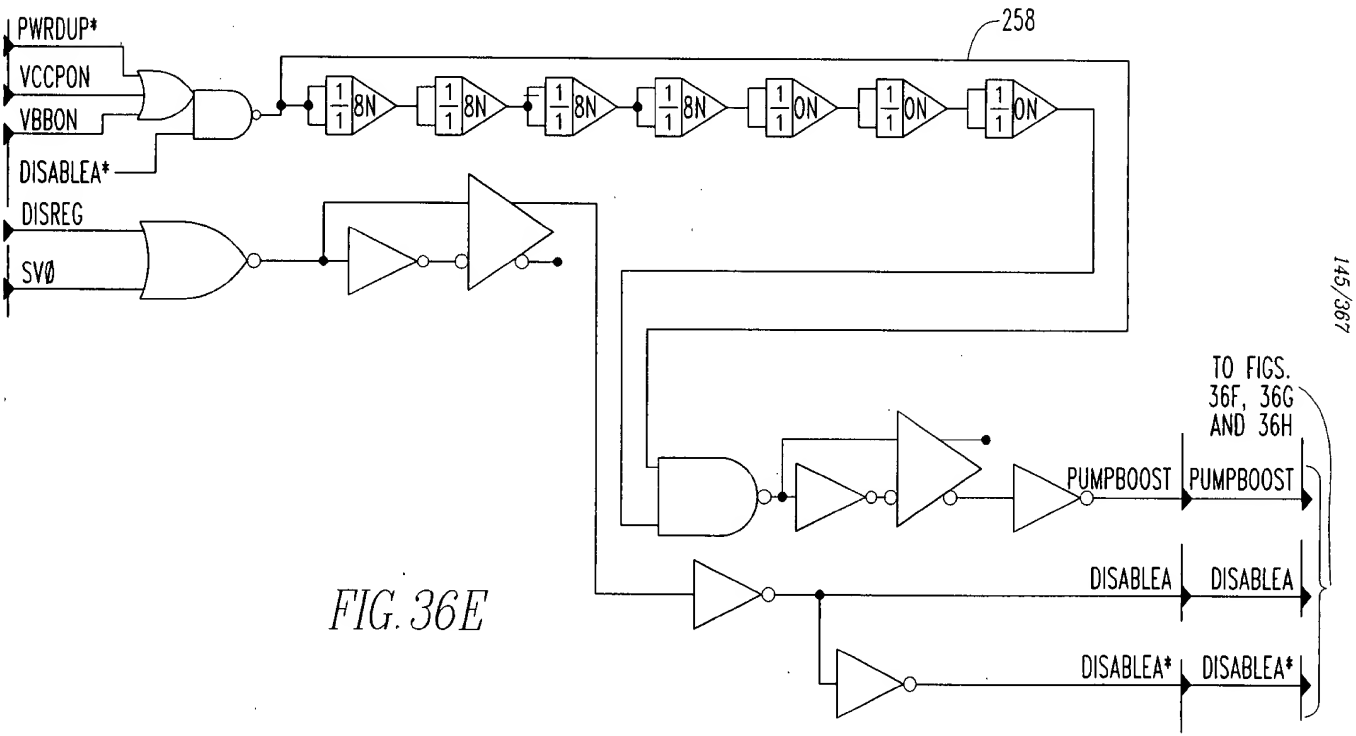

PWRDUP*
VCCPON
VBBON
DISABLEA*
DISREG
SVØ
258
1/1 8N
1/1 8N
1/1 8N
1/1 8N
1/1 ON
1/1 ON
1/1 ON
TO FIGS. 36F, 36G AND 36H
PUMPBOOST
PUMPBOOST
DISABLEA
DISABLEA
DISABLEA*
DISABLEA*

FIG. 36E

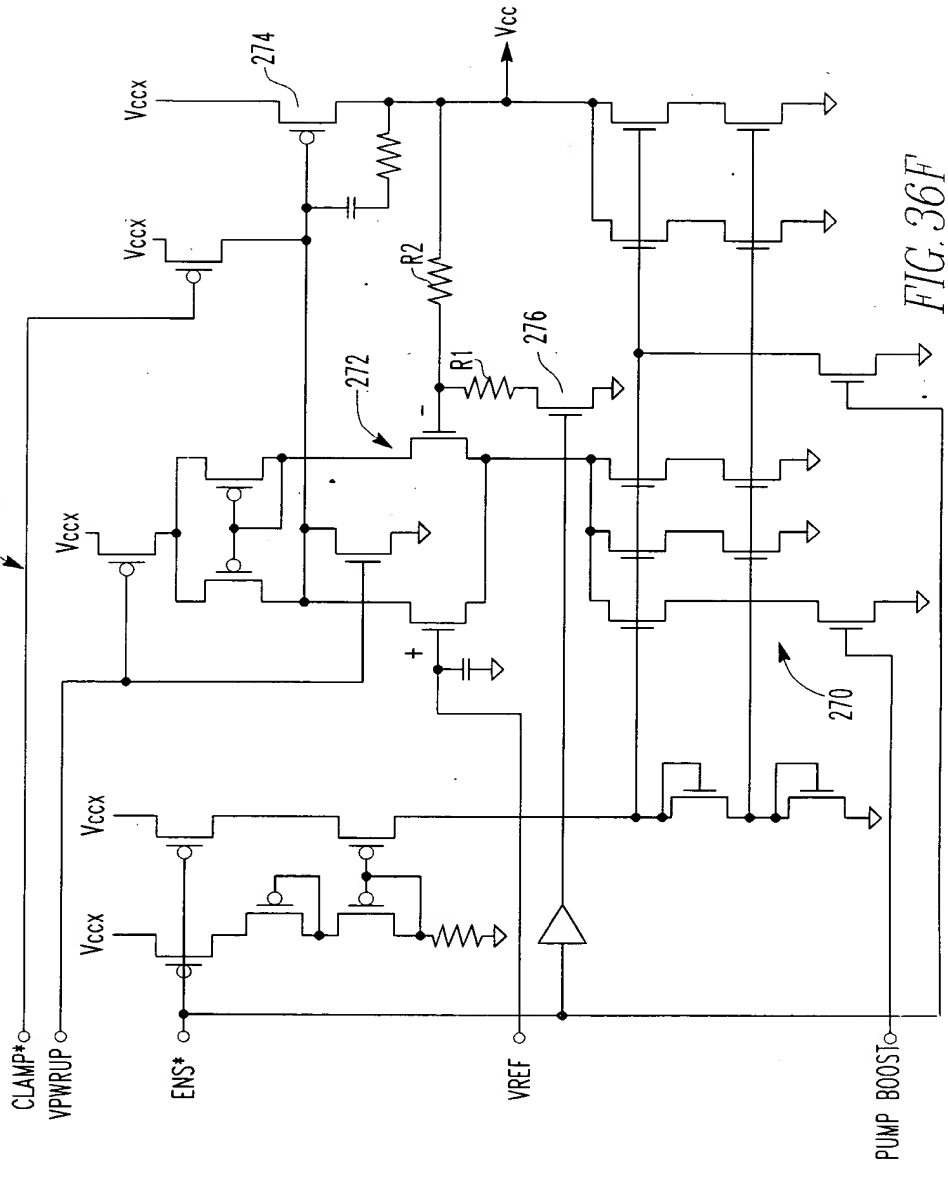

260
274
Vccx
Vcc
R2
R1
276
272
270
CLAMP*
VPWRUP
ENS*
VREF
PUMP BOOST

FIG. 36F

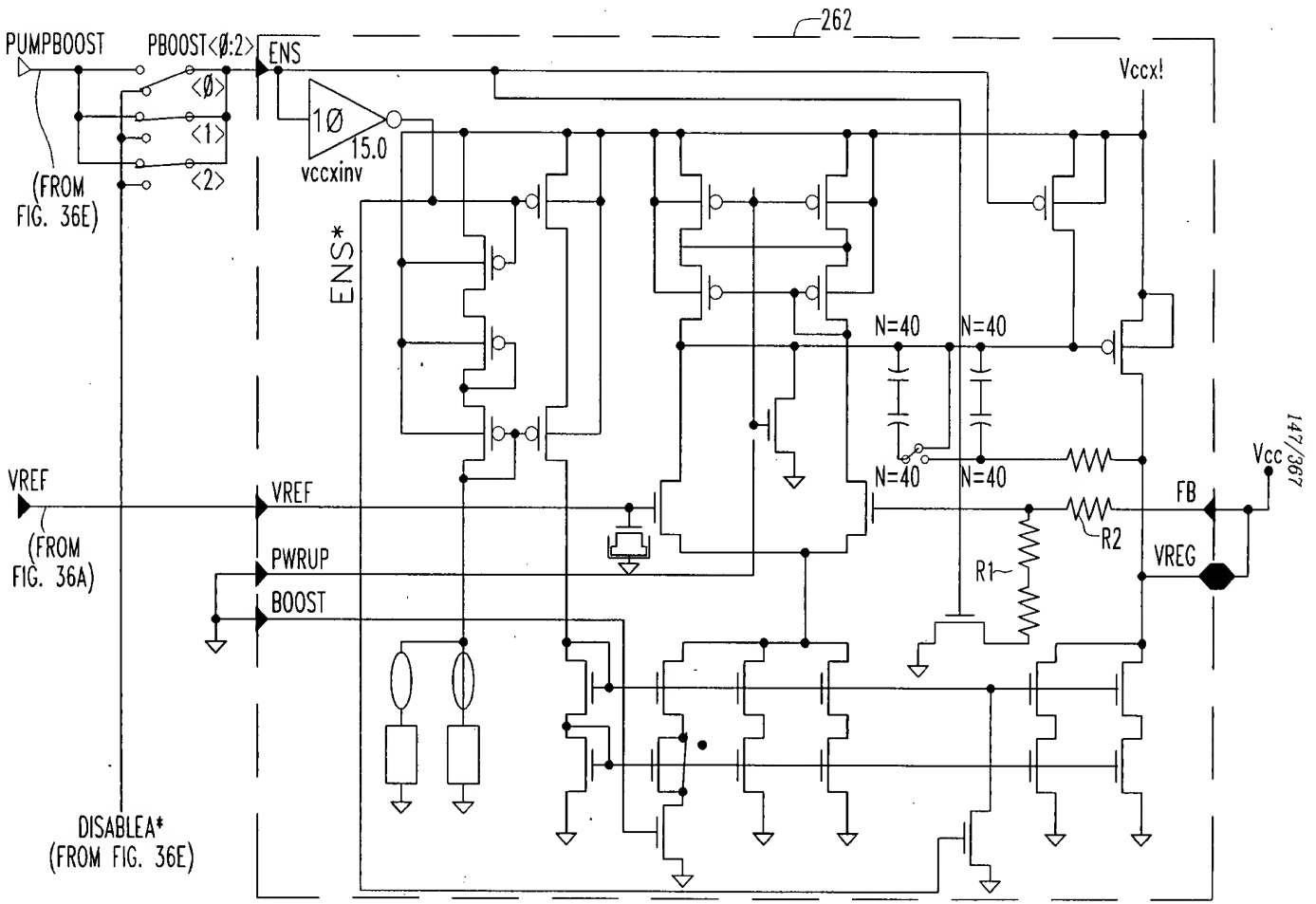

262
PUMPBOOST
PBOOST<Ø:2>
ENS
<Ø>
<1>
<2>
(FROM FIG. 36E)
1Ø
15.0
vccxinv
ENS*
Vccx!
N=40
N=40
N=40
N=40
VREF
(FROM FIG. 36A)
VREF
PWRUP
BOOST
DISABLEA*
(FROM FIG. 36E)
R1
R2
FB
VREG
Vcc

FIG. 36G

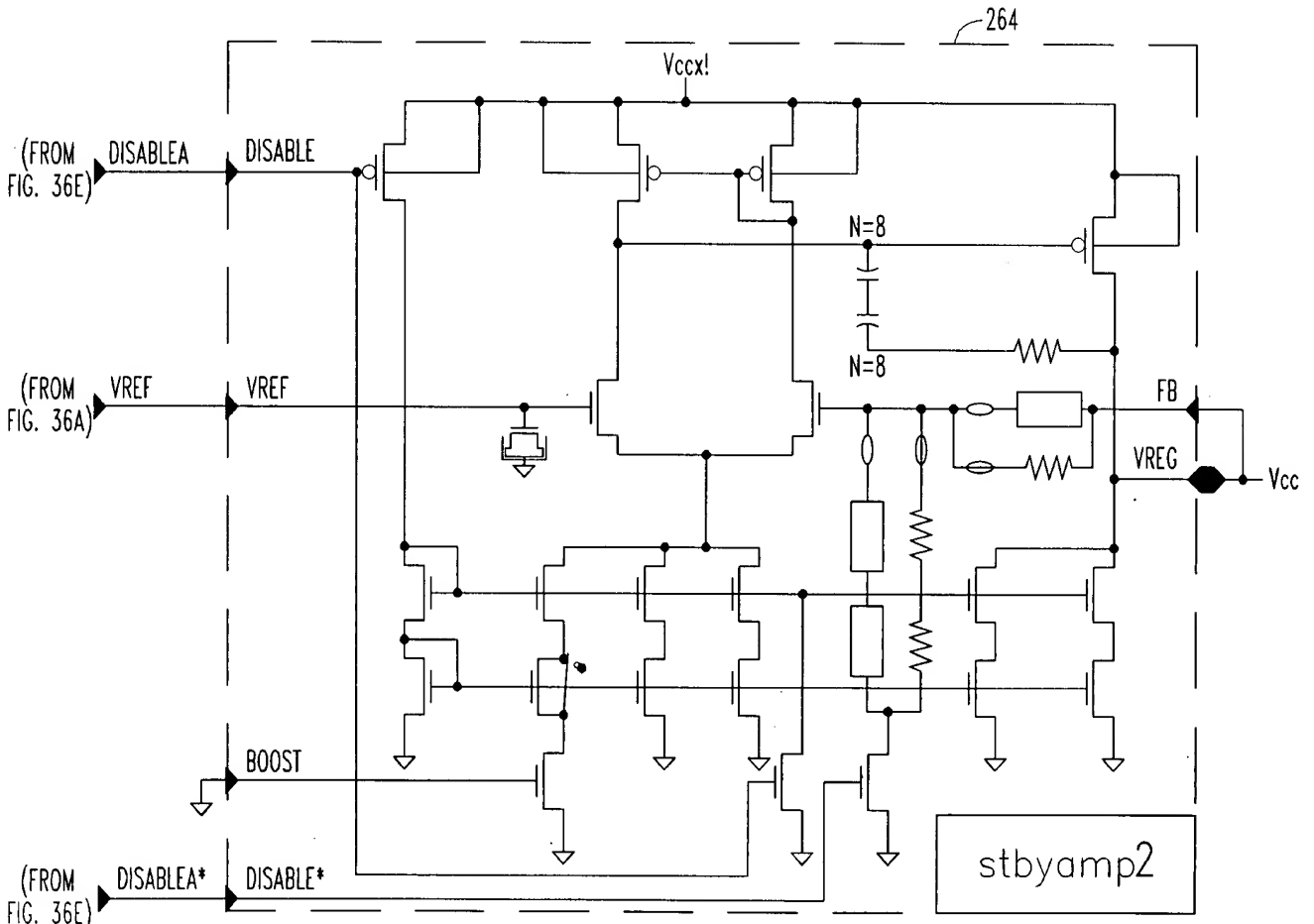

264
Vccx!
(FROM FIG. 36E)
DISABLEA
DISABLE
N=8
N=8
(FROM FIG. 36A)
VREF
VREF
FB
VREG
Vcc
BOOST
(FROM FIG. 36E)
DISABLEA*
DISABLE*
stbyamp2

FIG. 36H

FOGGED 02970260

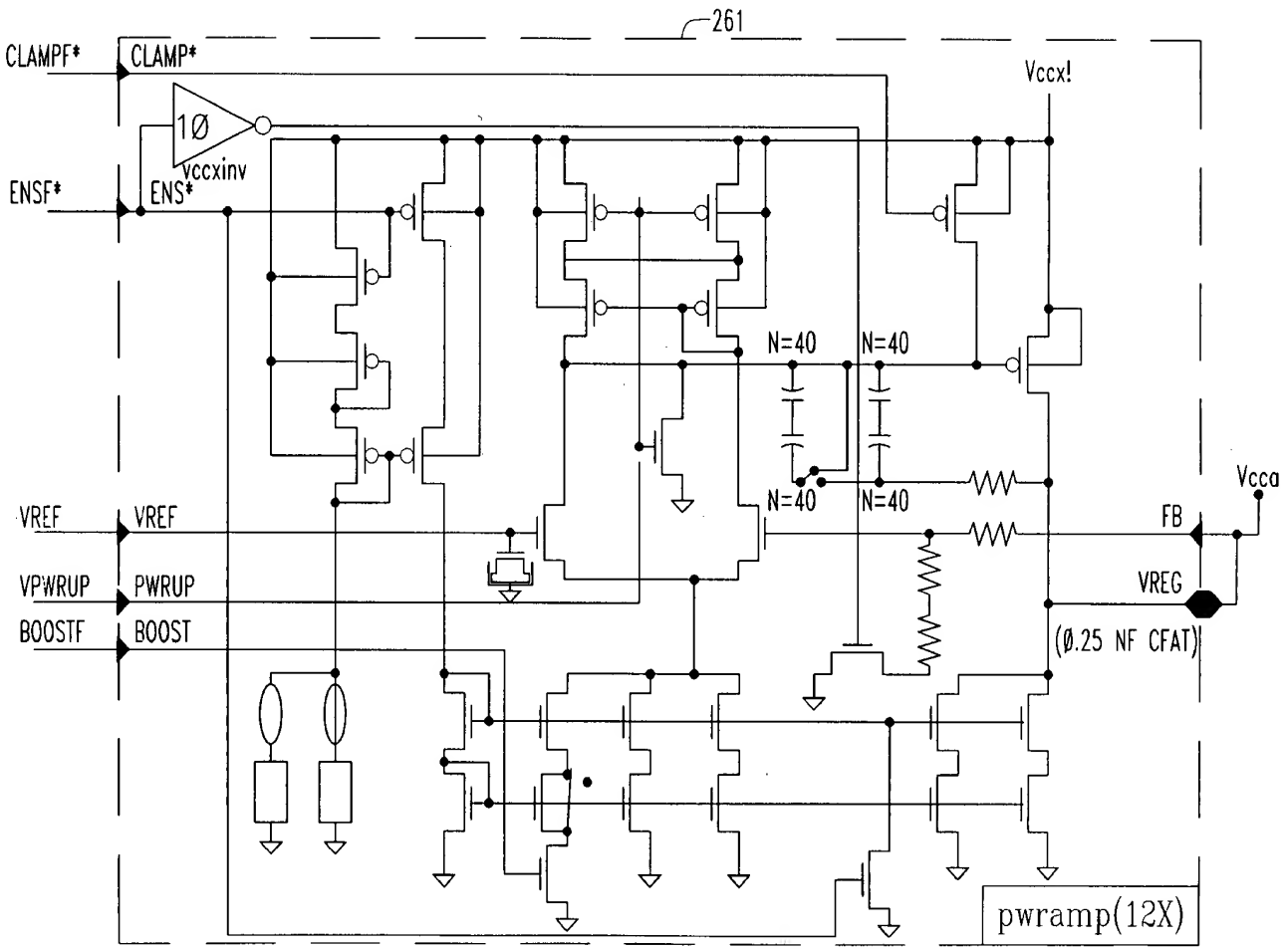


FIG. 36I

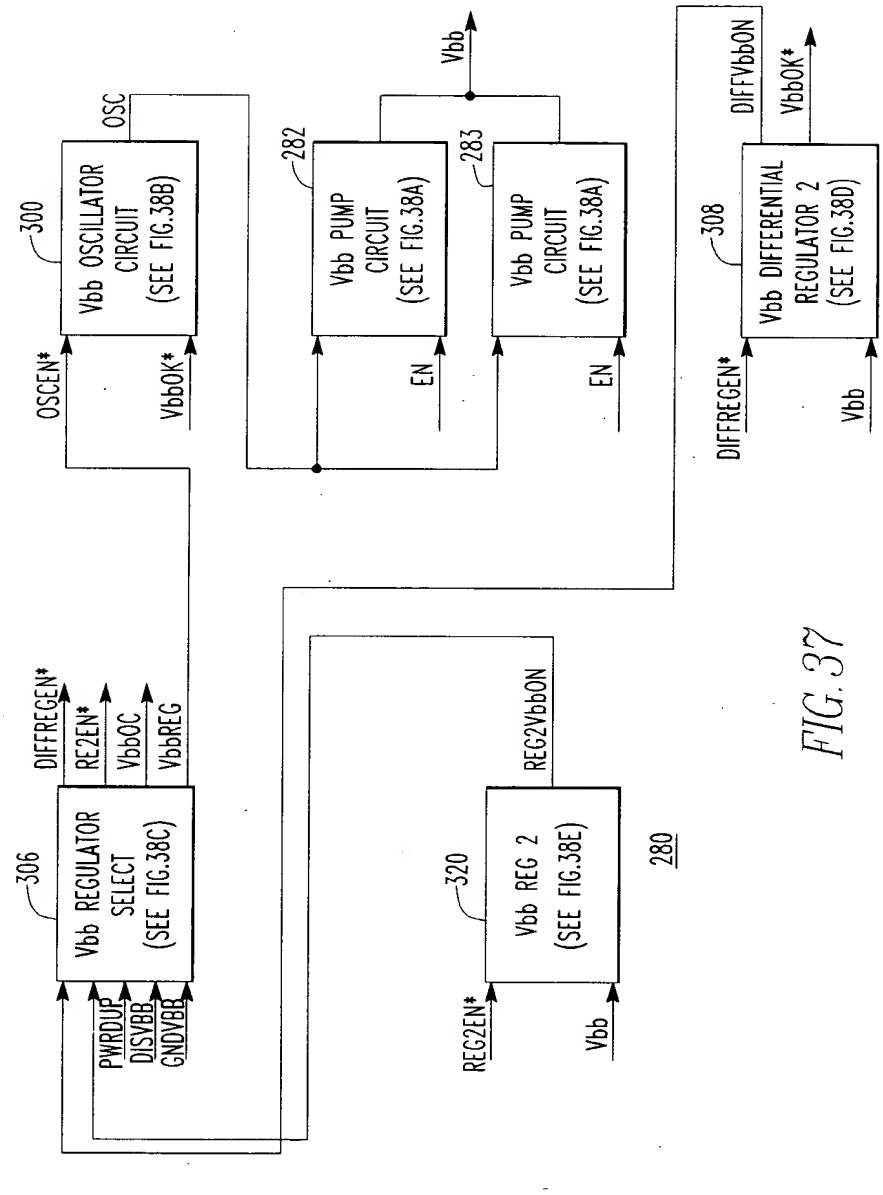

300
Vbb OSCILLATOR CIRCUIT (SEE FIG.38B)
OSC
OSCEN*
VbbOK*
282
Vbb PUMP CIRCUIT (SEE FIG.38A)
283
Vbb PUMP CIRCUIT (SEE FIG.38A)
Vbb
EN
EN
308
Vbb DIFFERENTIAL REGULATOR 2 (SEE FIG.38D)
DIFFVbbON
VbbOK*
DIFFREGEN*
Vbb
306
Vbb REGULATOR SELECT (SEE FIG.38C)
DIFFREGEN*
RE2EN*
VbbOC
VbbREG
PWRDUP
DISVBB
GNDVBB
320
Vbb REG 2 (SEE FIG.38E)
REG2VbbON
REG2EN*
Vbb
280

FIG. 37

TOSCO-82970860

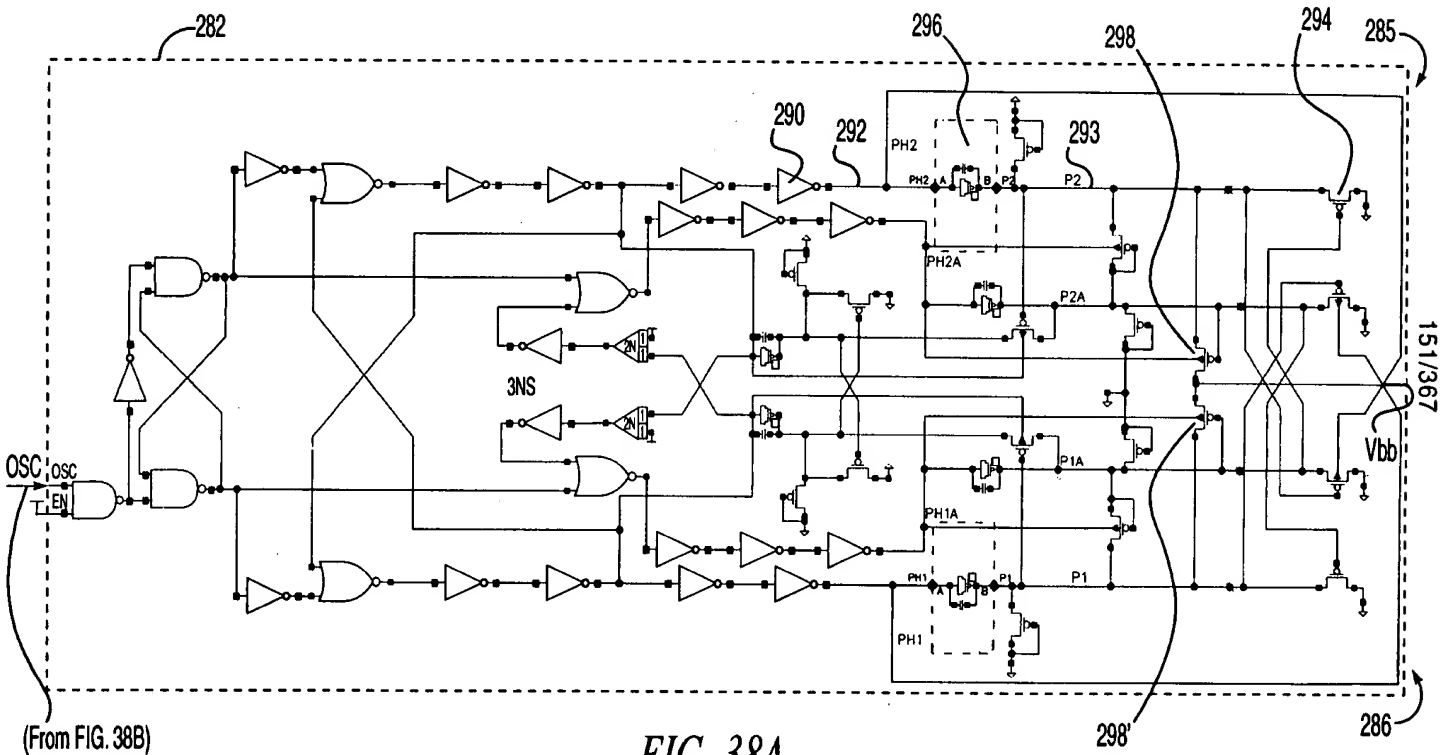


FIG. 38A

TOSHIBA 8297D660

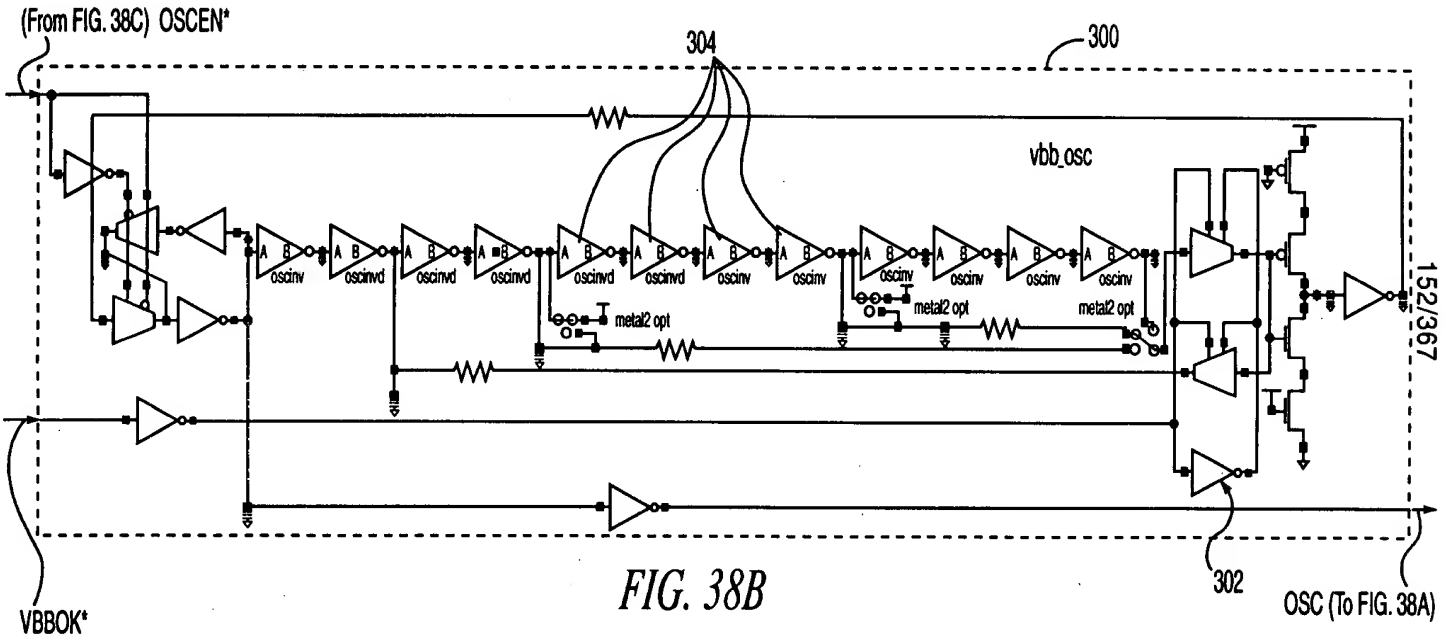


FIG. 38B

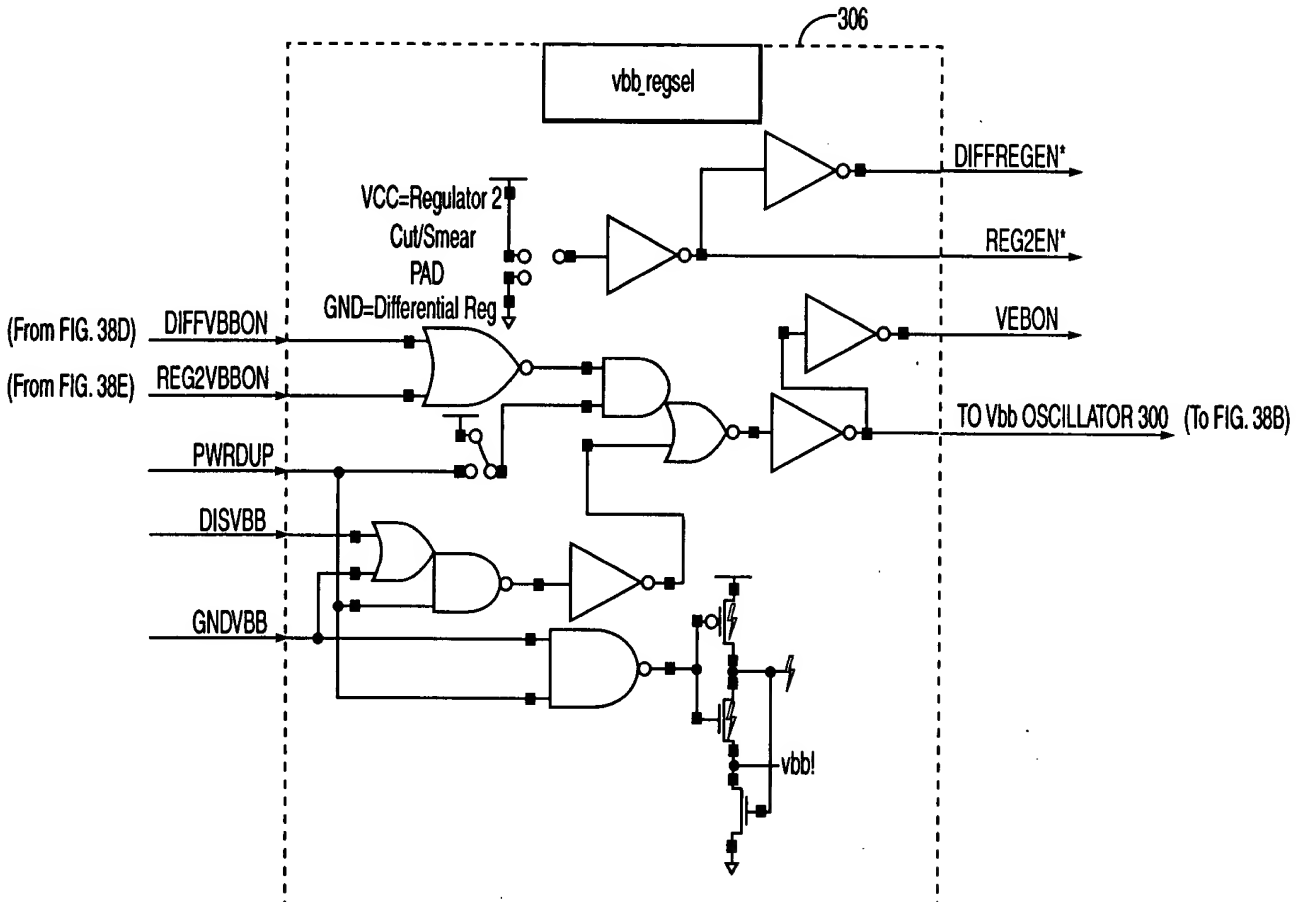

306
vbb_regsel
DIFFREGEN*
VCC=Regulator 2
Cut/Smear
PAD
GND=Differential Reg
REG2EN*
VEBON
(From FIG. 38D)
DIFFVBBON
(From FIG. 38E)
REG2VBBON
TO Vbb OSCILLATOR 300 (To FIG. 38B)
PWRDUP
DISVBB
GNDVBB
vbb!

FIG. 38C

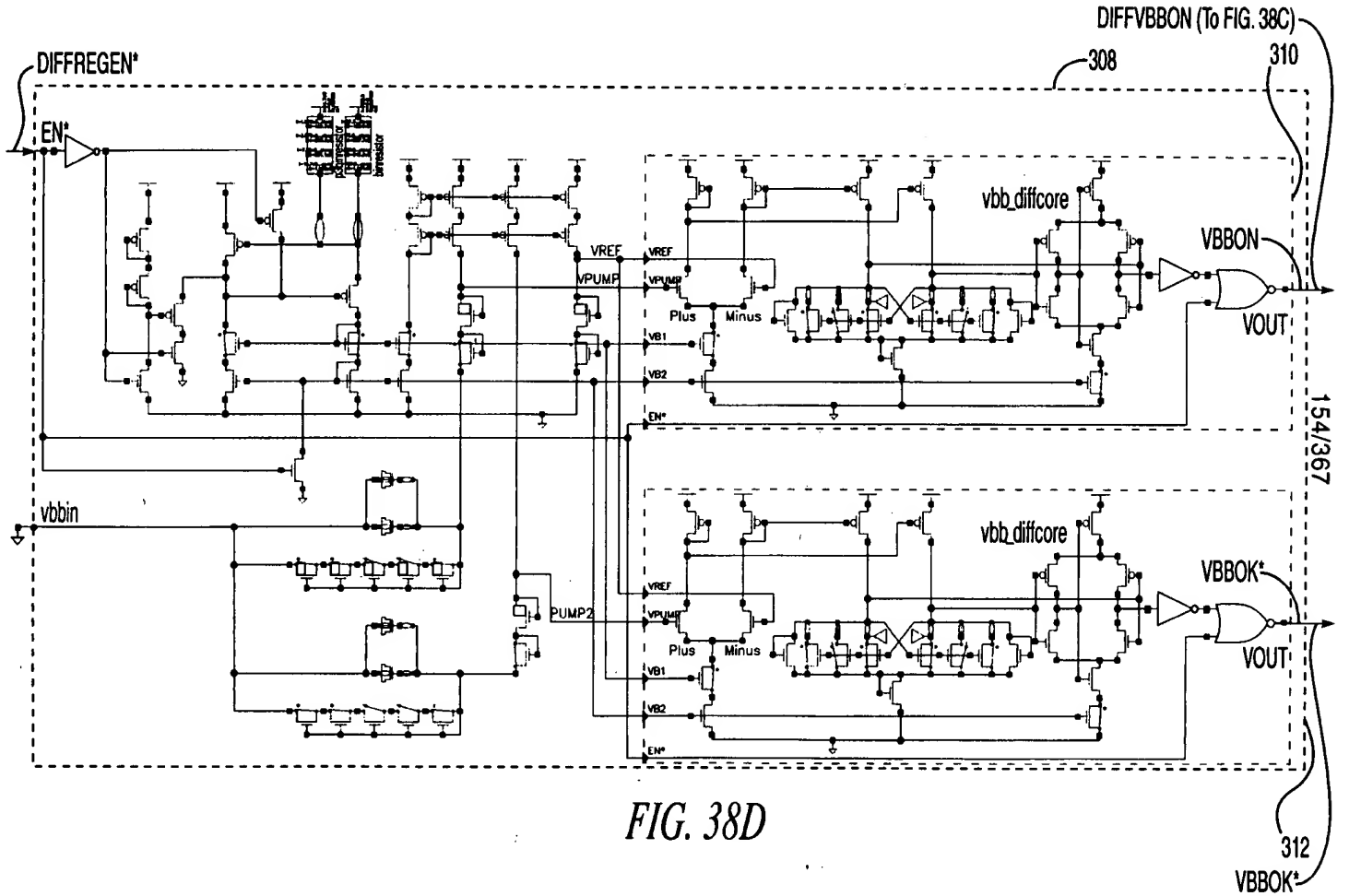

DIFFVBBON (To FIG. 38C)
DIFFREGEN*
308
310
EN*
VREF
VPUMP
vbb_diffcore
VBBON
Plus
Minus
VOUT
VB1
VB2
EN*
vbbin
PUMP2
VBBOK*
312
154/367

FIG. 38D

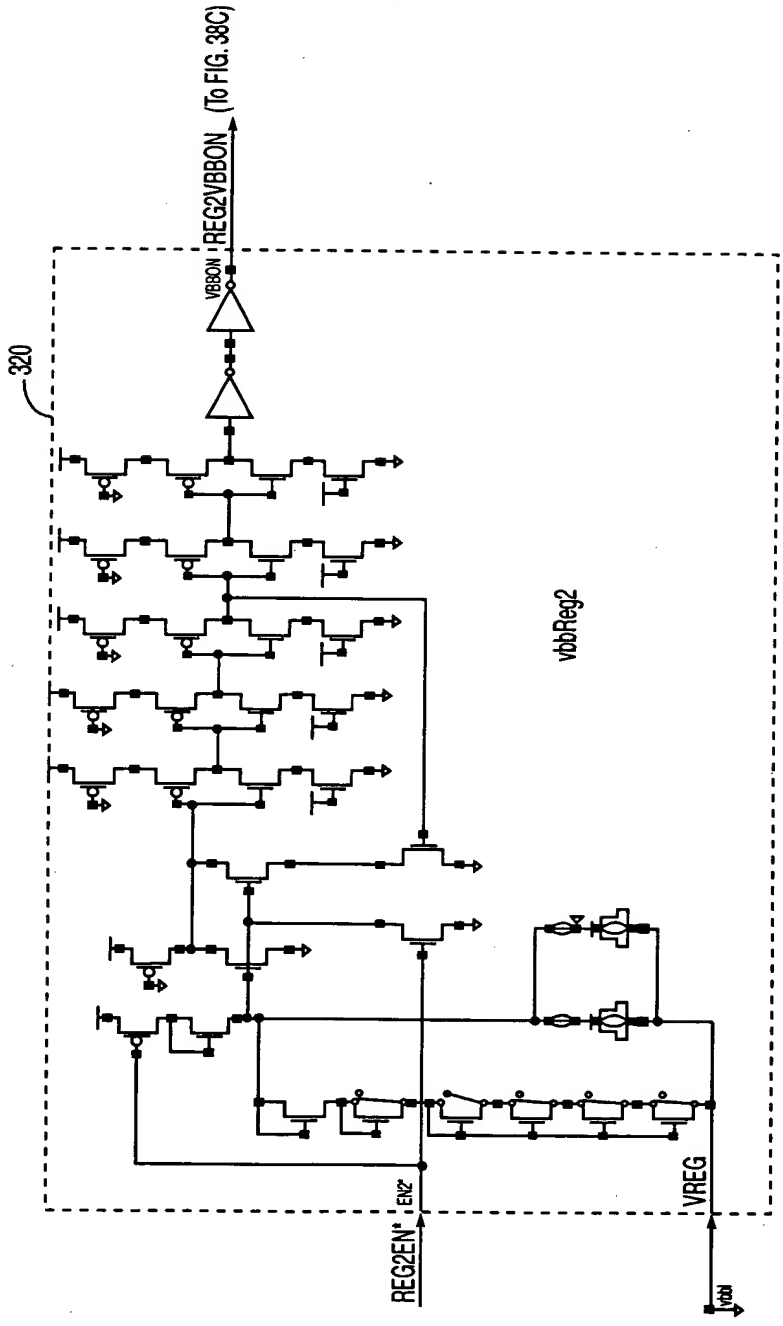


FIG. 38E

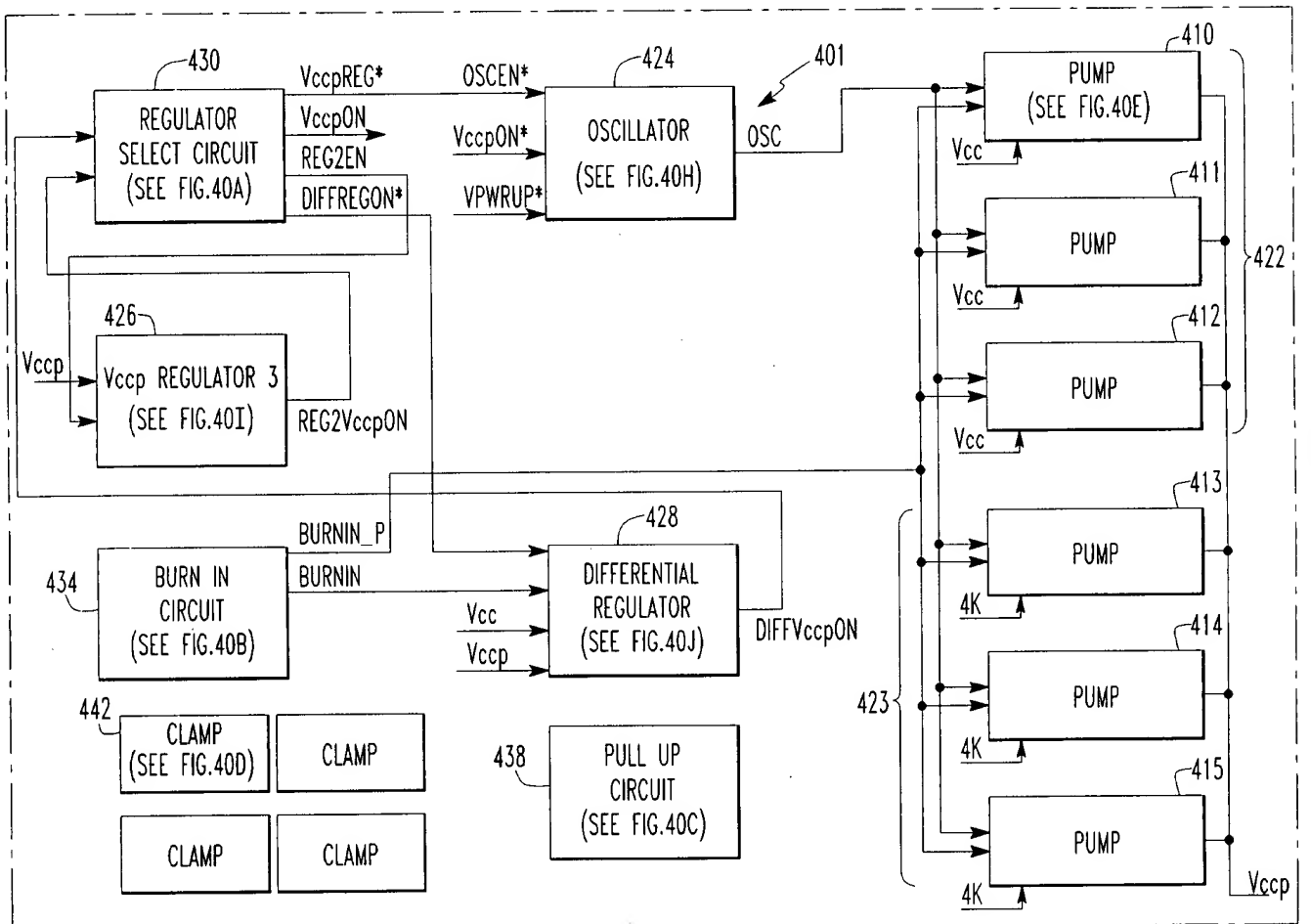

430
REGULATOR SELECT CIRCUIT (SEE FIG.40A)
VccpREG*
VccpON
REG2EN
DIFFREGON*
OSCEN*
VccpON*
VPWRUP*
424
OSCILLATOR (SEE FIG.40H)
OSC
401
410
PUMP (SEE FIG.40E)
411
PUMP
412
PUMP
413
PUMP
414
PUMP
415
PUMP
Vcc
4K
422
423
426
Vccp REGULATOR 3 (SEE FIG.40I)
Vccp
REG2VccpON
428
DIFFERENTIAL REGULATOR (SEE FIG.40J)
DIFFVccpON
BURNIN_P
BURNIN
434
BURN IN CIRCUIT (SEE FIG.40B)
442
CLAMP (SEE FIG.40D)
CLAMP
CLAMP
CLAMP
438
PULL UP CIRCUIT (SEE FIG.40C)
Vccp
400

FIG. 39

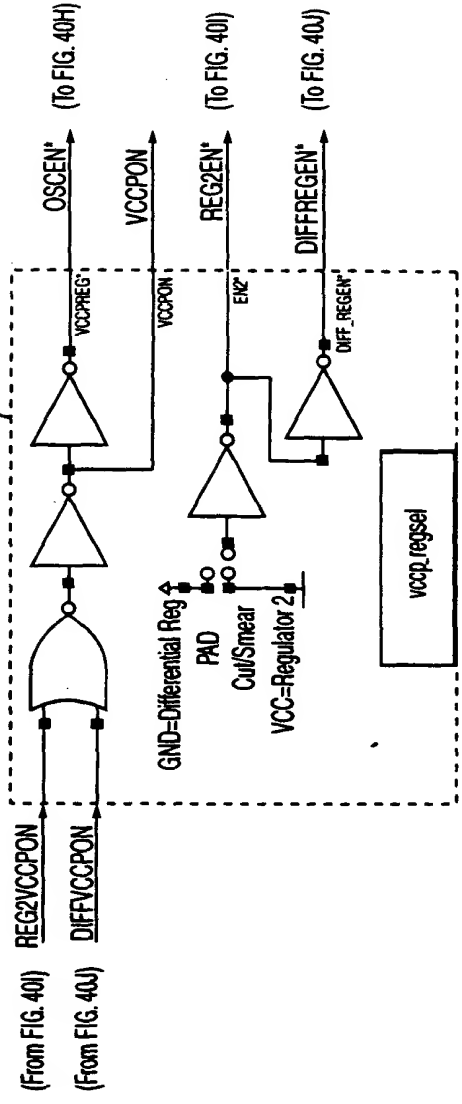

(From FIG. 40I)
(From FIG. 40J)
REG2VCCPON
DIFFVCCPON
430
OSCEN*
(To FIG. 40H)
VCCPON
REG2EN*
(To FIG. 40I)
DIFFREGEN*
(To FIG. 40J)
VCCPREG*
VCCPON
EN2*
DIFF_REGEN*
GND=Differential Reg
PAD
Cut/Smear
VCC=Regulator 2
vccp_regsel

FIG. 40A

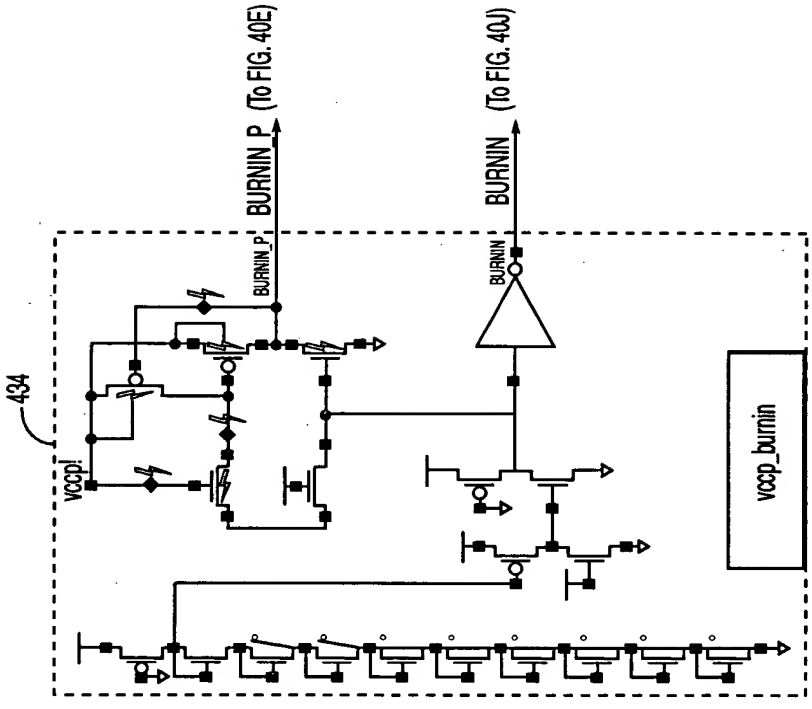

BURNIN_P (To FIG. 40E)
BURNIN (To FIG. 40J)
BURNIN_P
BURNIN
434
vccp
vccp_burnin

FIG. 40B

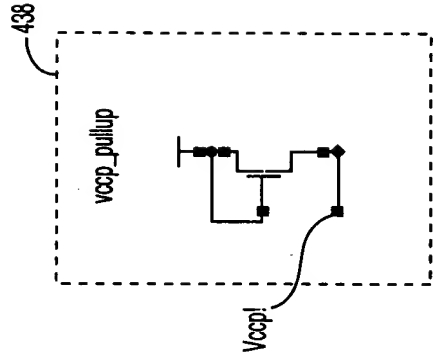


FIG. 40C

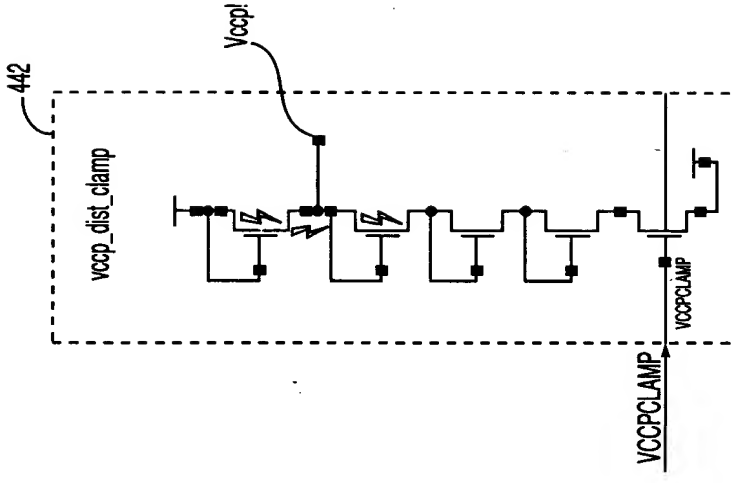


FIG. 40D

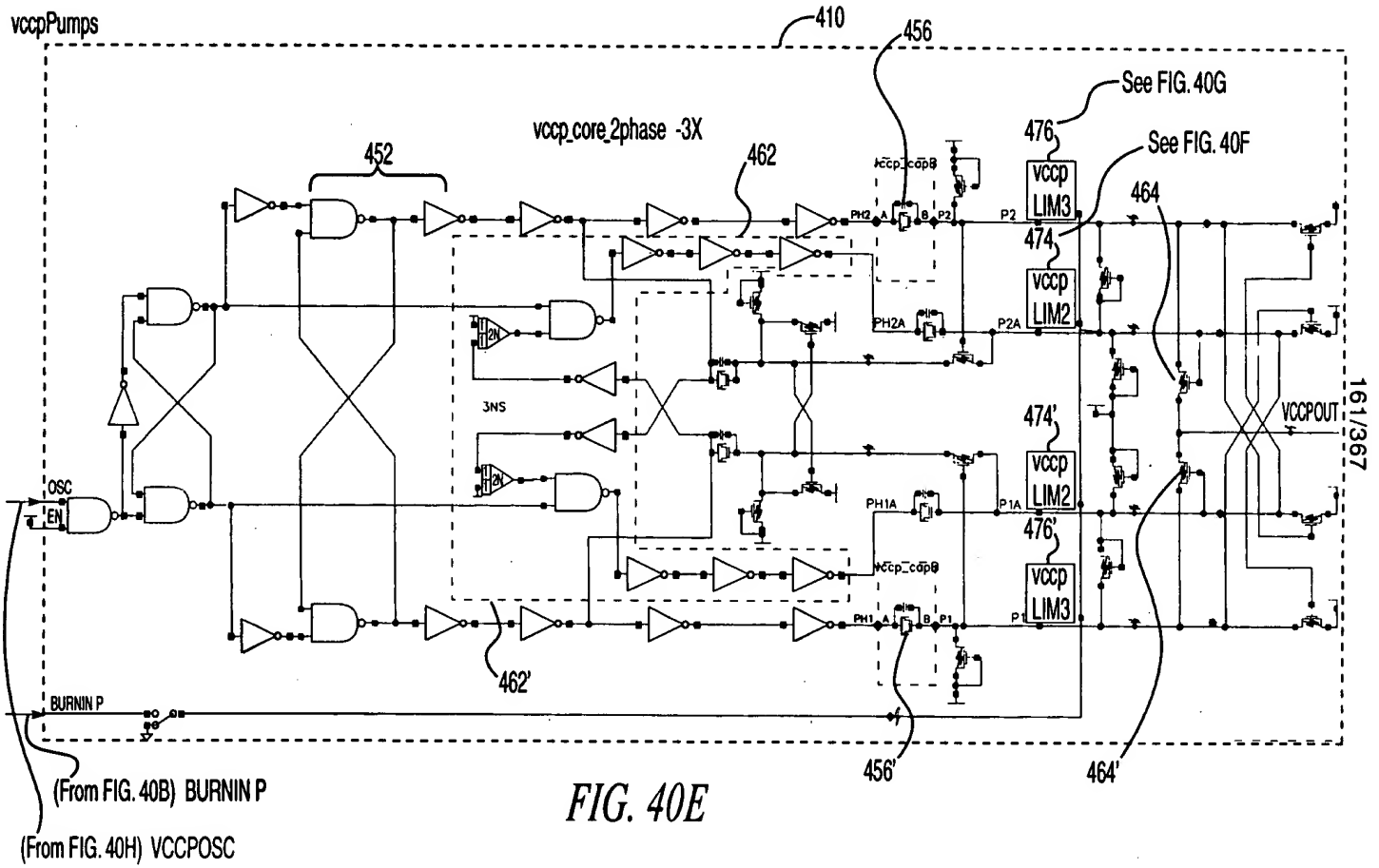

vccpPumps
410
456
See FIG. 40G
vccp_core_2phase -3X
476
See FIG. 40F
452
462
vccp LIM3
464
474
vccp LIM2
474'
vccp LIM2
476'
vccp LIM3
VCCPOUT
161/367
OSC
EN
BURNIN P
462'
456'
464'
(From FIG. 40B) BURNIN P
(From FIG. 40H) VCCPOSC

FIG. 40E

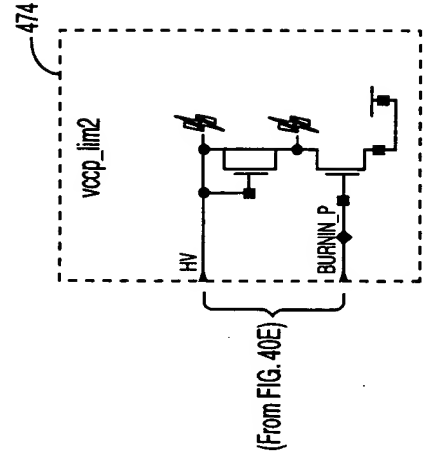


FIG. 40F

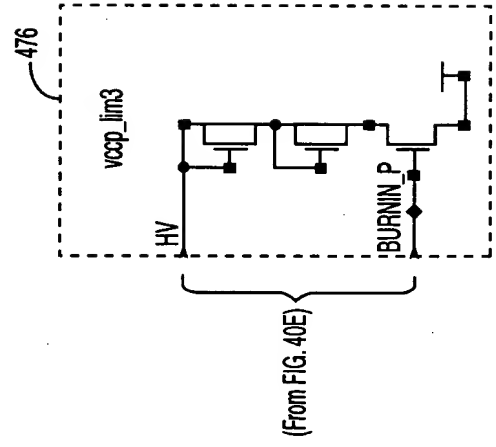


FIG. 40G

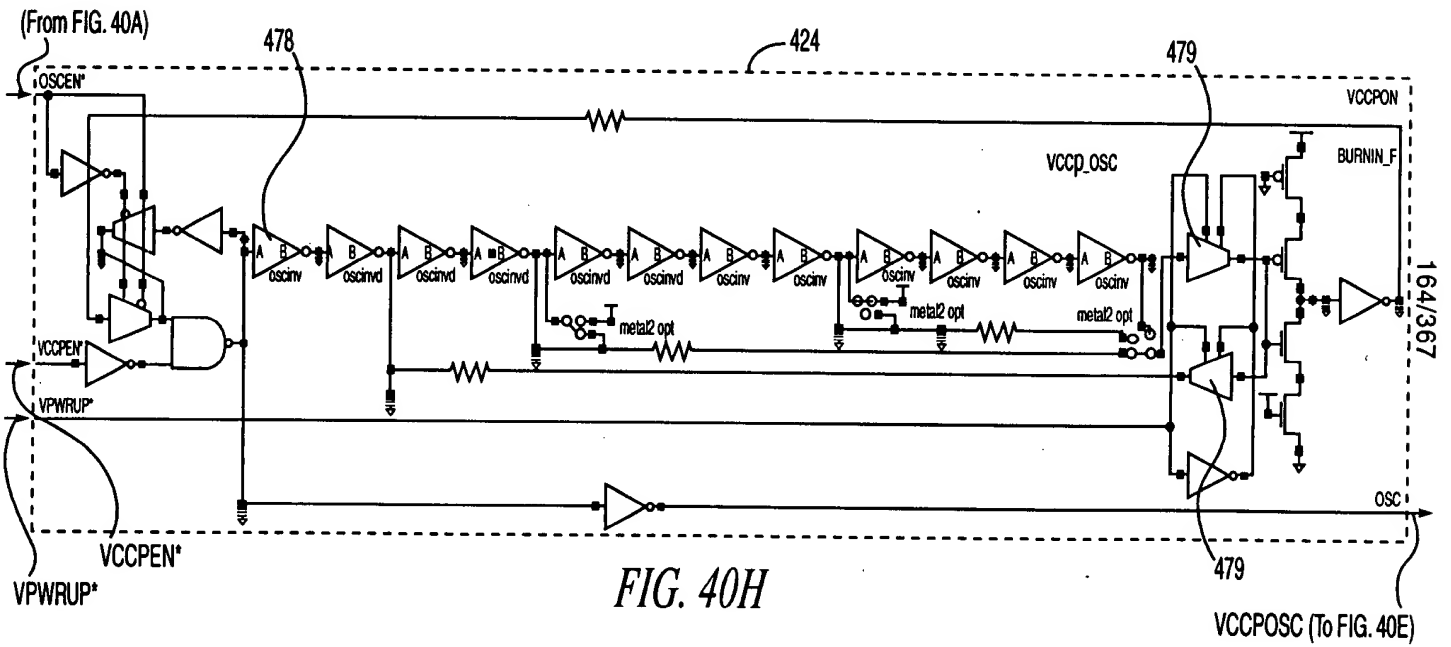

(From FIG. 40A)
478
424
479
OSCEN*
VCCPON
VCCP_OSC
BURNIN_F
oscinv
oscinvd
metal2 opt
VCCPEN*
VPWRUP*
OSC
164/367
VCCPEN*
VPWRUP*
479
VCCPOSC (To FIG. 40E)

FIG. 40H

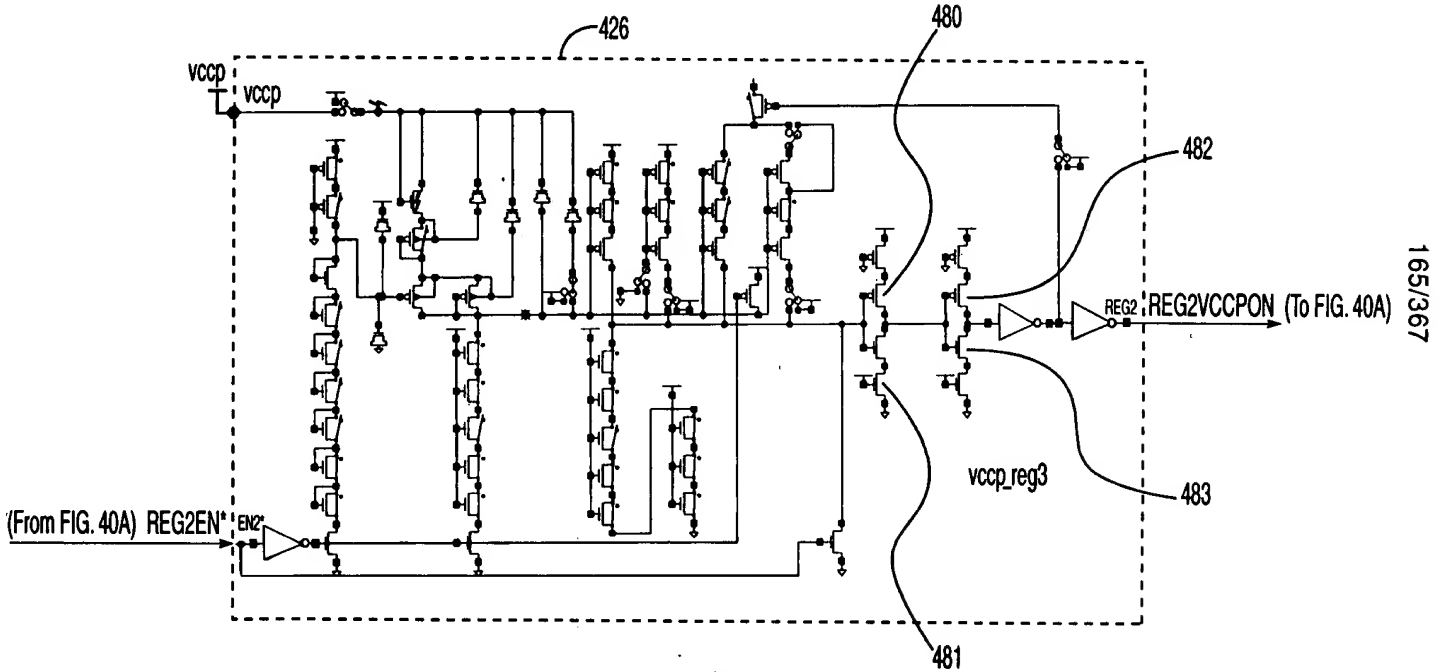

426
480
vccp
vccp
482
REG2
REG2VCCPON (To FIG. 40A)
vccp_reg3
483
(From FIG. 40A) REG2EN*
EN2*
481

FIG. 40I

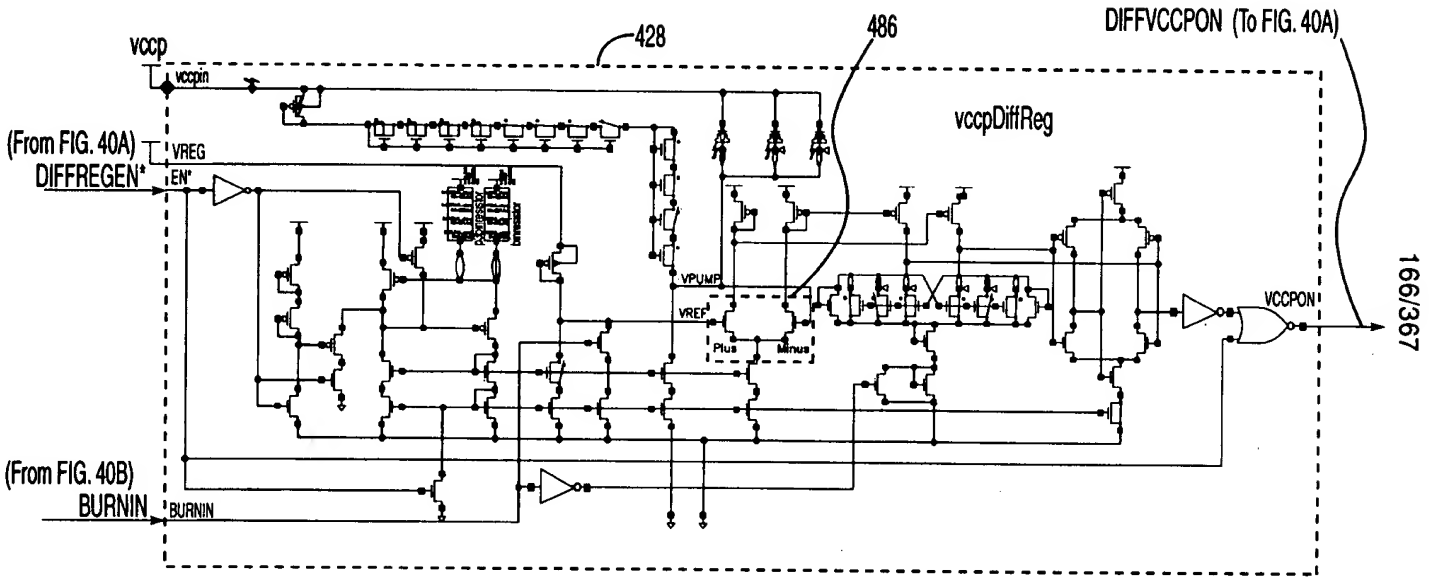

vccp
428
486
DIFFVCCPON (To FIG. 40A)
vccpin
vccpDiffReg
(From FIG. 40A)
DIFFREGEN*
VREG
EN*
VPUMP
VREF
Plus
Minus
VCCPON
166/367
(From FIG. 40B)
BURNIN
BURNIN

FIG. 40J

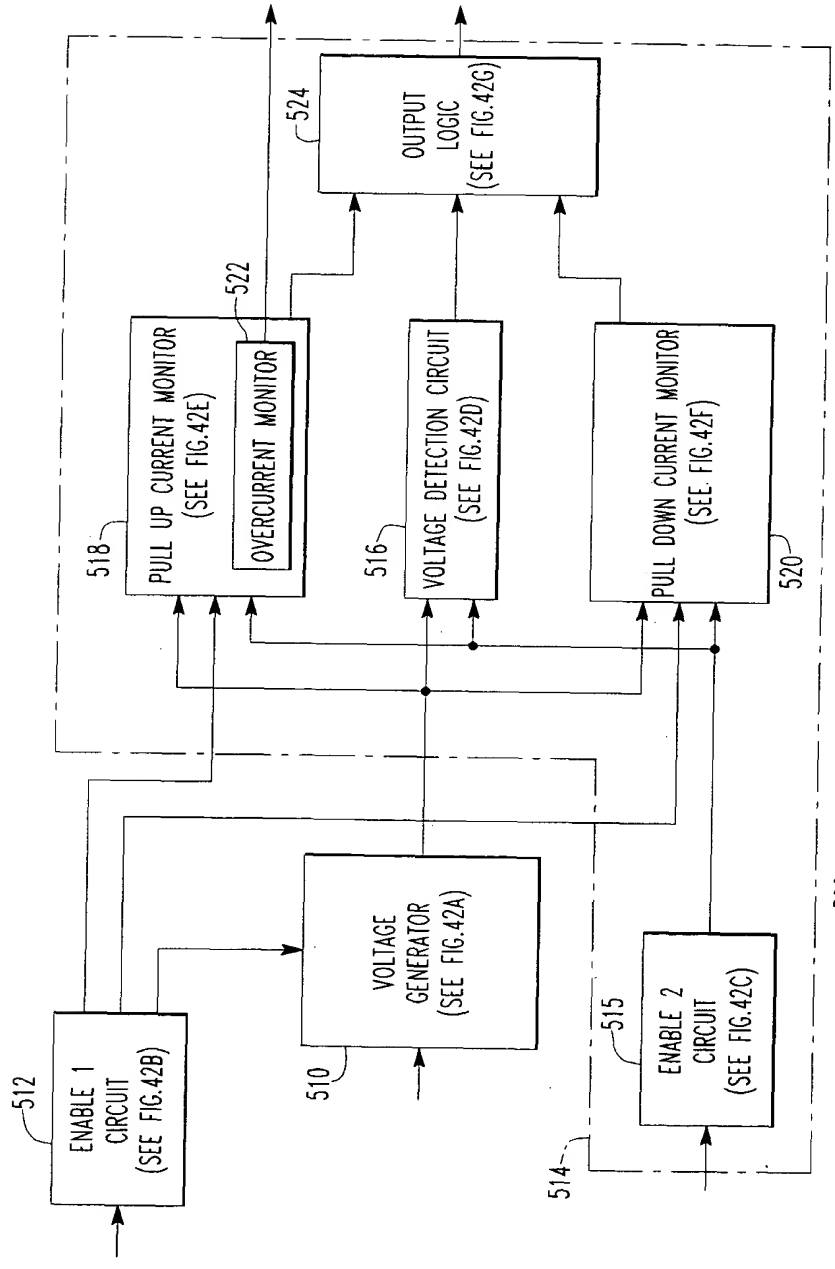

500
512
ENABLE 1 CIRCUIT (SEE FIG.42B)
510
VOLTAGE GENERATOR (SEE FIG.42A)
514
515
ENABLE 2 CIRCUIT (SEE FIG.42C)
518
PULL UP CURRENT MONITOR (SEE FIG.42E)
522
OVERCURRENT MONITOR
516
VOLTAGE DETECTION CIRCUIT (SEE FIG.42D)
520
PULL DOWN CURRENT MONITOR (SEE FIG.42F)
524
OUTPUT LOGIC (SEE FIG.42G)

FIG. 41

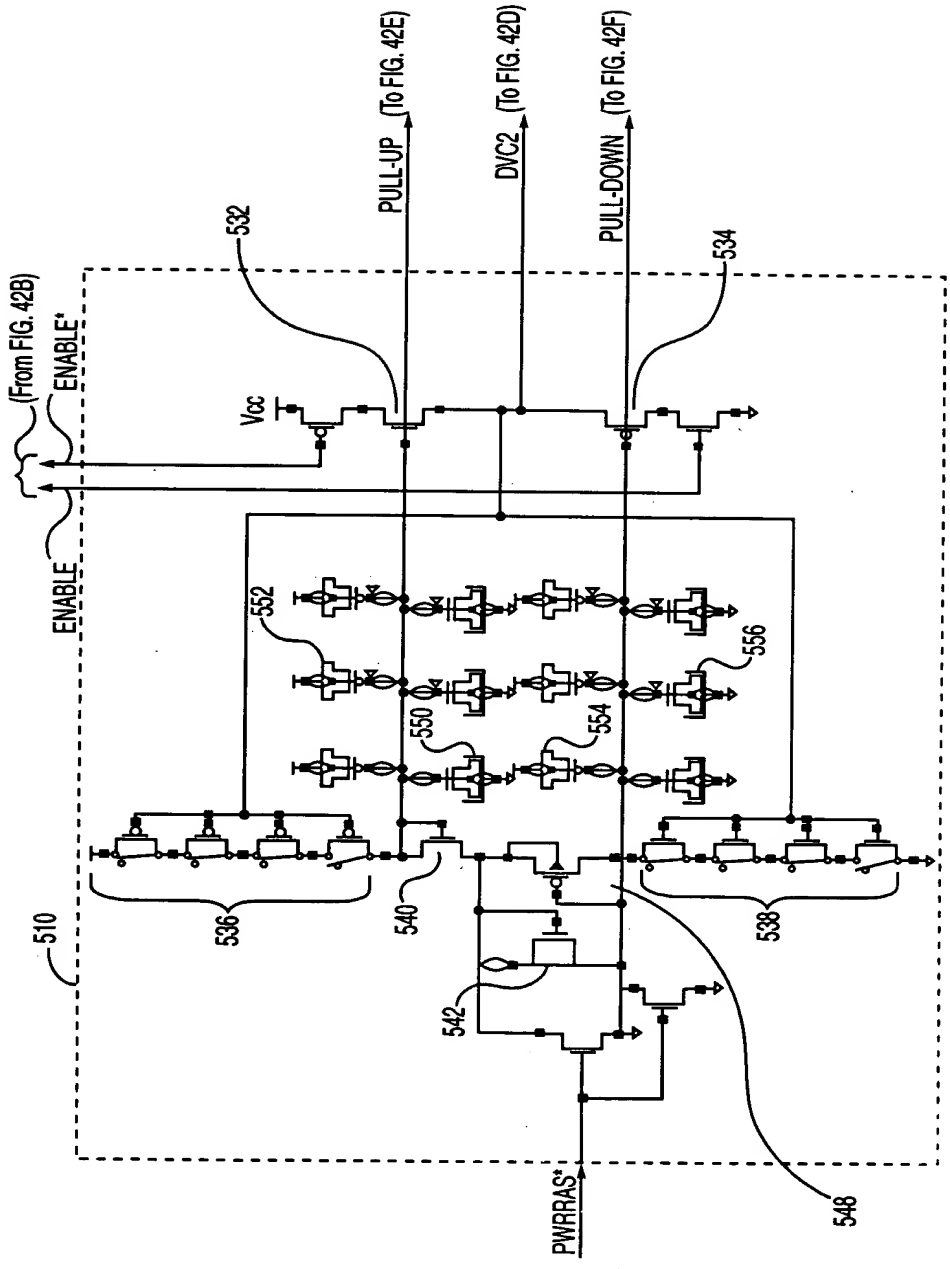

(From FIG. 42B)
ENABLE'
ENABLE
Vcc
532
PULL-UP (To FIG. 42E)
DVC2 (To FIG. 42D)
PULL-DOWN (To FIG. 42F)
534
552
556
550
554
510
536
540
538
542
548
PWRRAS'

FIG. 42A

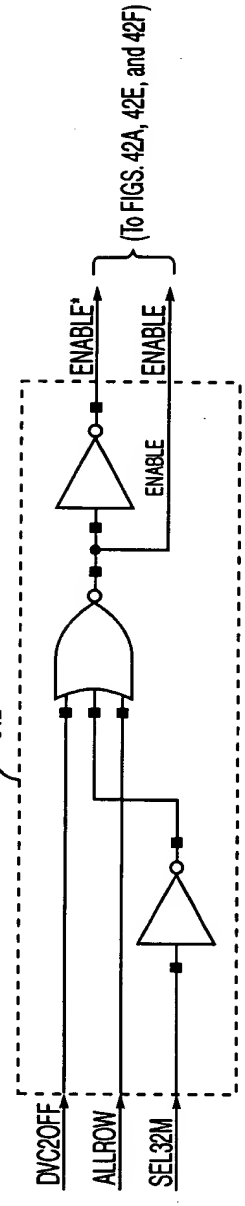

(To FIGS. 42A, 42E, and 42F)
ENABLE'
ENABLE
ENABLE
512
DVC2OFF
ALLROW
SEL32M

FIG. 42B

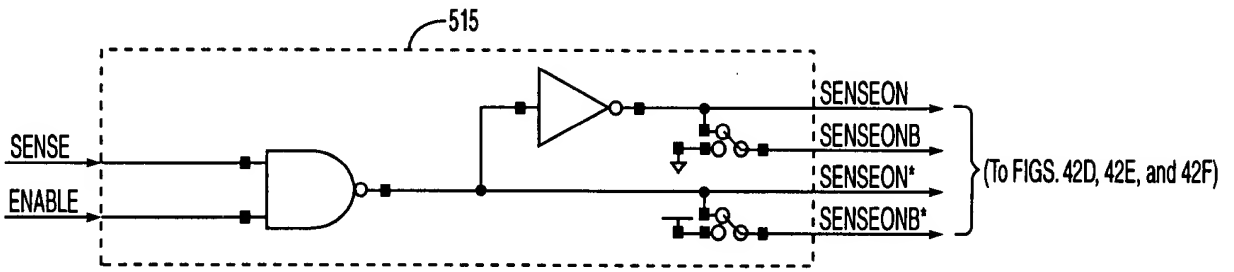

515
SENSE
ENABLE
SENSEON
SENSEONB
SENSEON*
SENSEONB*
(To FIGS. 42D, 42E, and 42F)

FIG. 42C

P0660-8251P0660

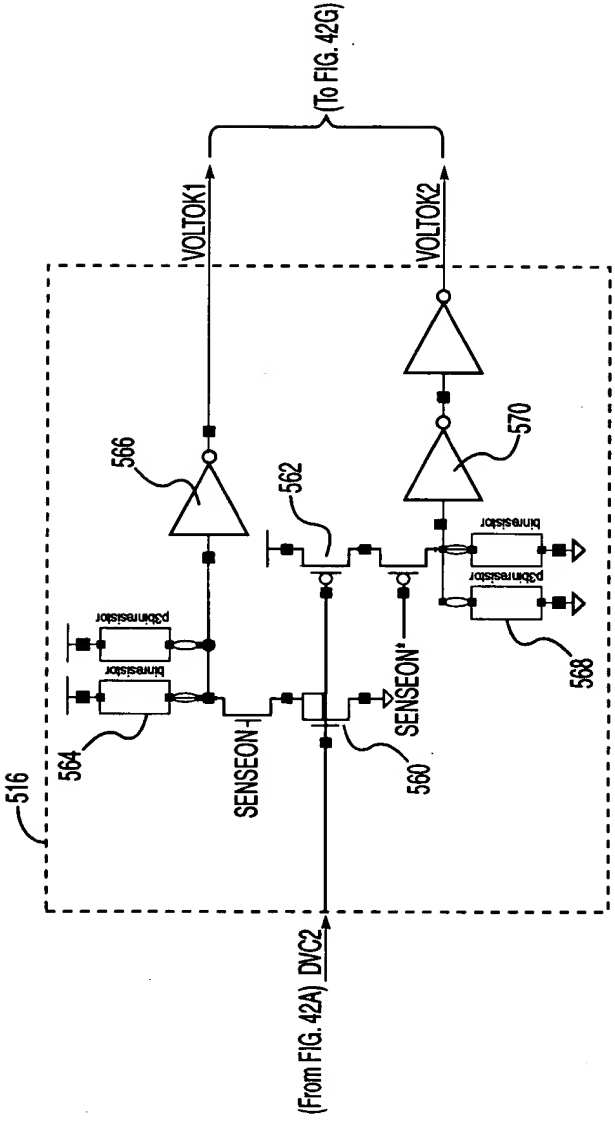


FIG. 42D

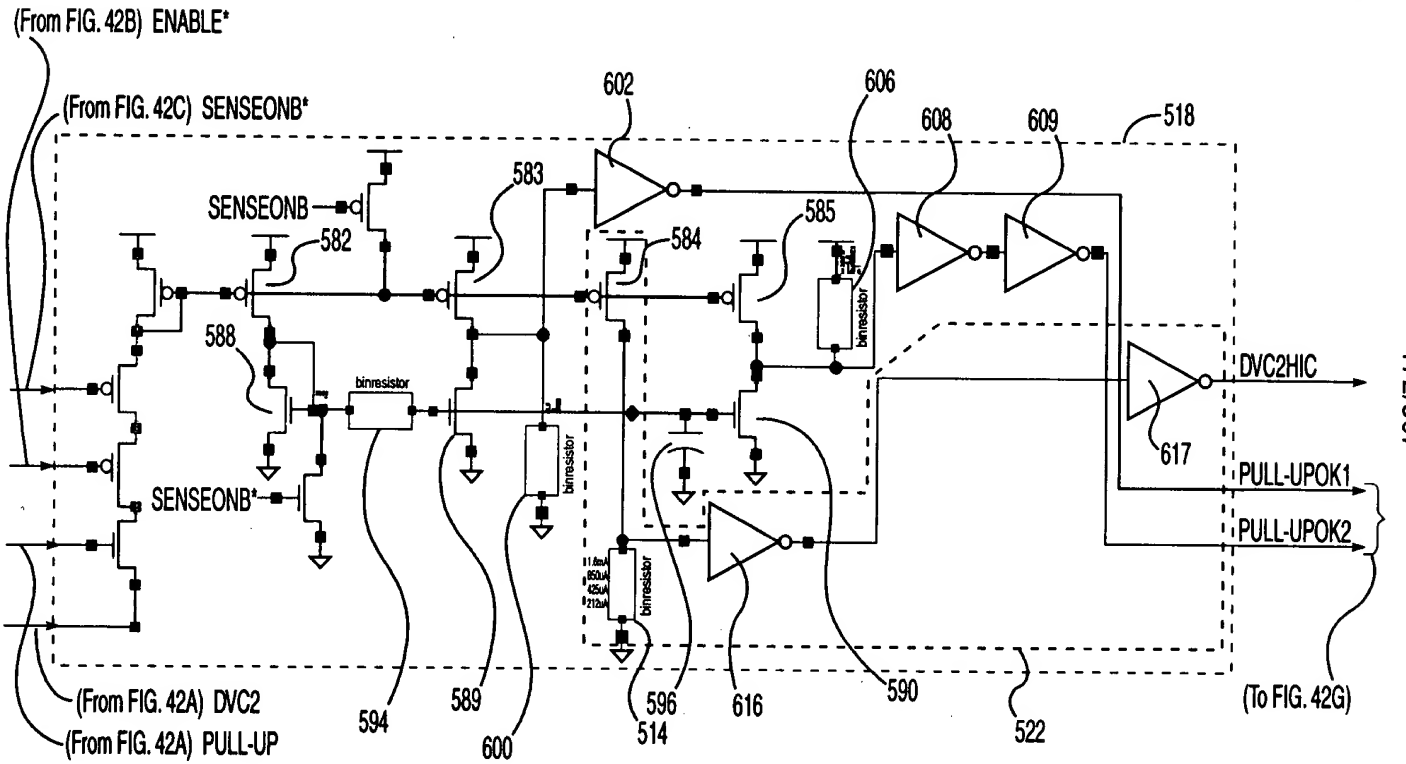

(From FIG. 42B) ENABLE*
(From FIG. 42C) SENSEONB*
602
606
608
609
518
583
585
584
582
SENSEONB
588
binresistor
SENSEONB*
DVC2HIC
617
PULL-UPOK1
PULL-UPOK2
(From FIG. 42A) DVC2
(From FIG. 42A) PULL-UP
594
589
600
596
514
616
590
522
(To FIG. 42G)

FIG. 42E

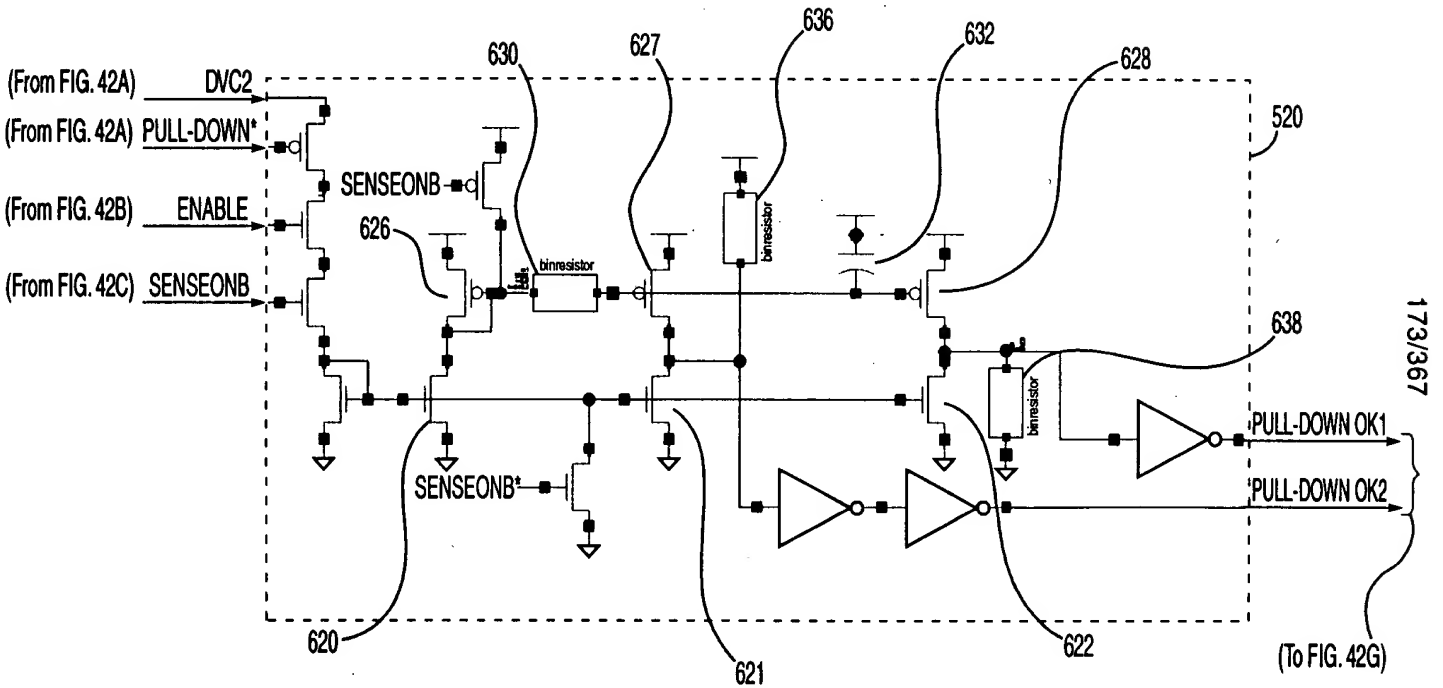

(From FIG. 42A) DVC2
(From FIG. 42A) PULL-DOWN*
(From FIG. 42B) ENABLE
(From FIG. 42C) SENSEONB
SENSEONB
SENSEONB*
626
630
627
636
632
628
520
638
binresistor
PULL-DOWN OK1
PULL-DOWN OK2
620
621
622
(To FIG. 42G)
173/367

FIG. 42F

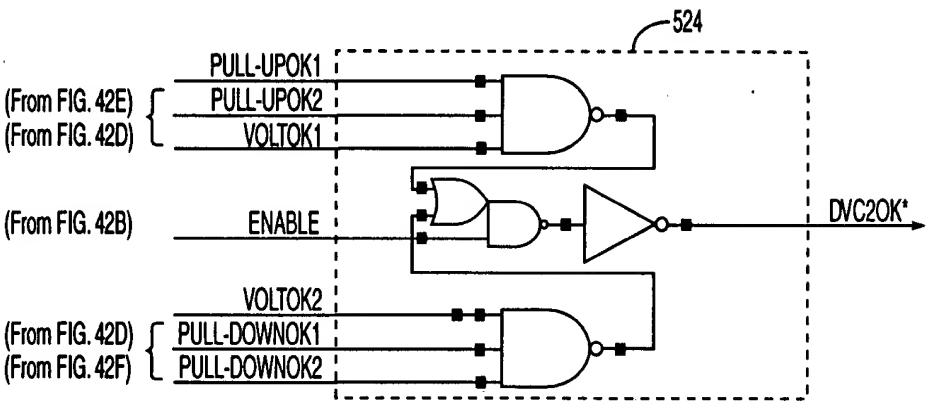

524
PULL-UPOK1
(From FIG. 42E)
PULL-UPOK2
(From FIG. 42D)
VOLTOK1
(From FIG. 42B)
ENABLE
DVC2OK*
VOLTOK2
(From FIG. 42D)
PULL-DOWNOK1
(From FIG. 42F)
PULL-DOWNOK2

FIG. 42G

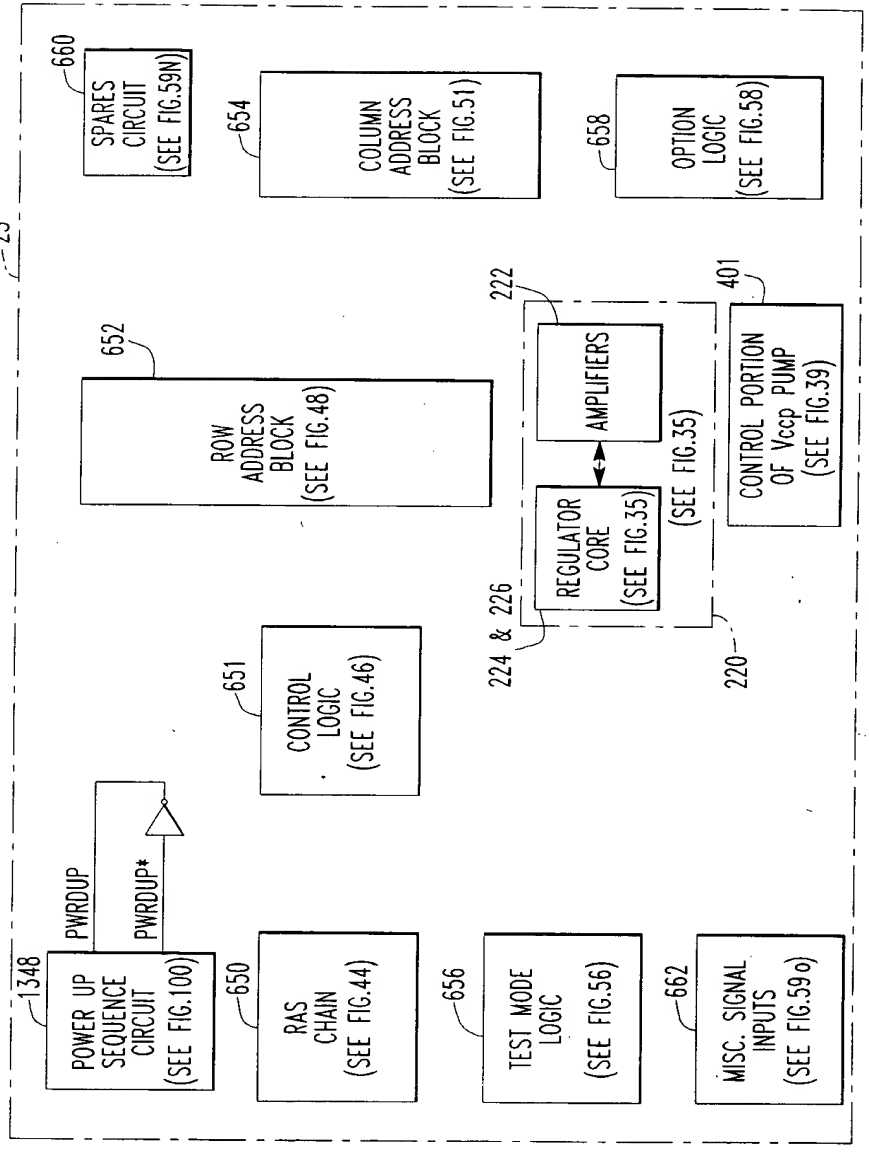

23
1348
POWER UP SEQUENCE CIRCUIT (SEE FIG.100)
PWRDUP
PWRDUP*
650
RAS CHAIN (SEE FIG.44)
656
TEST MODE LOGIC (SEE FIG.56)
662
MISC. SIGNAL INPUTS (SEE FIG.59o)
651
CONTROL LOGIC (SEE FIG.46)
652
ROW ADDRESS BLOCK (SEE FIG.48)
660
SPARES CIRCUIT (SEE FIG.59N)
654
COLUMN ADDRESS BLOCK (SEE FIG.51)
658
OPTION LOGIC (SEE FIG.58)
222
AMPLIFIERS
224 & 226
REGULATOR CORE (SEE FIG.35)
(SEE FIG.35)
220
401
CONTROL PORTION OF Vccp PUMP (SEE FIG.39)

FIG. 43

TOSOED"8251086O

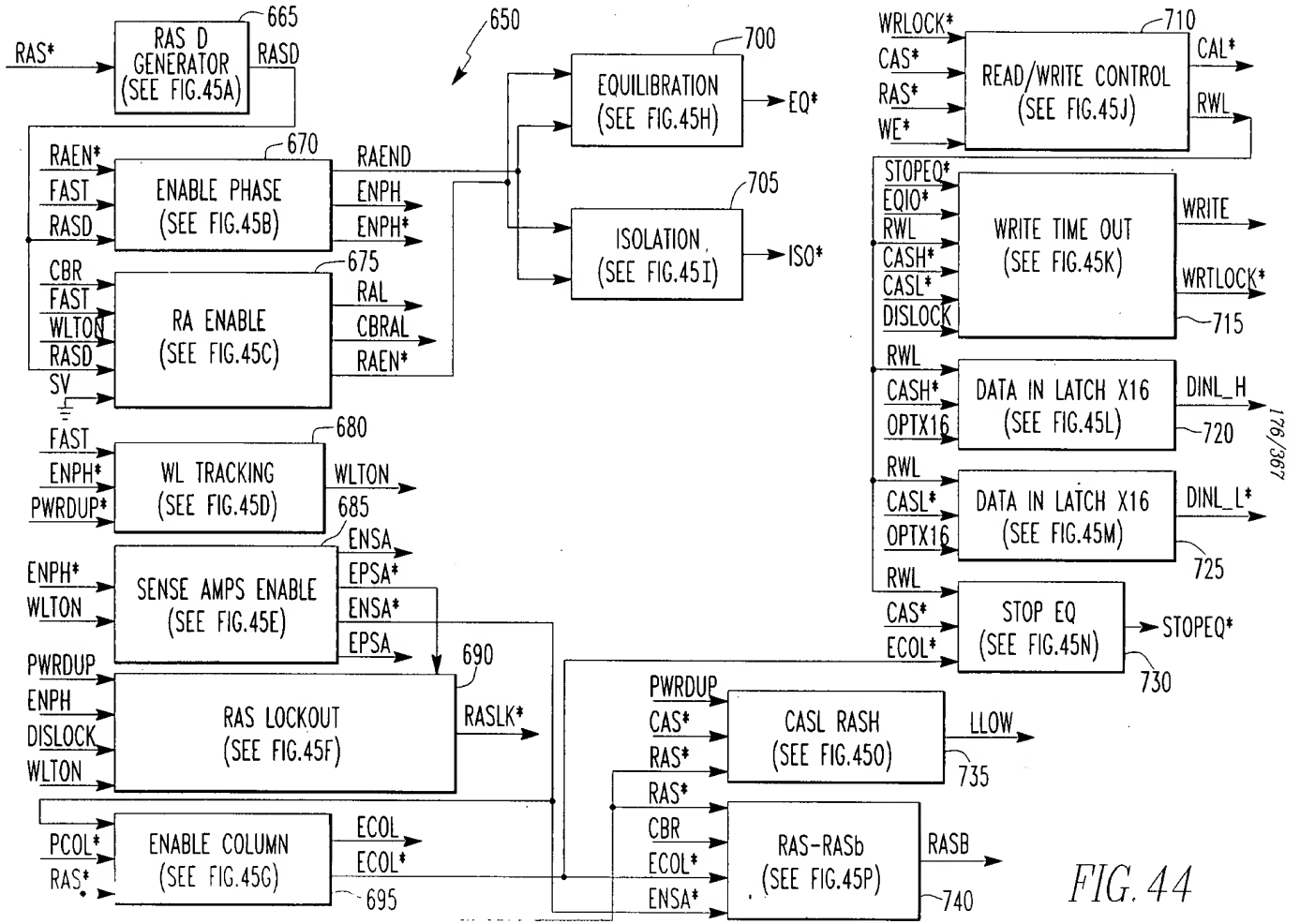


FIG. 44

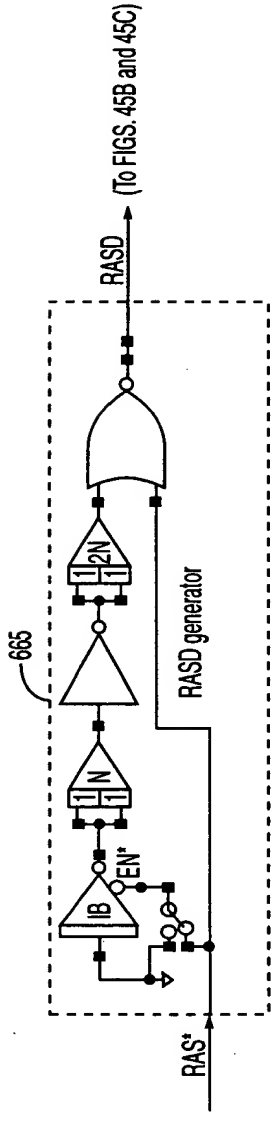


FIG. 45A

T080820 82970860

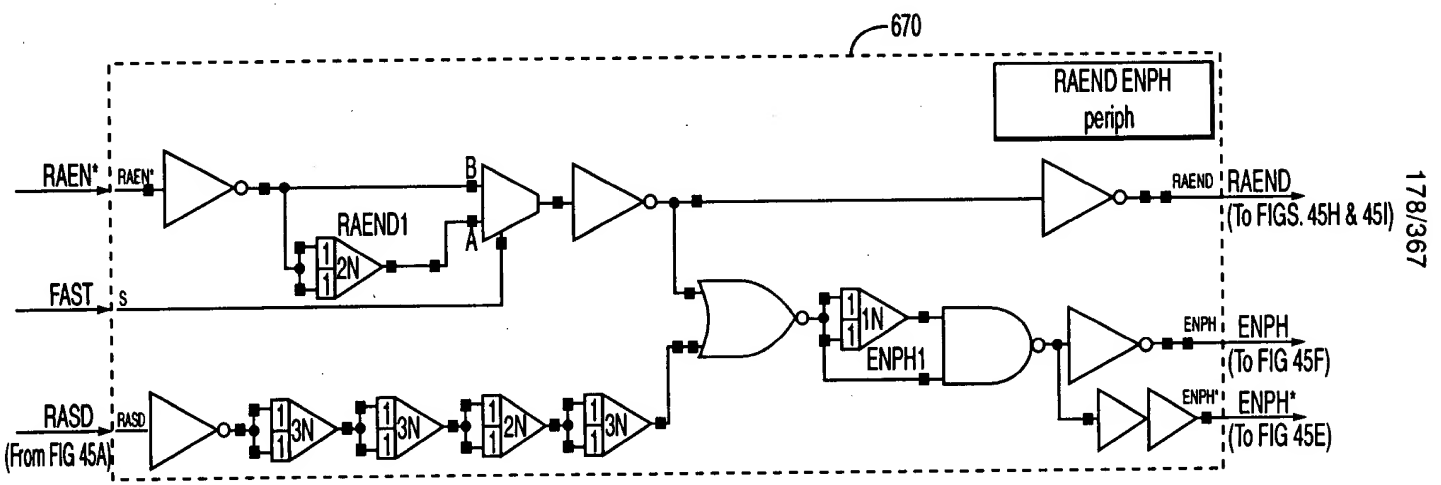


FIG. 45B

FOREIGN PATENT DOCUMENT

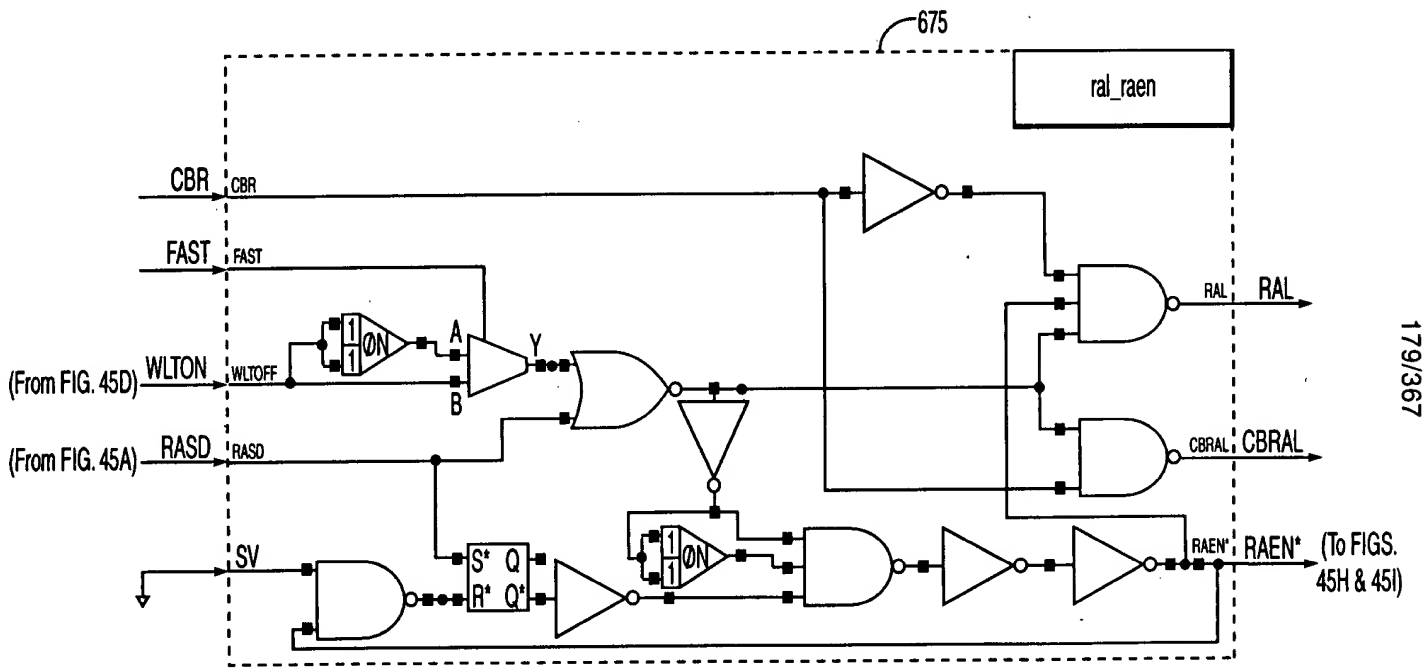


FIG. 45C

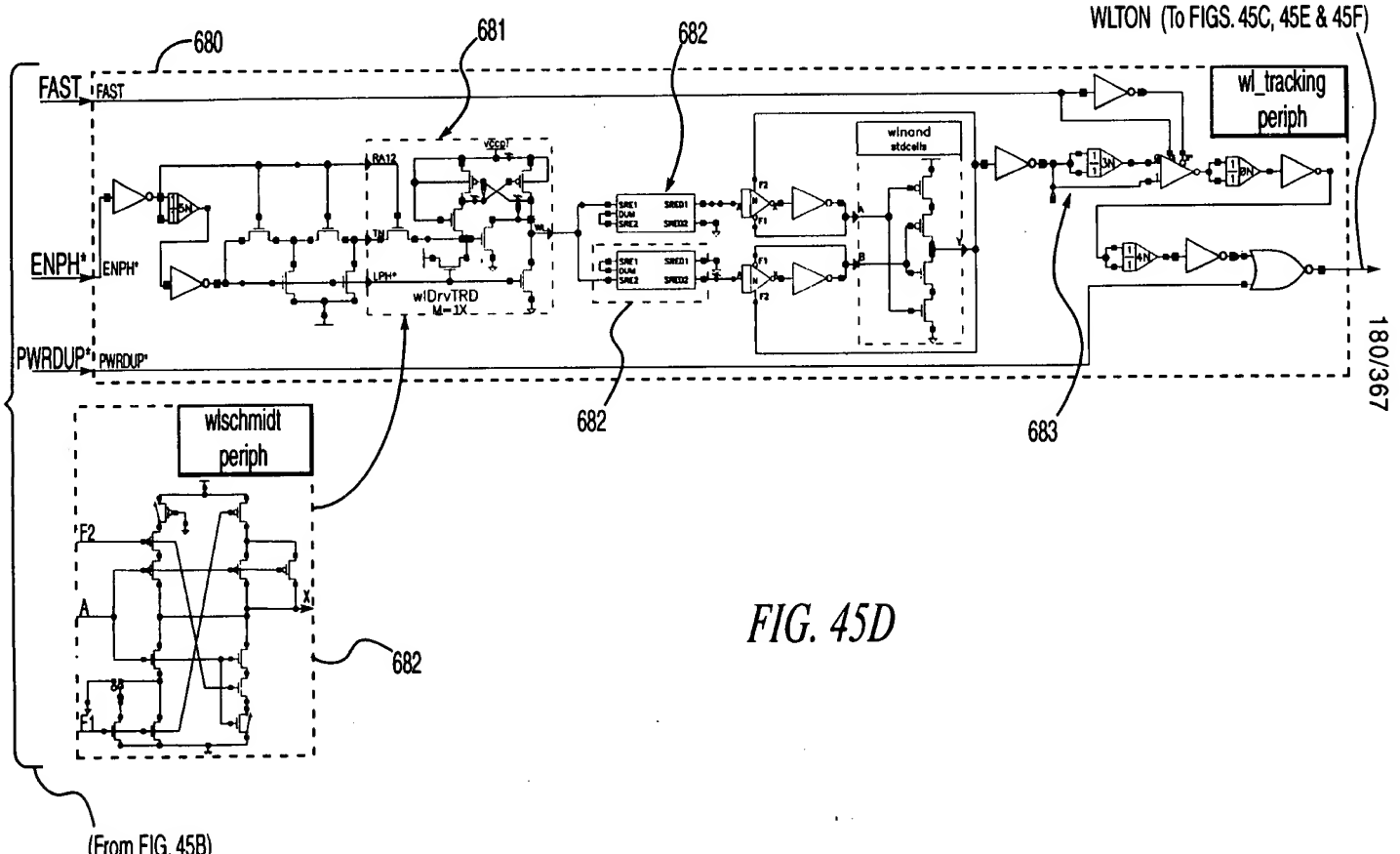

680
681
682
WLTON (To FIGS. 45C, 45E & 45F)
FAST
FAST
wl_tracking periph
ENPH*
ENPH*
PWRDUP*
PWRDUP*
RA12
LPH*
wlDrvTRD
M=1X
winand stdcells
wlschmidt periph
F2
A
F1
682
682
683
(From FIG. 45B)

FIG. 45D

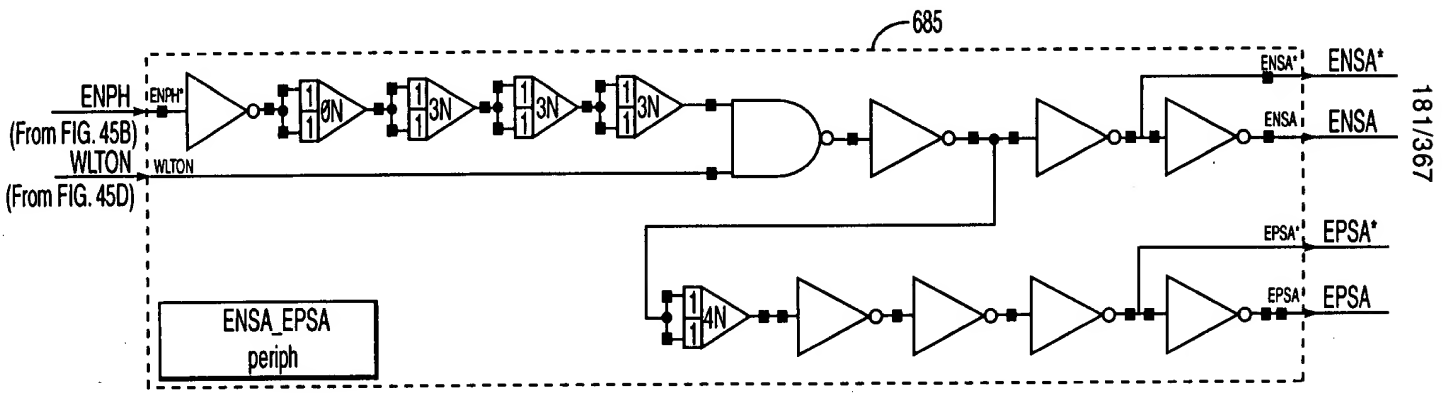

685
ENPH
(From FIG. 45B)
WLTON
(From FIG. 45D)
ENPH*
WLTON
ØN
3N
3N
3N
4N
ENSA*
ENSA
ENSA*
ENSA
EPSA*
EPSA
EPSA*
EPSA
ENSA_EPSA
periph

FIG. 45E

T08020 "8291866

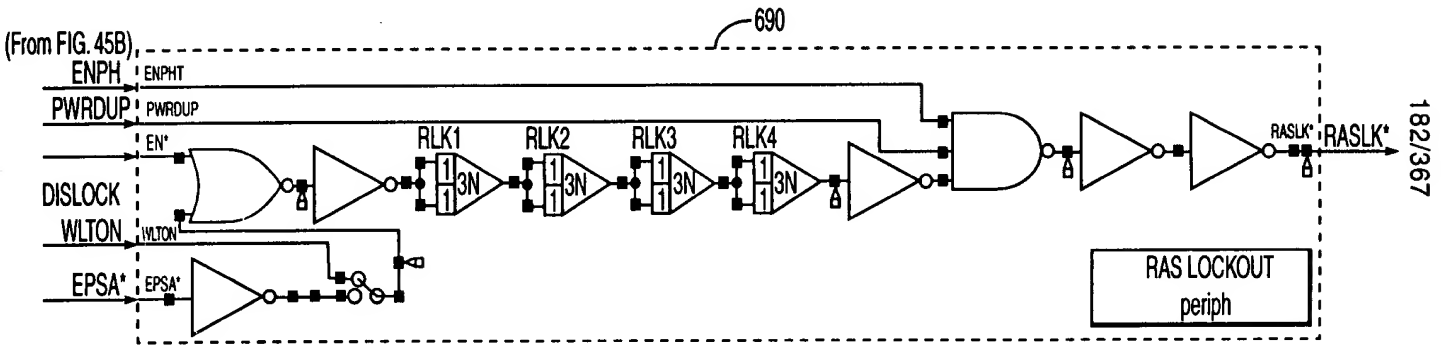


FIG. 45F

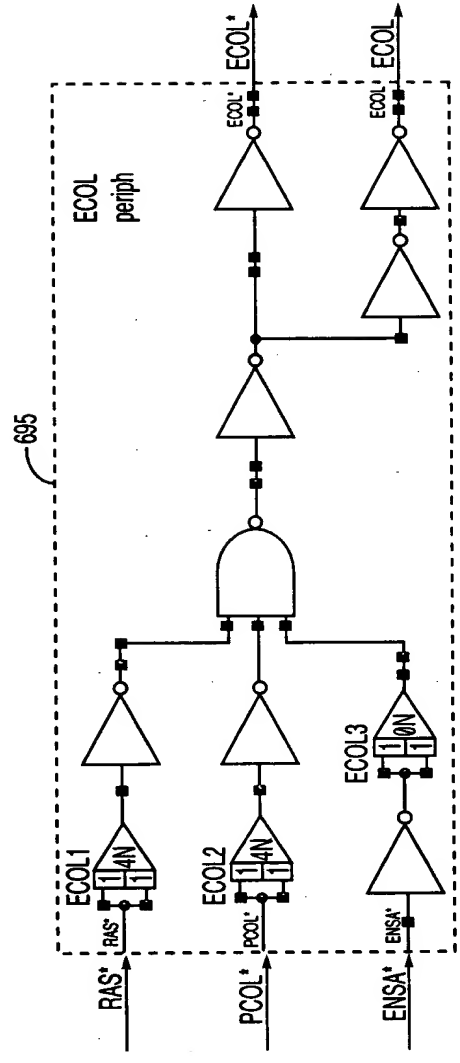

695
ECOL
periph
ECOL1
ECOL2
ECOL3
4N
0N
RAS'
PCOL'
ENSA'
ECOL'
ECOL

FIG. 45G

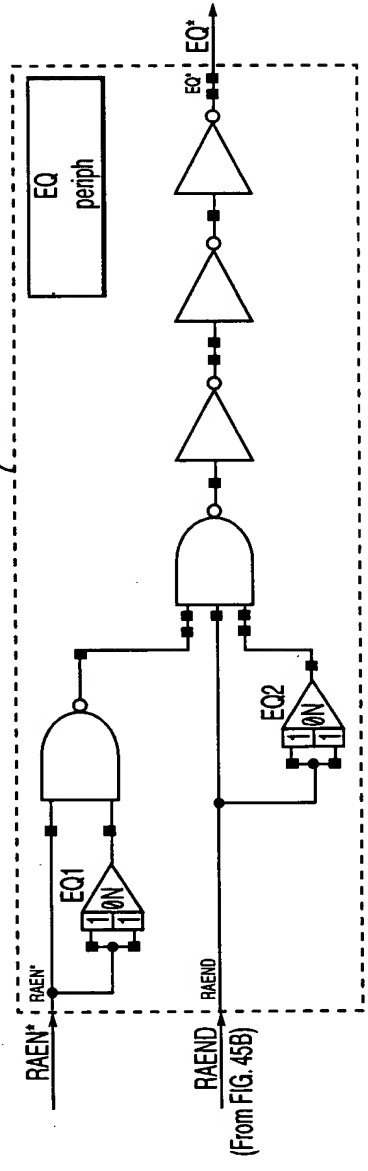

700
EQ periph
EQ*
EQ'
EQ1
EQ2
ØN
RAEN'
RAEND
RAEN'
RAEND
(From FIG. 45B)

FIG. 45H

FOCUS "85TC050"

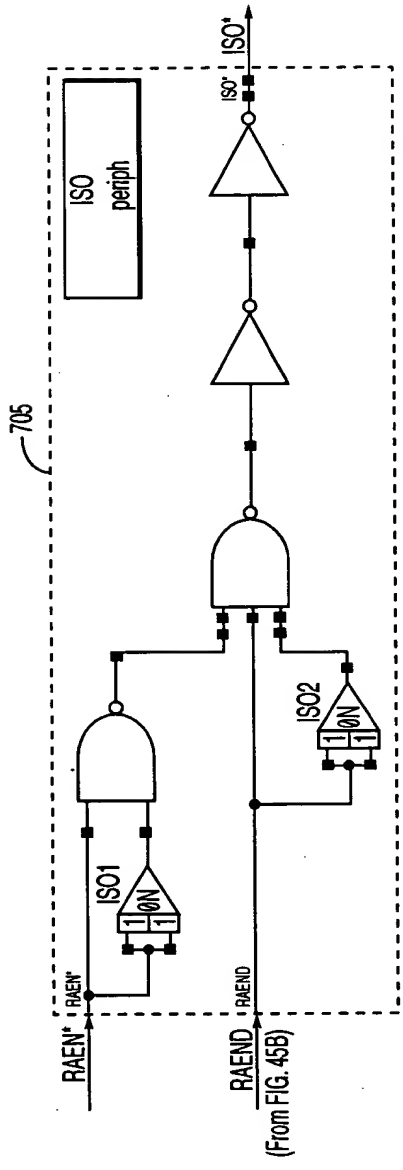


FIG. 45I

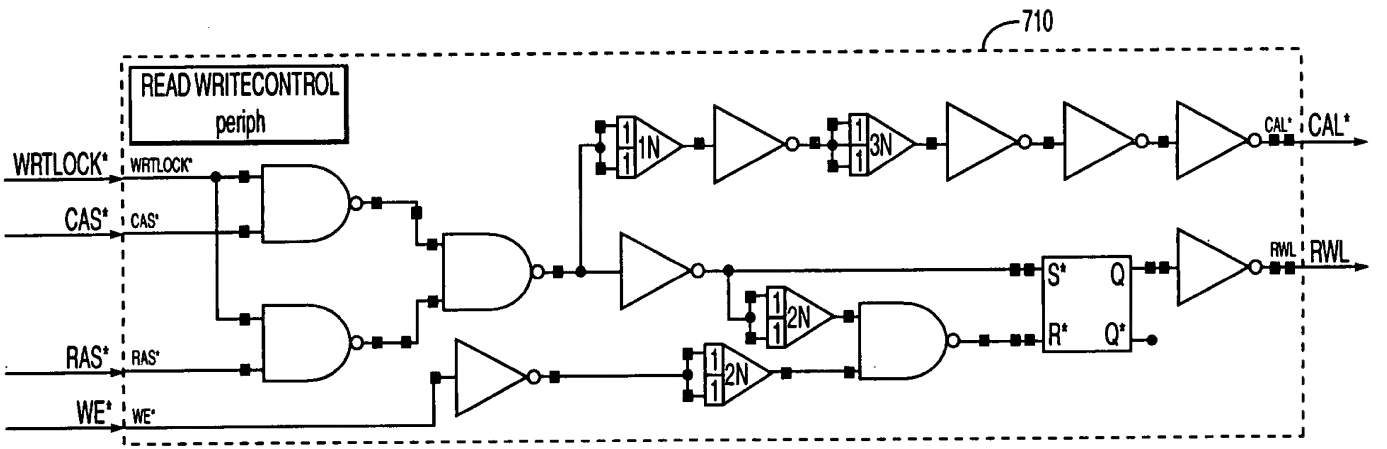

710
READ WRITECONTROL
periph
WRTLOCK*
CAS*
RAS*
WE*
WRTLOCK*
CAS*
RAS*
WE*
1N
3N
2N
2N
S*
Q
R*
Q*
CAL*
CAL*
RWL
RWL

FIG. 45J

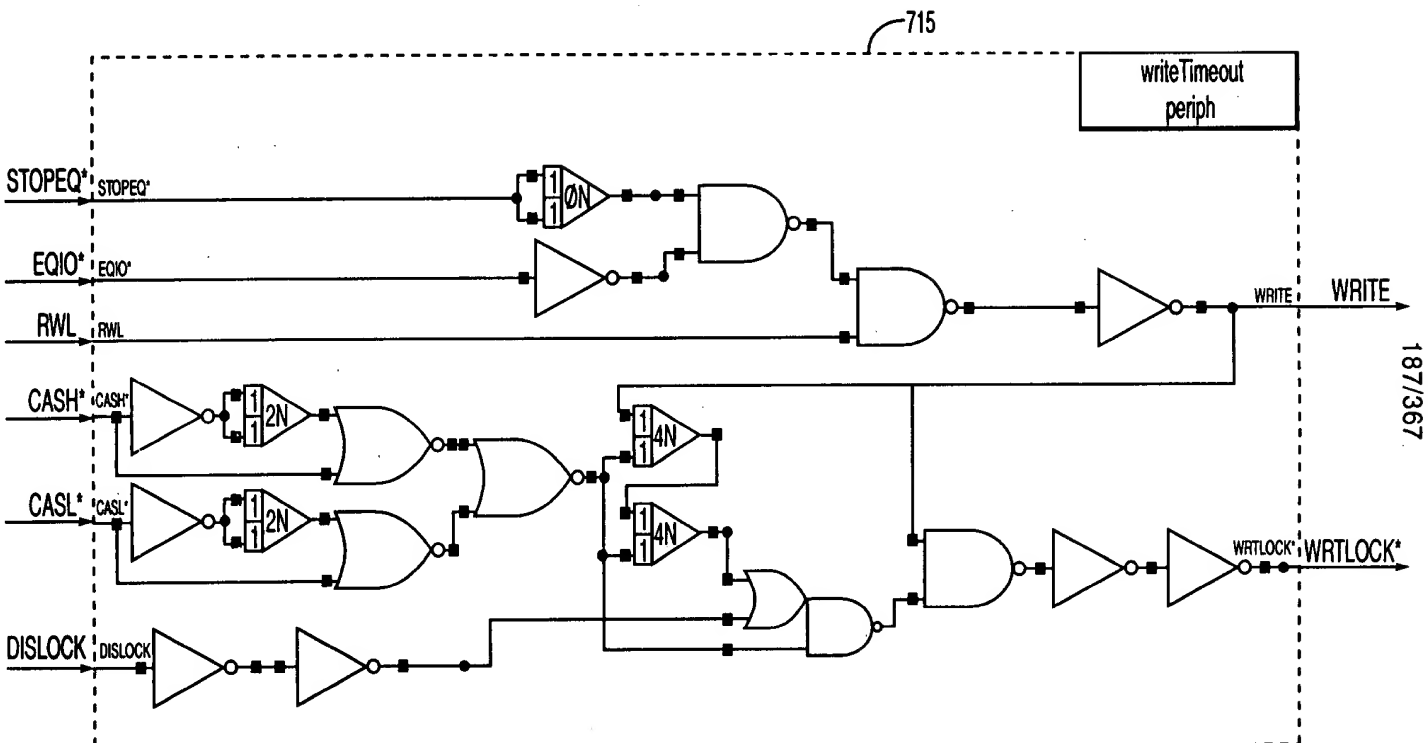

715
writeTimeout
periph
STOPEQ*
STOPEQ*
EQIO*
EQIO*
RWL
RWL
CASH*
CASH*
CASL*
CASL*
DISLOCK
DISLOCK
ØN
2N
2N
4N
4N
WRITE
WRITE
WRTLOCK*
WRTLOCK*

FIG. 45K

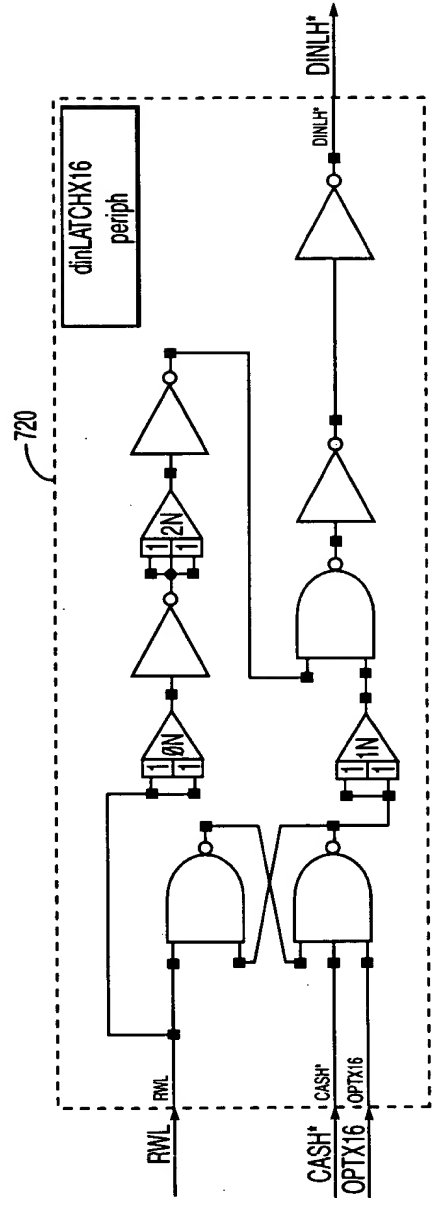

720
dinLATCHX16
periph
DINLH'
DINLH'
2N
ØN
1N
RWL
RWL
CASH'
CASH'
OPTX16
OPTX16

FIG. 45L

T0800" 6234268

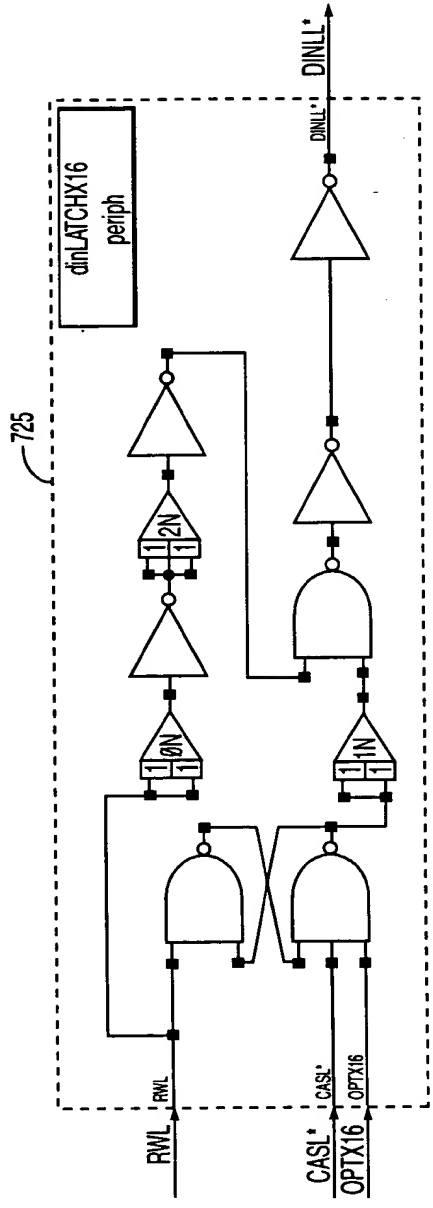


FIG. 45M

1998"8"25"0350

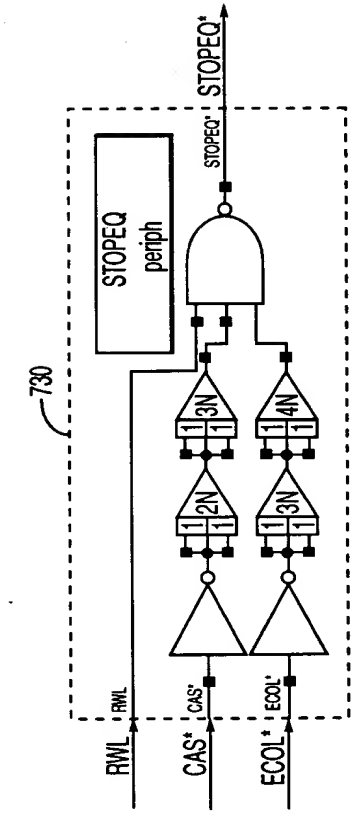


FIG. 45N

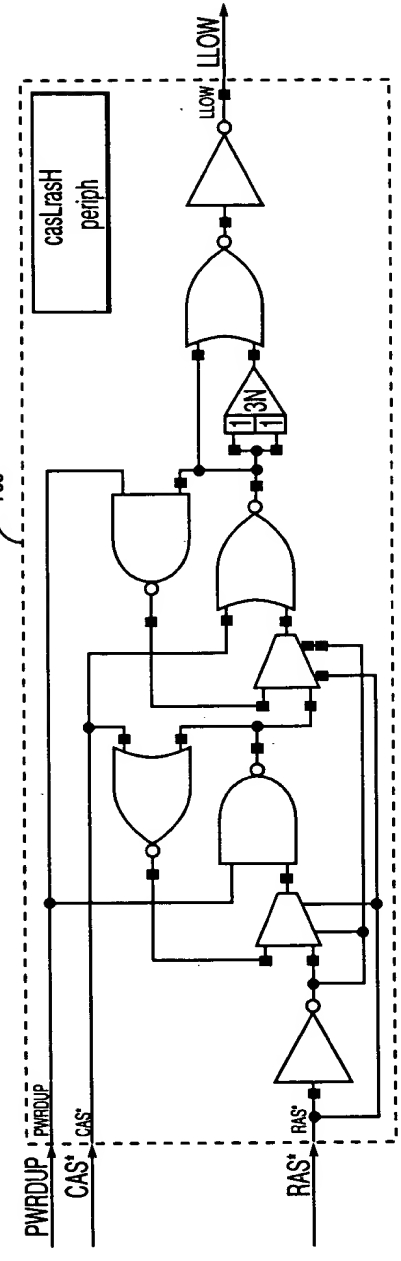

LLOW
LLOW'
casLrasH
periph
735
3N
PWRDUP
CAS*
RAS*
PWRDUP'
CAS*'
RAS*'

FIG. 450

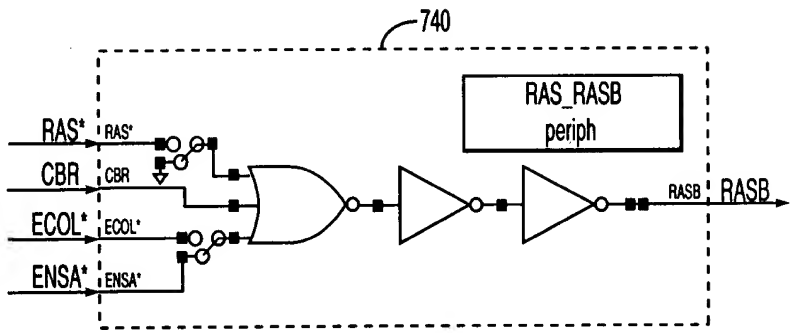

740
RAS_RASB
periph
RAS*
RAS*
CBR
CBR
ECOL*
ECOL*
ENSA*
ENSA*
RASB
RASB

FIG. 45P

T08020 "82570860

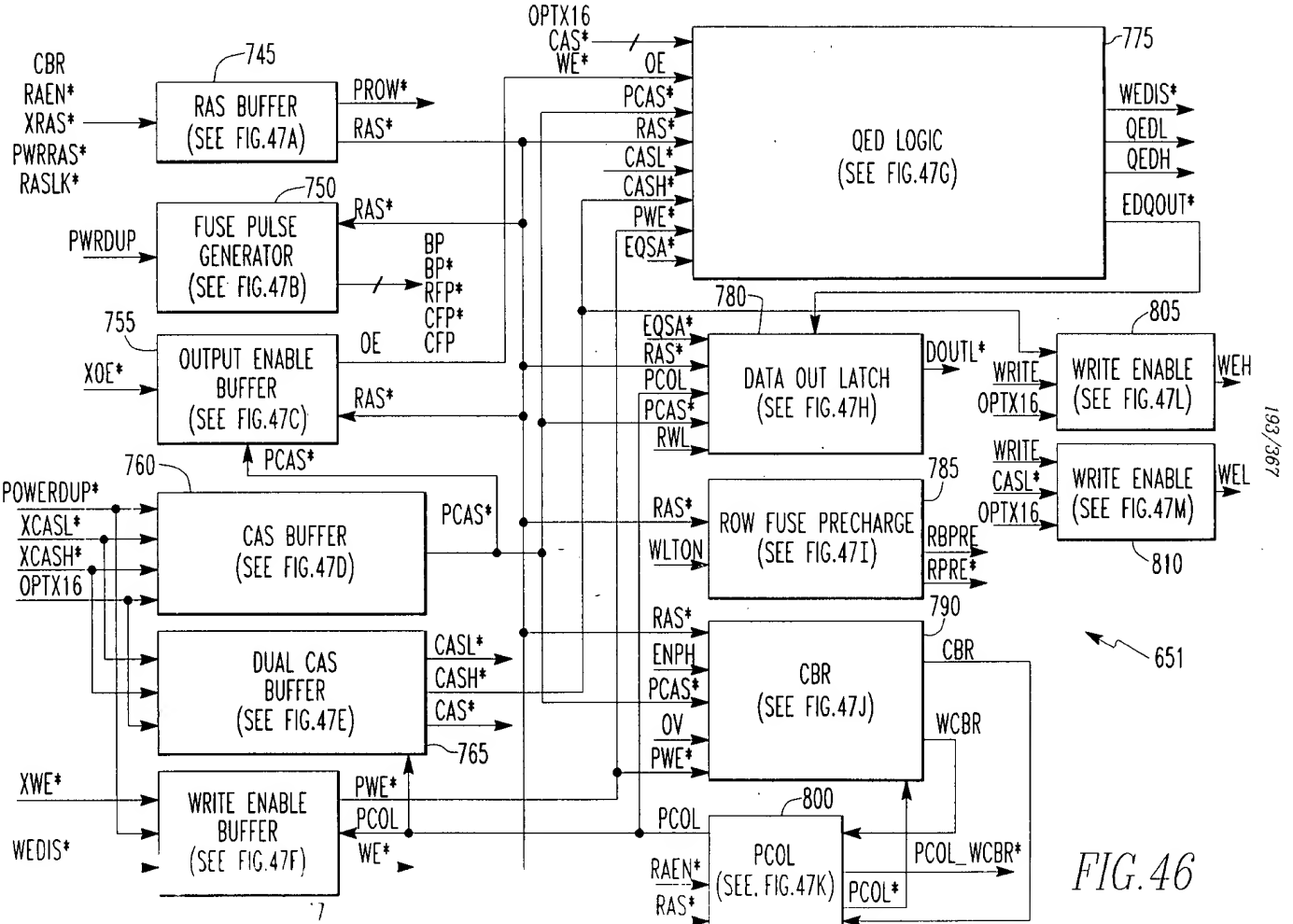


FIG. 46

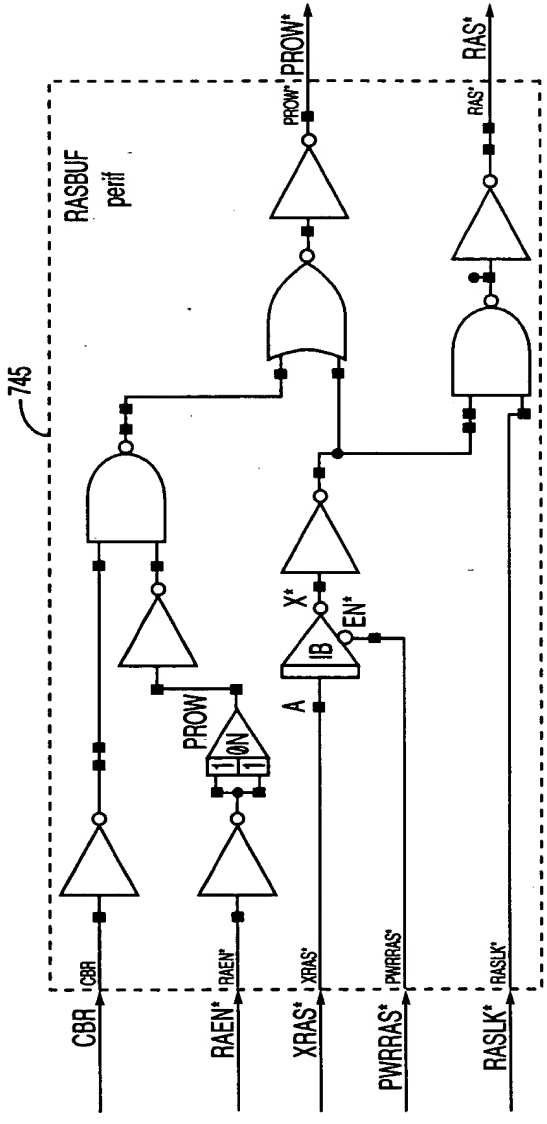

745
RASBUF
perif
CBR
RAEN*
XRAS*
PWRRAS*
RASLK*
CBR
RAEN
XRAS
PWRRAS
RASLK
PROW
10N
A
IB
X*
EN*
PROW*
RAS*

FIG. 47A

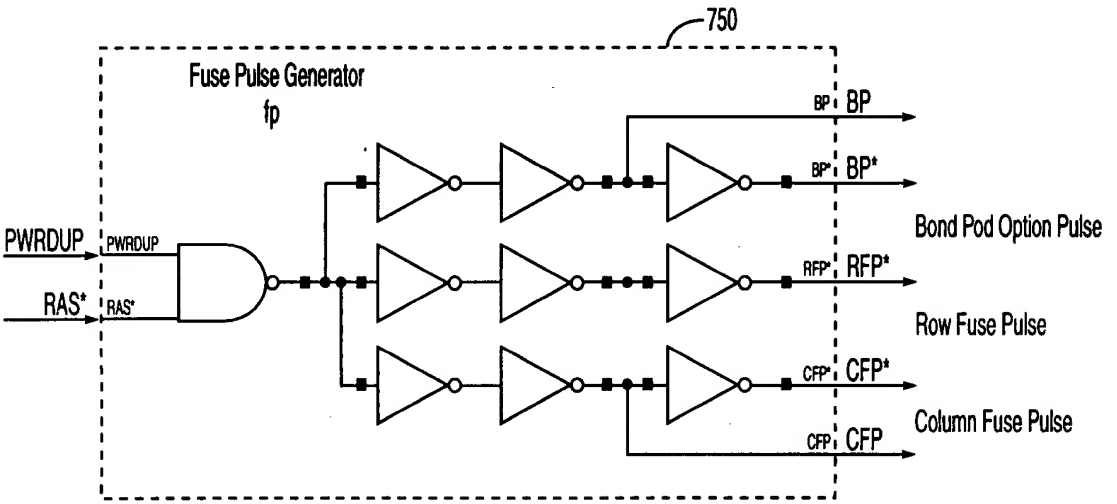

750
Fuse Pulse Generator
fp
PWRDUP
RAS*
PWRDUP
RAS*
BP
BP*
RFP*
CFP*
CFP
BP
BP*
RFP
CFP
Bond Pod Option Pulse
Row Fuse Pulse
Column Fuse Pulse

FIG. 47B

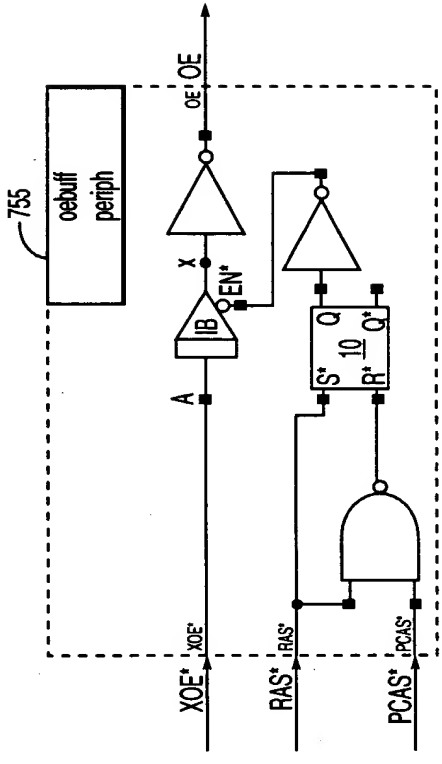

755
oebuff
periph
OE
OE'
X
EN*
IB
A
S*
10
R*
Q
Q*
XOE*
XOE'
RAS*
RAS'
PCAS*
PCAS'

FIG. 47C

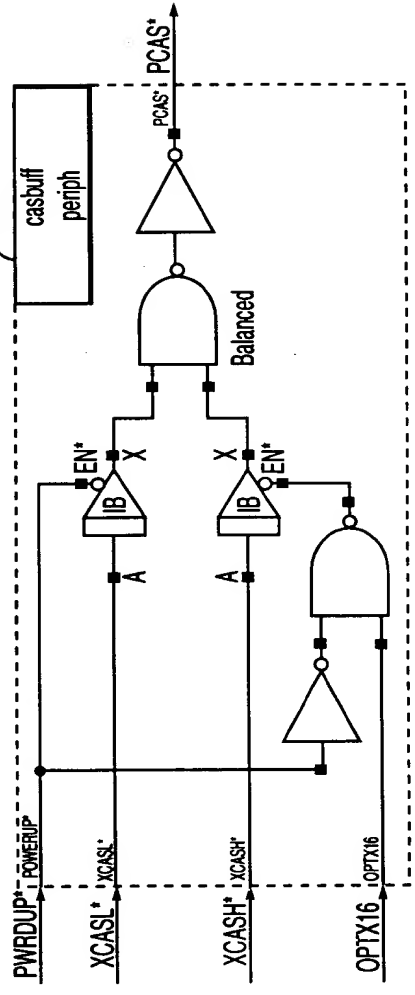

760
casbuff
periph
PCAS*
PCAS*
Balanced
EN*
X
IB
A
X
EN*
IB
A
PWRDUP*
POWERUP*
XCASL*
XCASL*
XCASH*
XCASH*
OPTX16
OPTX16

FIG. 47D

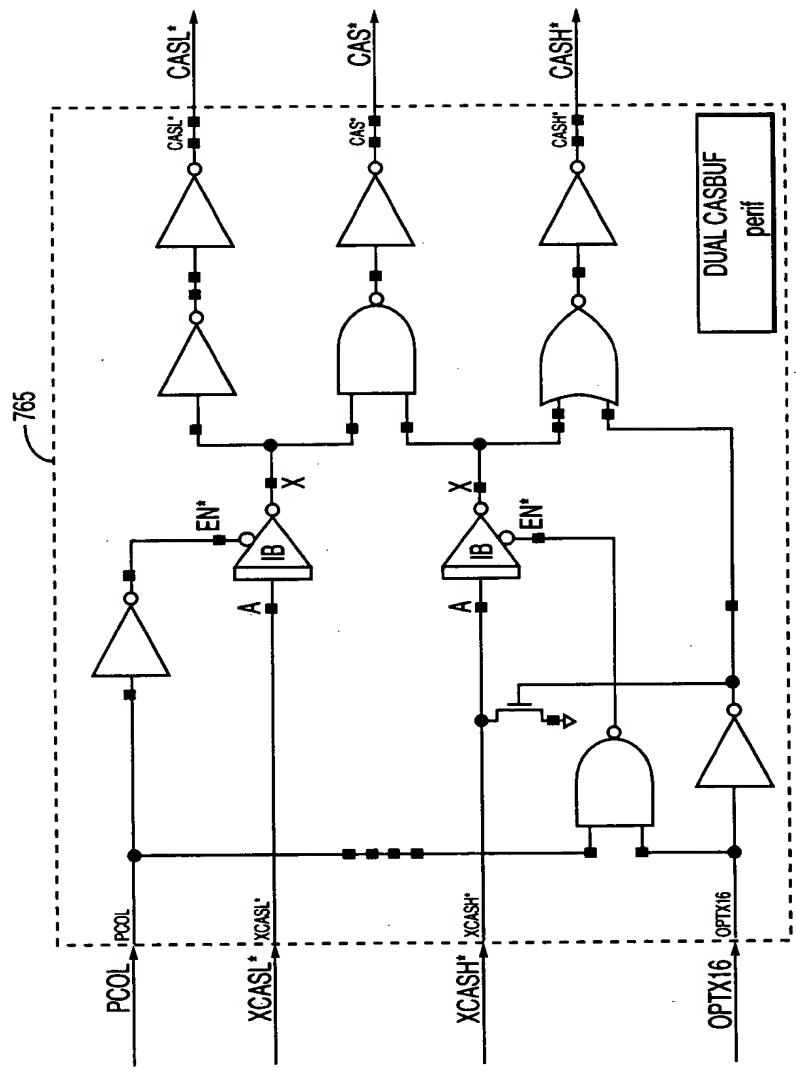

765
CASL*
CAS*
CASH*
DUAL CASBUF
perfi
EN*
X
IB
A
PCOL
XCASL*
XCASH*
OPTX16

FIG. 47E

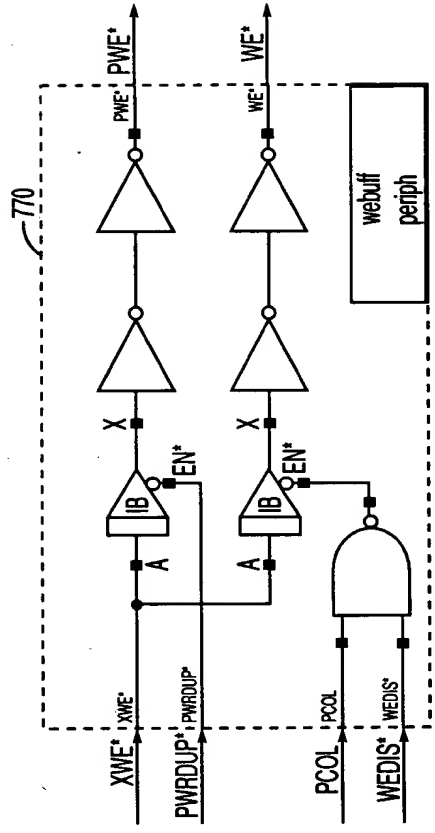


FIG. 47F

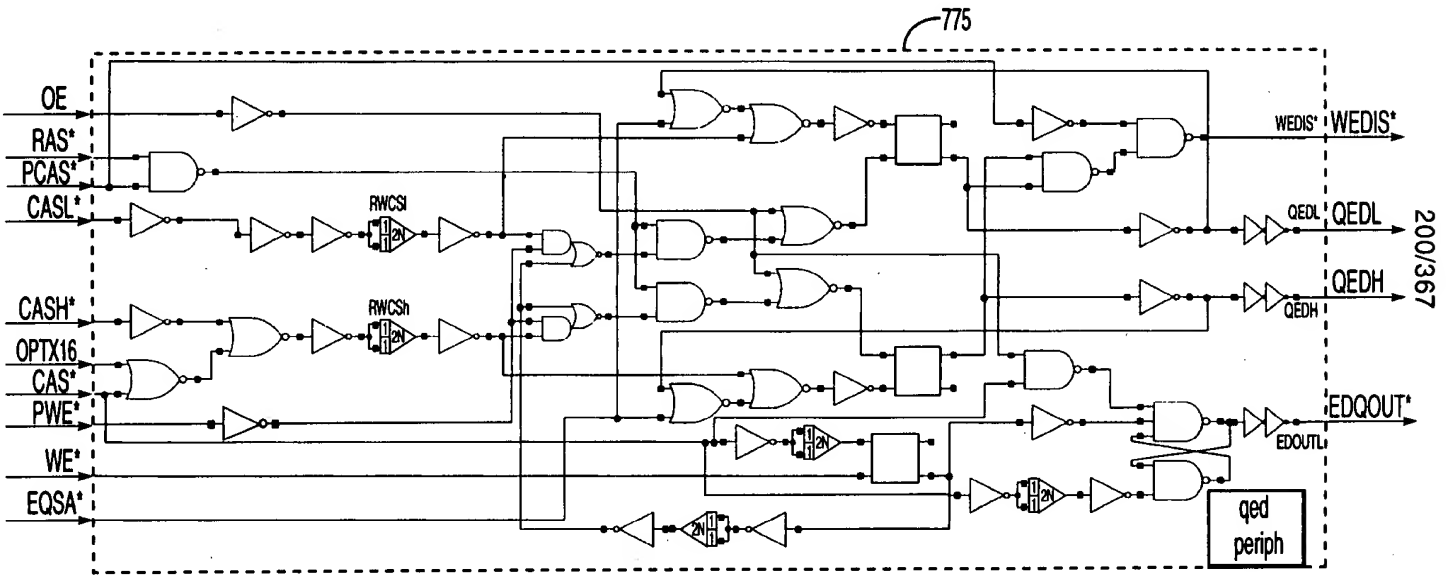

775
OE
RAS*
PCAS*
CASL*
CASH*
OPTX16
CAS*
PWE*
WE*
EQSA*
RWCSl
RWCSh
2N
WEDIS*
WEDIS*
QEDL
QEDL
QEDH
QEDH
EDQOUT*
EDOUTL
qed
periph

FIG. 47G

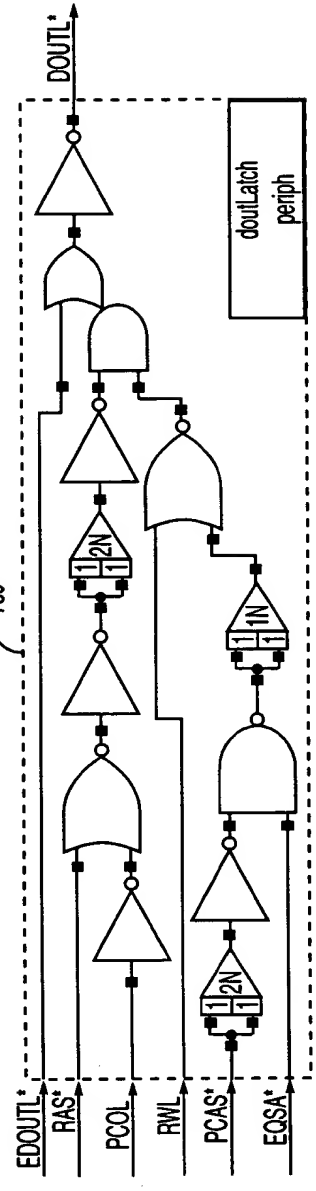


FIG. 47H

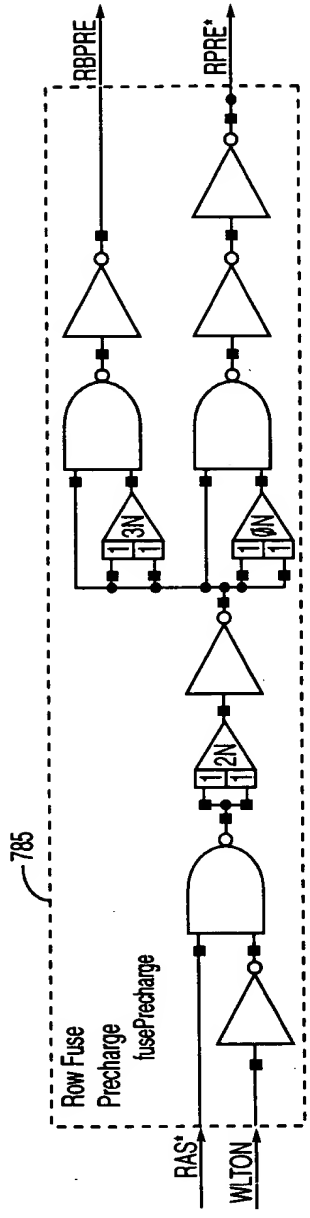

RBPRE
RPRE'
3N
ØN
2N
785
Row Fuse
Precharge
fusePrecharge
RAS'
WLTON

FIG. 47I

TOSHIBA 8291060

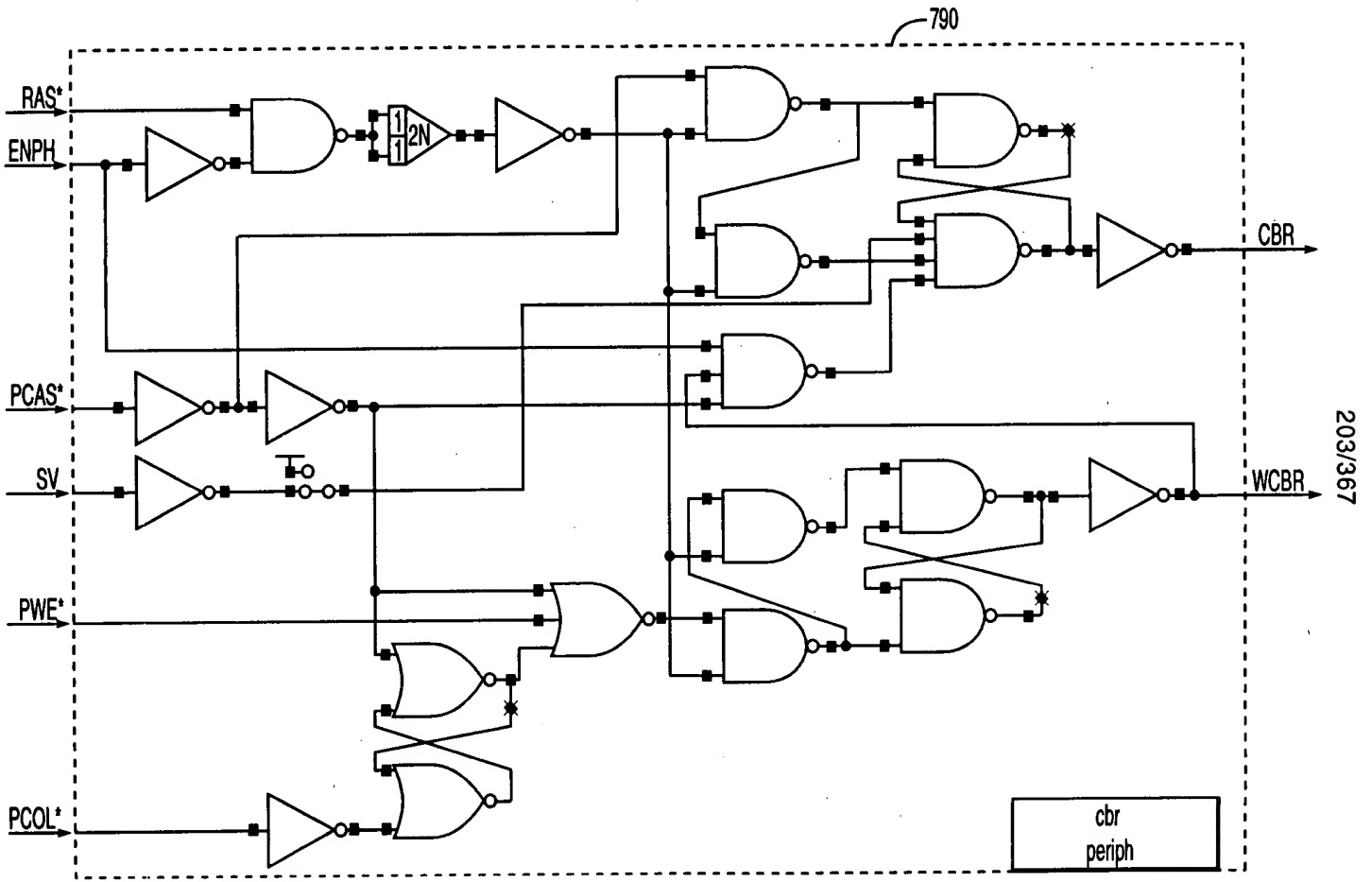


FIG. 47J

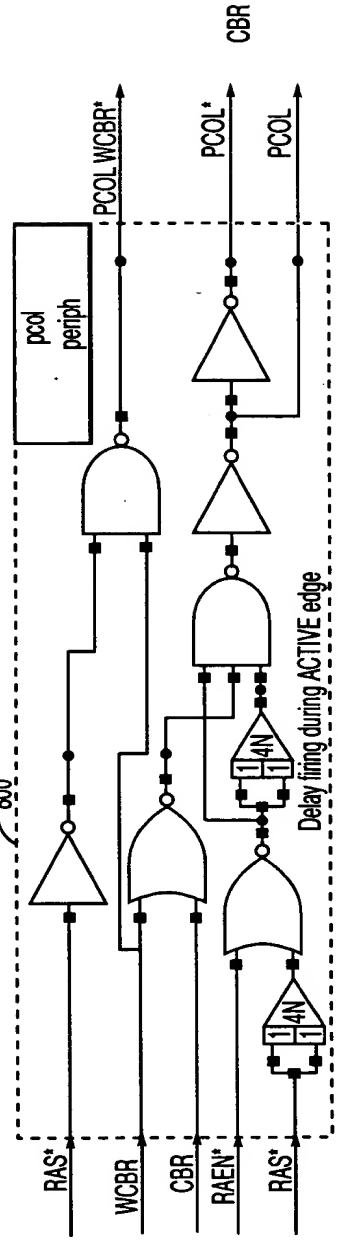

RAS*
WCBR
CBR
RAEN*
RAS*
800
4N
4N
Delay firing during ACTIVE edge
pcol periph
PCOL WCBR*
PCOL*
PCOL
CBR

FIG. 47K

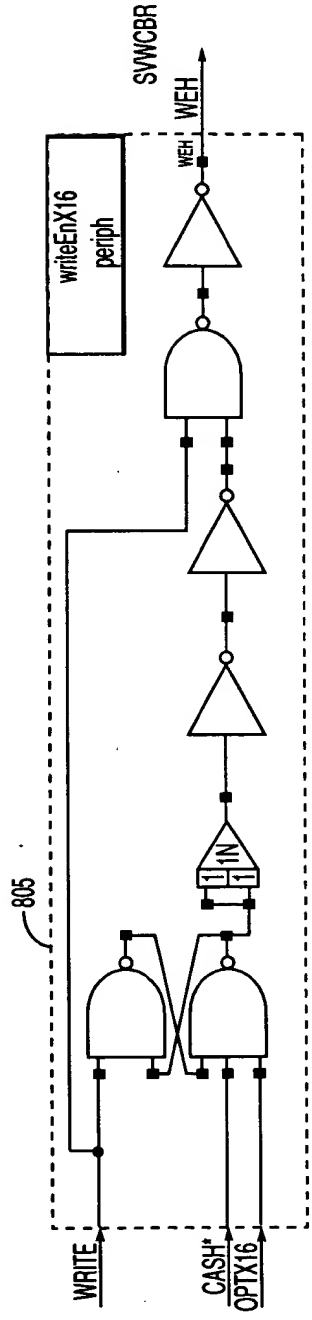

SVWCBR
WEH
WEH
writeEnX16
periph
805
1
1
1N
1
WRITE
CASH*
OPTX16

FIG. 47L

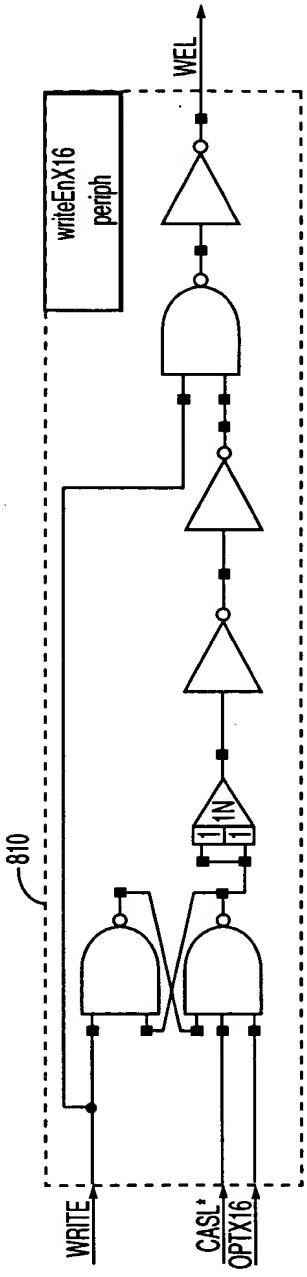


FIG. 47M

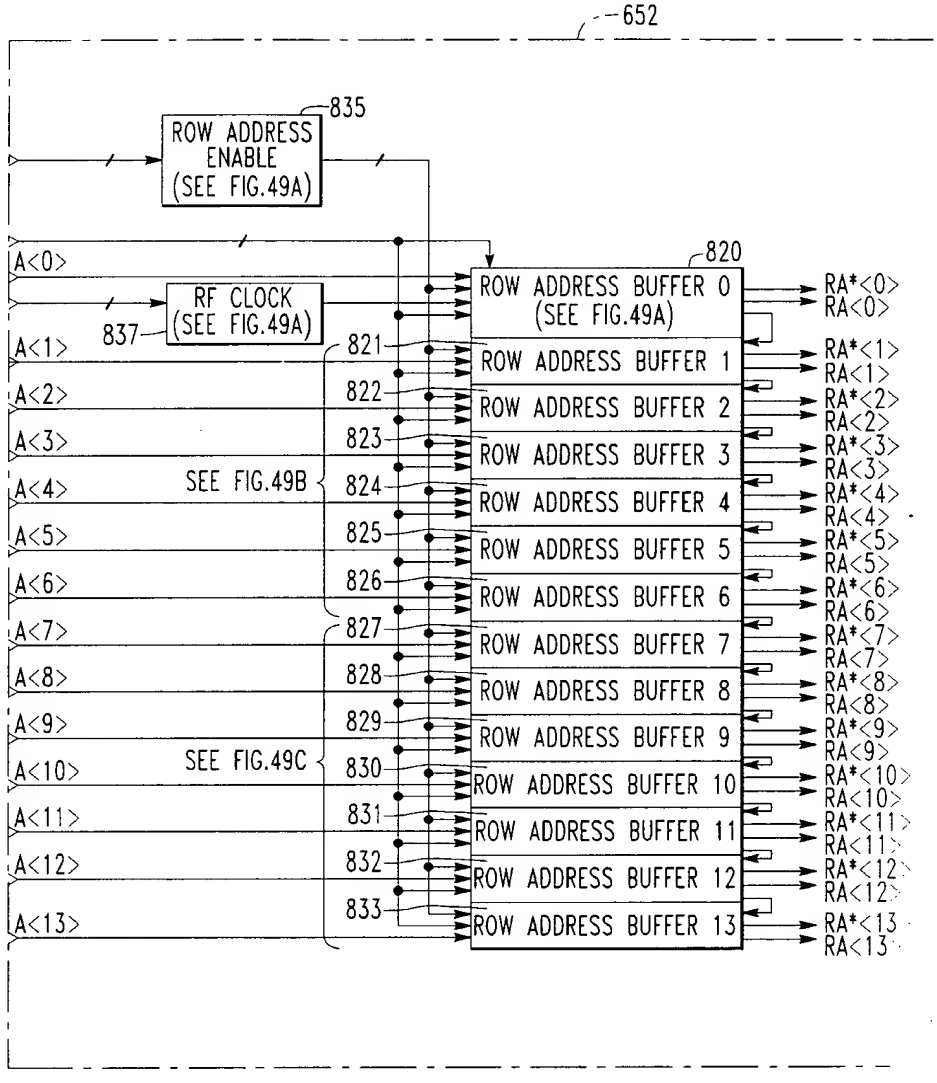

652
835
ROW ADDRESS ENABLE (SEE FIG.49A)
820
A<0>
RF CLOCK (SEE FIG.49A)
837
A<1>
A<2>
A<3>
A<4>
A<5>
A<6>
A<7>
A<8>
A<9>
A<10>
A<11>
A<12>
A<13>
SEE FIG.49B
SEE FIG.49C
821
822
823
824
825
826
827
828
829
830
831
832
833
ROW ADDRESS BUFFER 0 (SEE FIG.49A)
ROW ADDRESS BUFFER 1
ROW ADDRESS BUFFER 2
ROW ADDRESS BUFFER 3
ROW ADDRESS BUFFER 4
ROW ADDRESS BUFFER 5
ROW ADDRESS BUFFER 6
ROW ADDRESS BUFFER 7
ROW ADDRESS BUFFER 8
ROW ADDRESS BUFFER 9
ROW ADDRESS BUFFER 10
ROW ADDRESS BUFFER 11
ROW ADDRESS BUFFER 12
ROW ADDRESS BUFFER 13
RA*<0>
RA<0>
RA*<1>
RA<1>
RA*<2>
RA<2>
RA*<3>
RA<3>
RA*<4>
RA<4>
RA*<5>
RA<5>
RA*<6>
RA<6>
RA*<7>
RA<7>
RA*<8>
RA<8>
RA*<9>
RA<9>
RA*<10>
RA<10>
RA*<11>
RA<11>
RA*<12>
RA<12>
RA*<13>
RA<13>

FIG. 48A

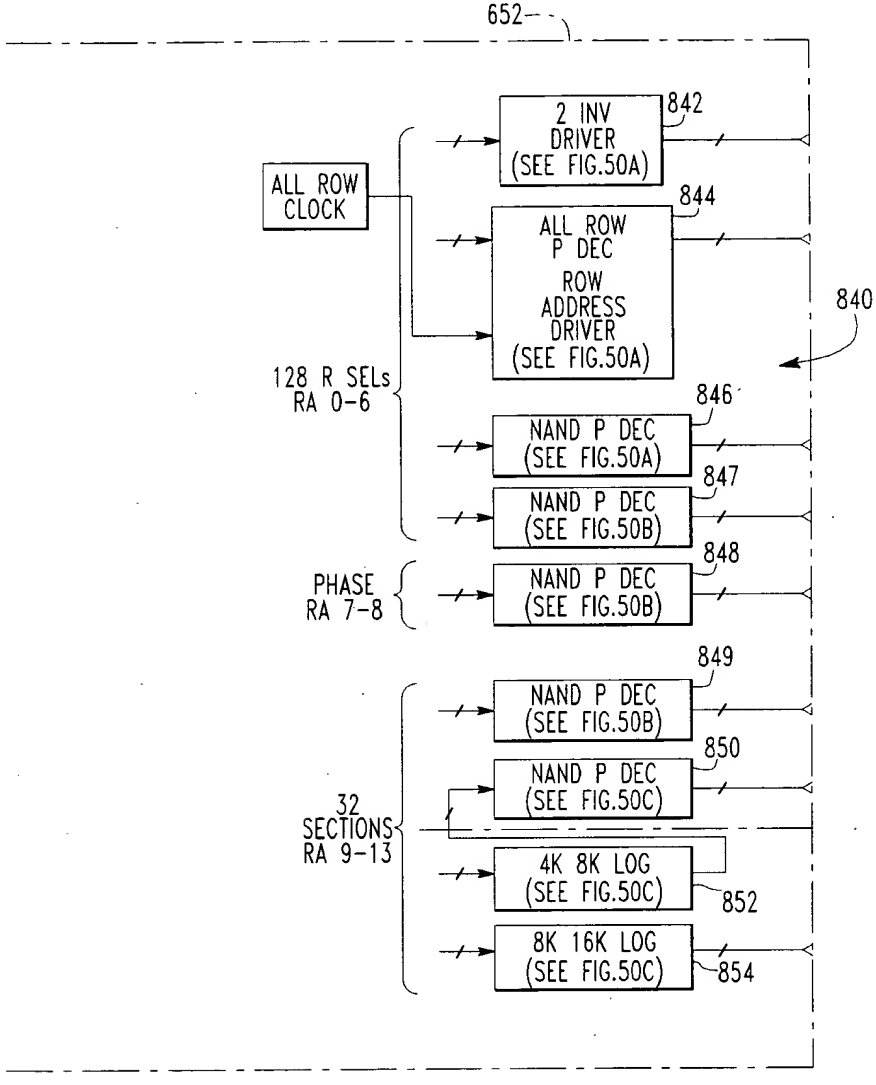

652
2 INV DRIVER (SEE FIG.50A)
842
ALL ROW CLOCK
ALL ROW P DEC
ROW ADDRESS DRIVER (SEE FIG.50A)
844
840
128 R SELs RA 0-6
NAND P DEC (SEE FIG.50A)
846
NAND P DEC (SEE FIG.50B)
847
PHASE RA 7-8
NAND P DEC (SEE FIG.50B)
848
NAND P DEC (SEE FIG.50B)
849
32 SECTIONS RA 9-13
NAND P DEC (SEE FIG.50C)
850
4K 8K LOG (SEE FIG.50C)
852
8K 16K LOG (SEE FIG.50C)
854

FIG. 48B

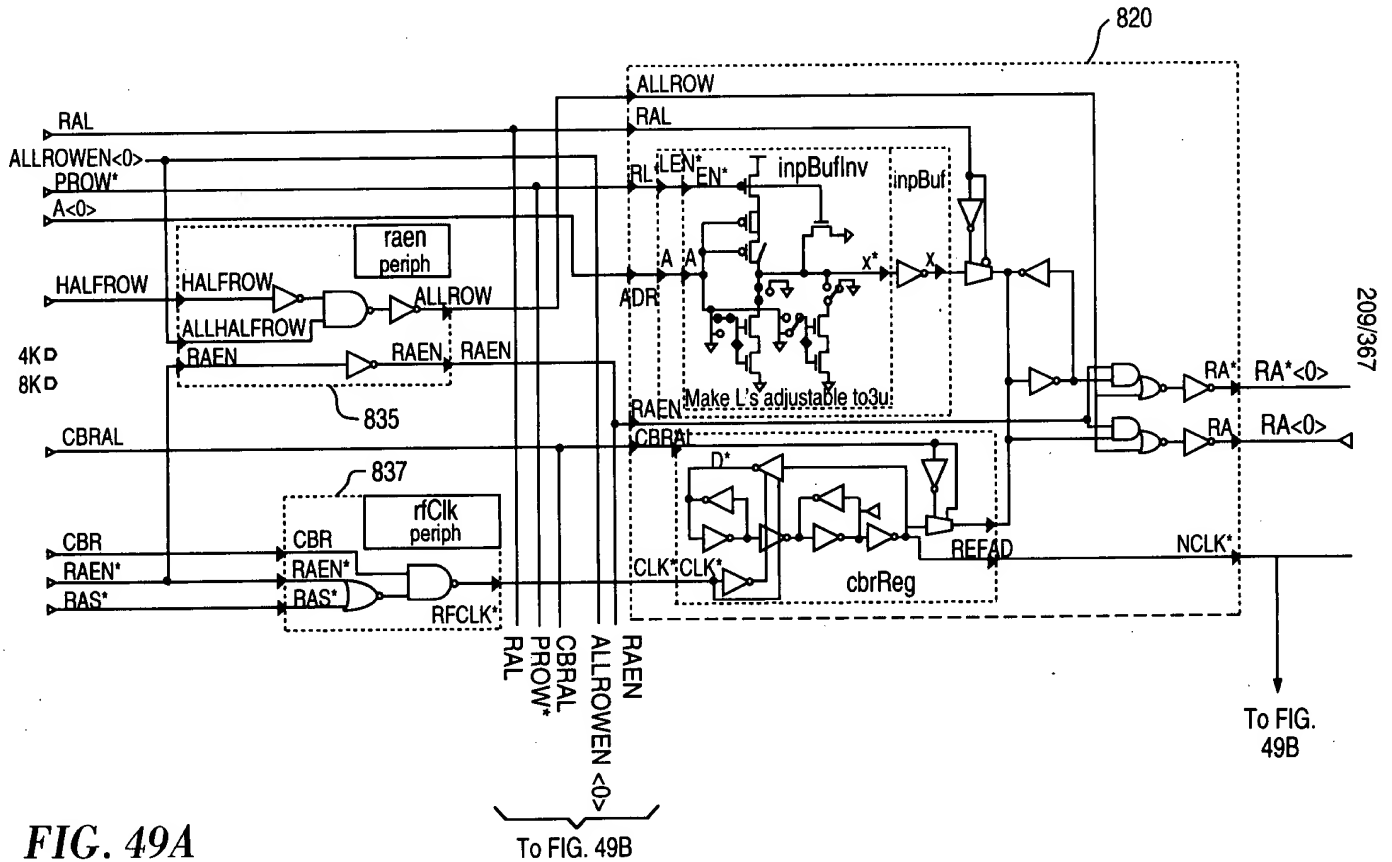

820
ALLROW
RAL
RAL
ALLROWEN<0>
PROW*
A<0>
RL
LEN*
EN*
inpBufInv
inpBuf
raen
periph
HALFROW
HALFROW
ALLROW
ALLHALFROW
RAEN
RAEN
RAEN
4KD
8KD
835
A
A
x*
X
ADR
Make L's adjustable to3u
RA*
RA*<0>
RA
RA<0>
RAEN
CBRAL
CBRAL
837
rfClk
periph
D*
CBR
CBR
RAEN*
RAEN*
BAS*
BAS*
RFCLK*
CLK*
CLK*
cbrReg
REFAD
NCLK*
RAL
CBRAL
PROW*
ALLROWEN <0>
RAEN
To FIG. 49B
To FIG. 49B

FIG. 49A

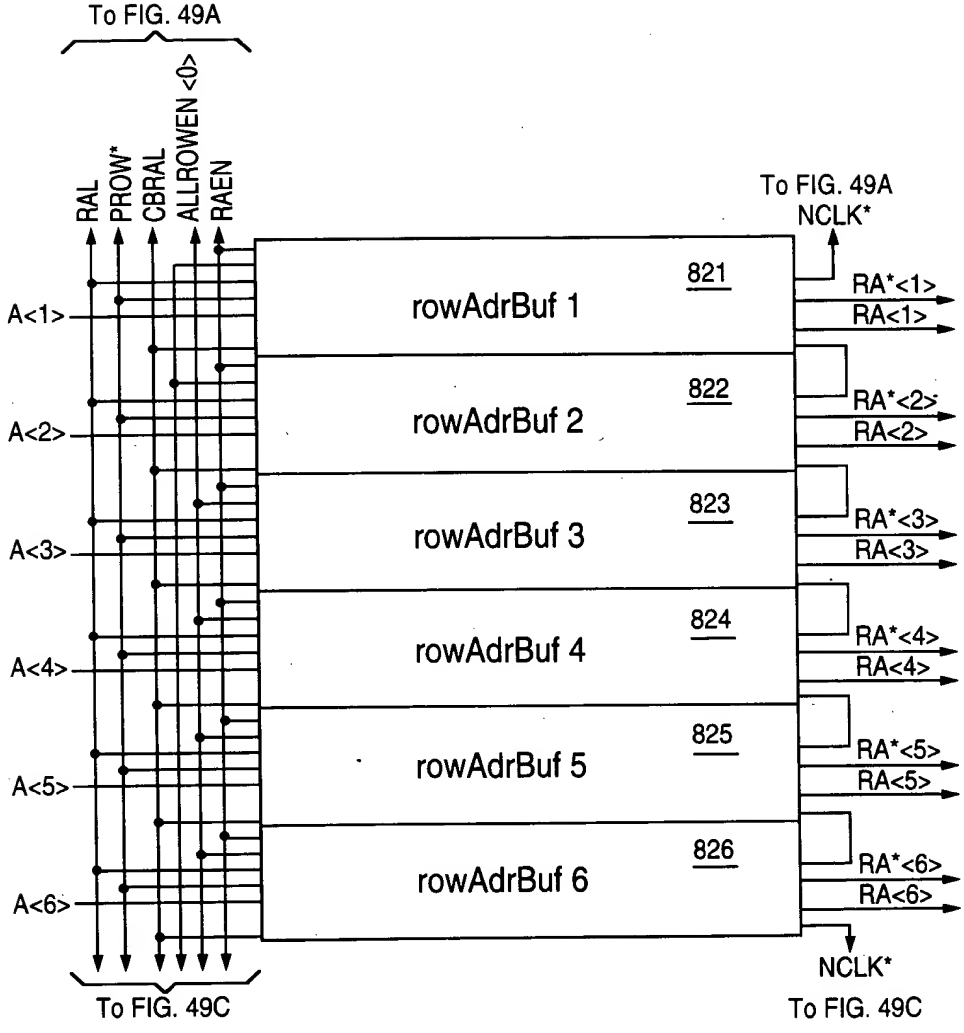

To FIG. 49A
RAL
PROW*
CBRAL
ALLROWEN <0>
RAEN
To FIG. 49A
NCLK*
A<1>
A<2>
A<3>
A<4>
A<5>
A<6>
rowAdrBuf 1
821
rowAdrBuf 2
822
rowAdrBuf 3
823
rowAdrBuf 4
824
rowAdrBuf 5
825
rowAdrBuf 6
826
RA*<1>
RA<1>
RA*<2>
RA<2>
RA*<3>
RA<3>
RA*<4>
RA<4>
RA*<5>
RA<5>
RA*<6>
RA<6>
NCLK*
To FIG. 49C
To FIG. 49C

FIG. 49B

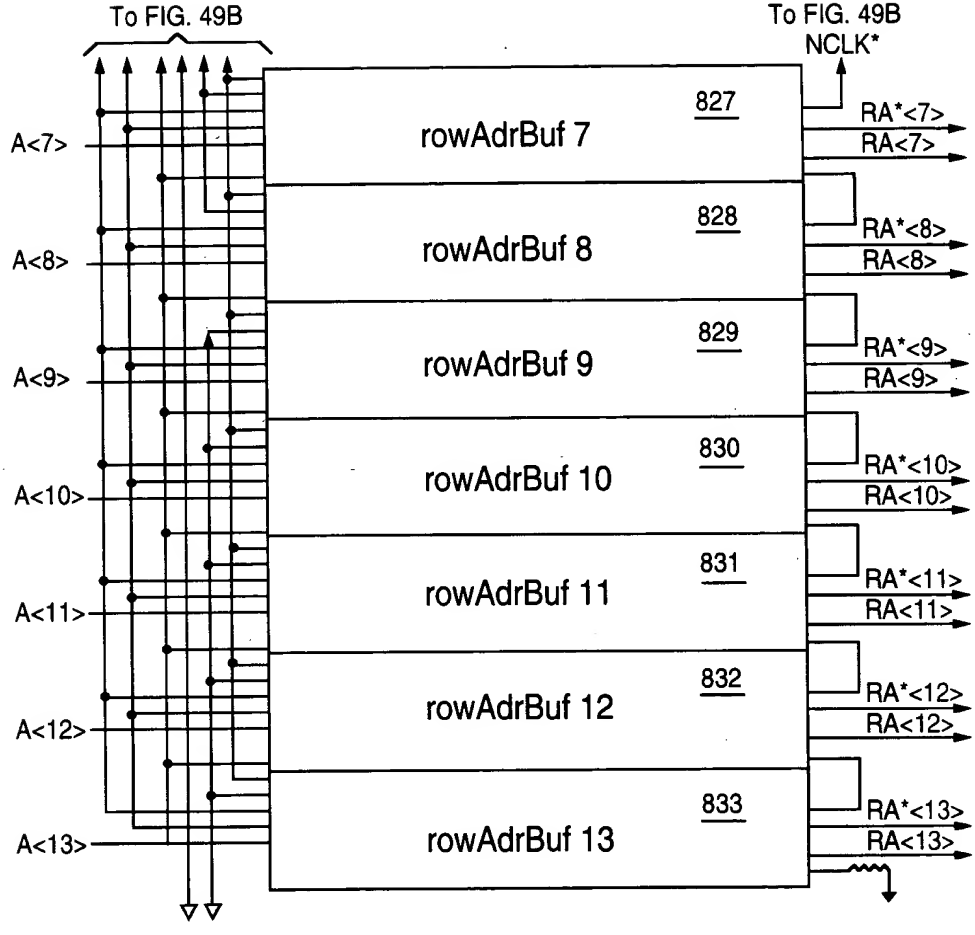

To FIG. 49B
To FIG. 49B
NCLK*
A<7>
A<8>
A<9>
A<10>
A<11>
A<12>
A<13>
rowAdrBuf 7
827
rowAdrBuf 8
828
rowAdrBuf 9
829
rowAdrBuf 10
830
rowAdrBuf 11
831
rowAdrBuf 12
832
rowAdrBuf 13
833
RA*<7>
RA<7>
RA*<8>
RA<8>
RA*<9>
RA<9>
RA*<10>
RA<10>
RA*<11>
RA<11>
RA*<12>
RA<12>
RA*<13>
RA<13>

FIG. 49C

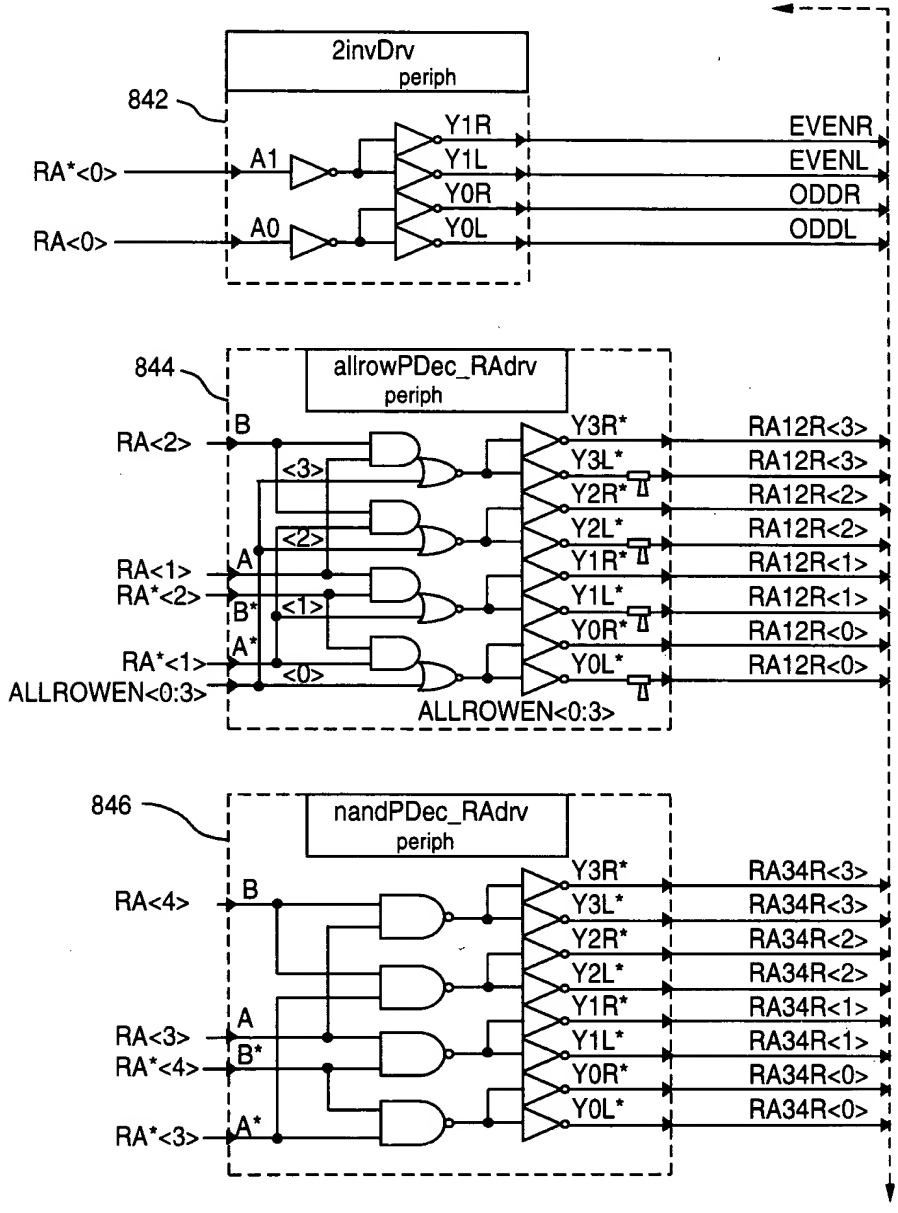

2invDrv
periph
842
RA*<0>
RA<0>
A1
A0
Y1R
Y1L
Y0R
Y0L
EVENR
EVENL
ODDR
ODDL
844
allrowPDec_RAdrv
periph
RA<2>
RA<1>
RA*<2>
RA*<1>
ALLROWEN<0:3>
B
A
B*
A*
<3>
<2>
<1>
<0>
Y3R*
Y3L*
Y2R*
Y2L*
Y1R*
Y1L*
Y0R*
Y0L*
RA12R<3>
RA12R<3>
RA12R<2>
RA12R<2>
RA12R<1>
RA12R<1>
RA12R<0>
RA12R<0>
ALLROWEN<0:3>
846
nandPDec_RAdrv
periph
RA<4>
RA<3>
RA*<4>
RA*<3>
B
A
B*
A*
Y3R*
Y3L*
Y2R*
Y2L*
Y1R*
Y1L*
Y0R*
Y0L*
RA34R<3>
RA34R<3>
RA34R<2>
RA34R<2>
RA34R<1>
RA34R<1>
RA34R<0>
RA34R<0>

FIG. 50A

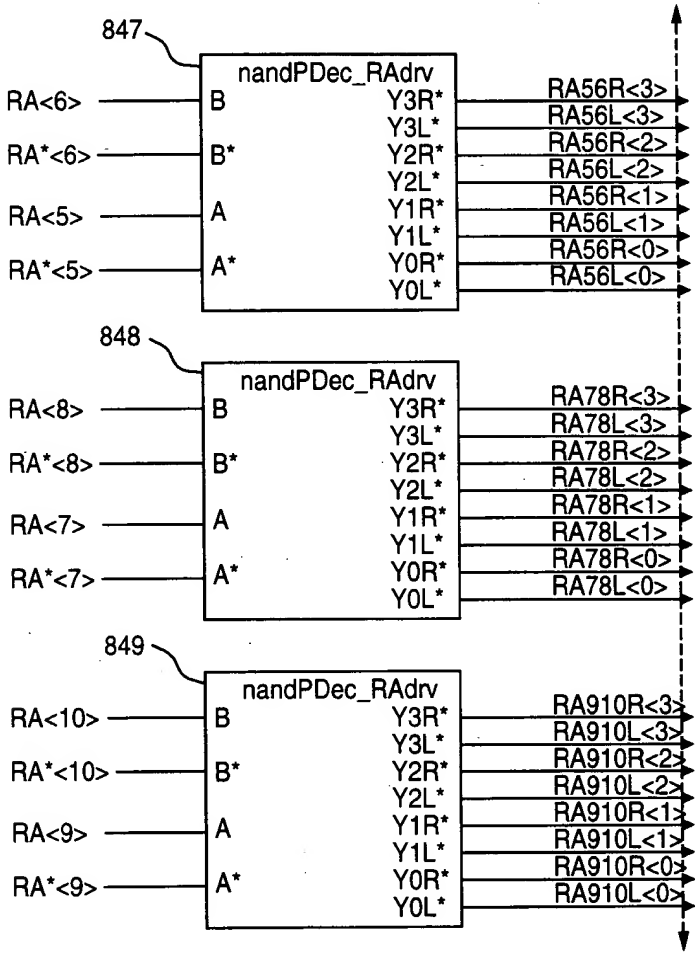

847
nandPDec_RAdrv
RA<6>
RA*<6>
RA<5>
RA*<5>
B
B*
A
A*
Y3R*
Y3L*
Y2R*
Y2L*
Y1R*
Y1L*
Y0R*
Y0L*
RA56R<3>
RA56L<3>
RA56R<2>
RA56L<2>
RA56R<1>
RA56L<1>
RA56R<0>
RA56L<0>
848
nandPDec_RAdrv
RA<8>
RA*<8>
RA<7>
RA*<7>
B
B*
A
A*
Y3R*
Y3L*
Y2R*
Y2L*
Y1R*
Y1L*
Y0R*
Y0L*
RA78R<3>
RA78L<3>
RA78R<2>
RA78L<2>
RA78R<1>
RA78L<1>
RA78R<0>
RA78L<0>
849
nandPDec_RAdrv
RA<10>
RA*<10>
RA<9>
RA*<9>
B
B*
A
A*
Y3R*
Y3L*
Y2R*
Y2L*
Y1R*
Y1L*
Y0R*
Y0L*
RA910R<3>
RA910L<3>
RA910R<2>
RA910L<2>
RA910R<1>
RA910L<1>
RA910R<0>
RA910L<0>

FIG. 50B

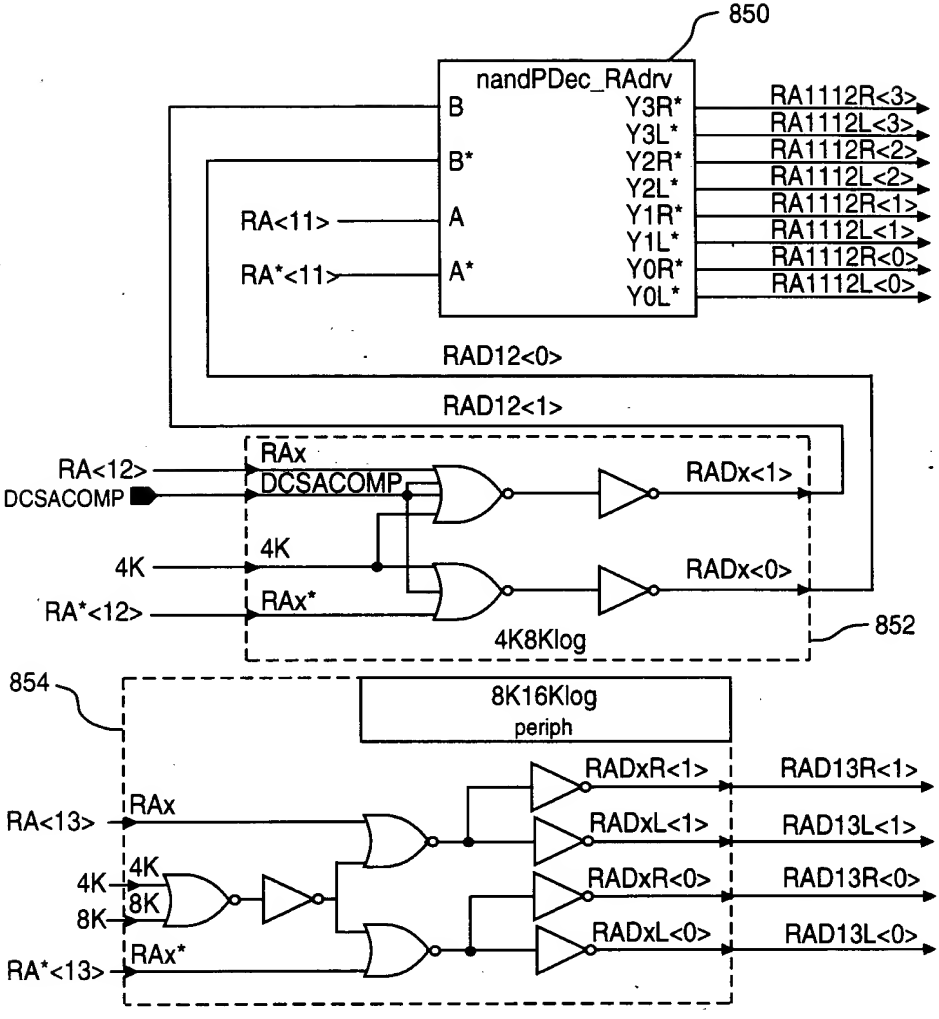

850
nandPDec_RAdrv
B
B*
A
A*
RA<11>
RA*<11>
Y3R*
Y3L*
Y2R*
Y2L*
Y1R*
Y1L*
Y0R*
Y0L*
RA1112R<3>
RA1112L<3>
RA1112R<2>
RA1112L<2>
RA1112R<1>
RA1112L<1>
RA1112R<0>
RA1112L<0>
RAD12<0>
RAD12<1>
RA<12>
DCSACOMP
RAx
DCSACOMP
RADx<1>
4K
4K
RA*<12>
RAx*
RADx<0>
4K8Klog
852
854
8K16Klog
periph
RA<13>
RAx
4K
8K
4K
8K
RA*<13>
RAx*
RADxR<1>
RADxL<1>
RADxR<0>
RADxL<0>
RAD13R<1>
RAD13L<1>
RAD13R<0>
RAD13L<0>

FIG. 50C

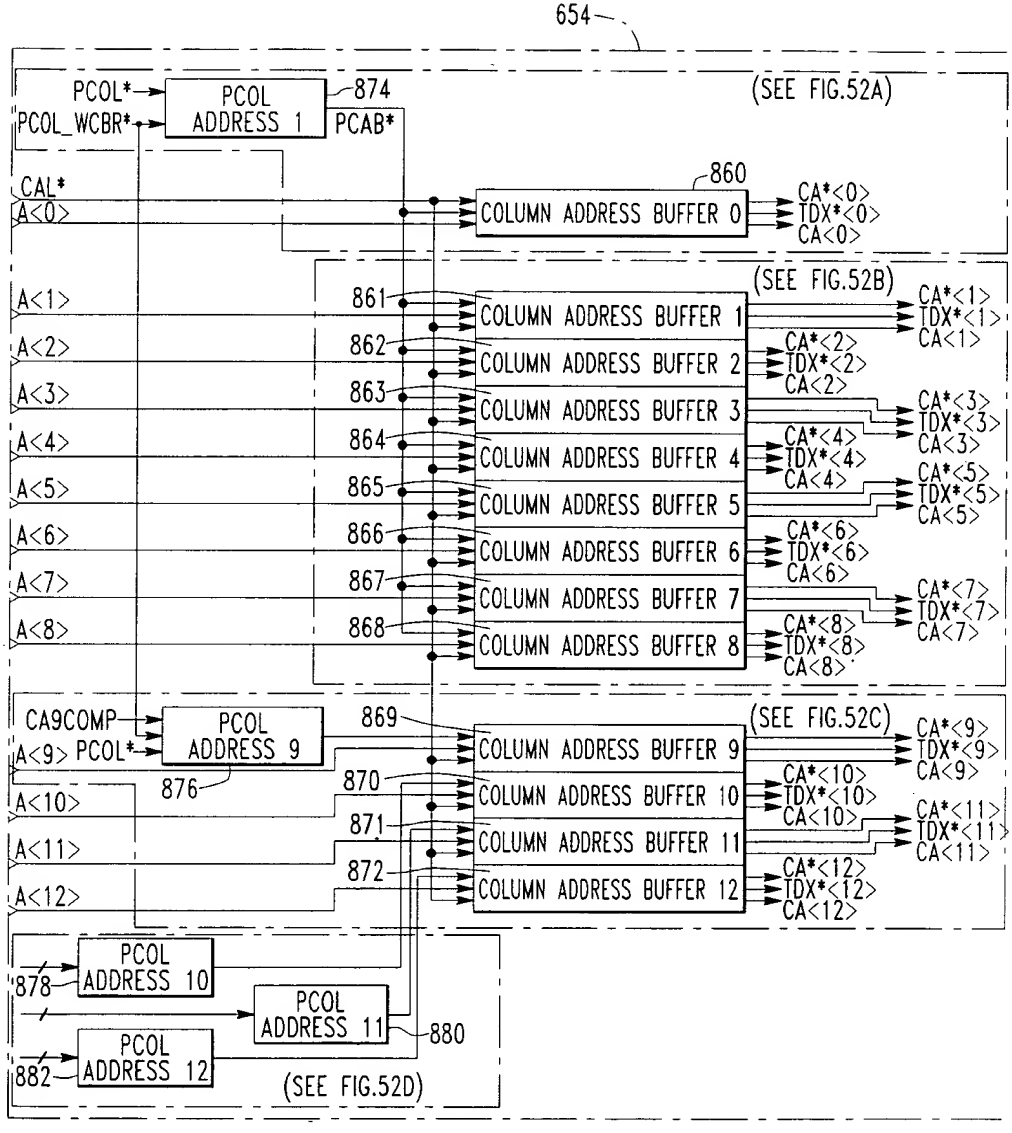

654
PCOL*
PCOL_WCBR*
PCOL ADDRESS 1
874
PCAB*
(SEE FIG.52A)
CAL*
A<0>
860
COLUMN ADDRESS BUFFER 0
CA*<0>
TDX*<0>
CA<0>
(SEE FIG.52B)
A<1>
A<2>
A<3>
A<4>
A<5>
A<6>
A<7>
A<8>
861
862
863
864
865
866
867
868
COLUMN ADDRESS BUFFER 1
COLUMN ADDRESS BUFFER 2
COLUMN ADDRESS BUFFER 3
COLUMN ADDRESS BUFFER 4
COLUMN ADDRESS BUFFER 5
COLUMN ADDRESS BUFFER 6
COLUMN ADDRESS BUFFER 7
COLUMN ADDRESS BUFFER 8
CA*<1>
TDX*<1>
CA<1>
CA*<2>
TDX*<2>
CA<2>
CA*<3>
TDX*<3>
CA<3>
CA*<4>
TDX*<4>
CA<4>
CA*<5>
TDX*<5>
CA<5>
CA*<6>
TDX*<6>
CA<6>
CA*<7>
TDX*<7>
CA<7>
CA*<8>
TDX*<8>
CA<8>
CA9COMP
A<9>
PCOL*
PCOL ADDRESS 9
876
(SEE FIG.52C)
A<10>
A<11>
A<12>
869
870
871
872
COLUMN ADDRESS BUFFER 9
COLUMN ADDRESS BUFFER 10
COLUMN ADDRESS BUFFER 11
COLUMN ADDRESS BUFFER 12
CA*<9>
TDX*<9>
CA<9>
CA*<10>
TDX*<10>
CA<10>
CA*<11>
TDX*<11>
CA<11>
CA*<12>
TDX*<12>
CA<12>
878
PCOL ADDRESS 10
PCOL ADDRESS 11
880
882
PCOL ADDRESS 12
(SEE FIG.52D)

FIG. 51A

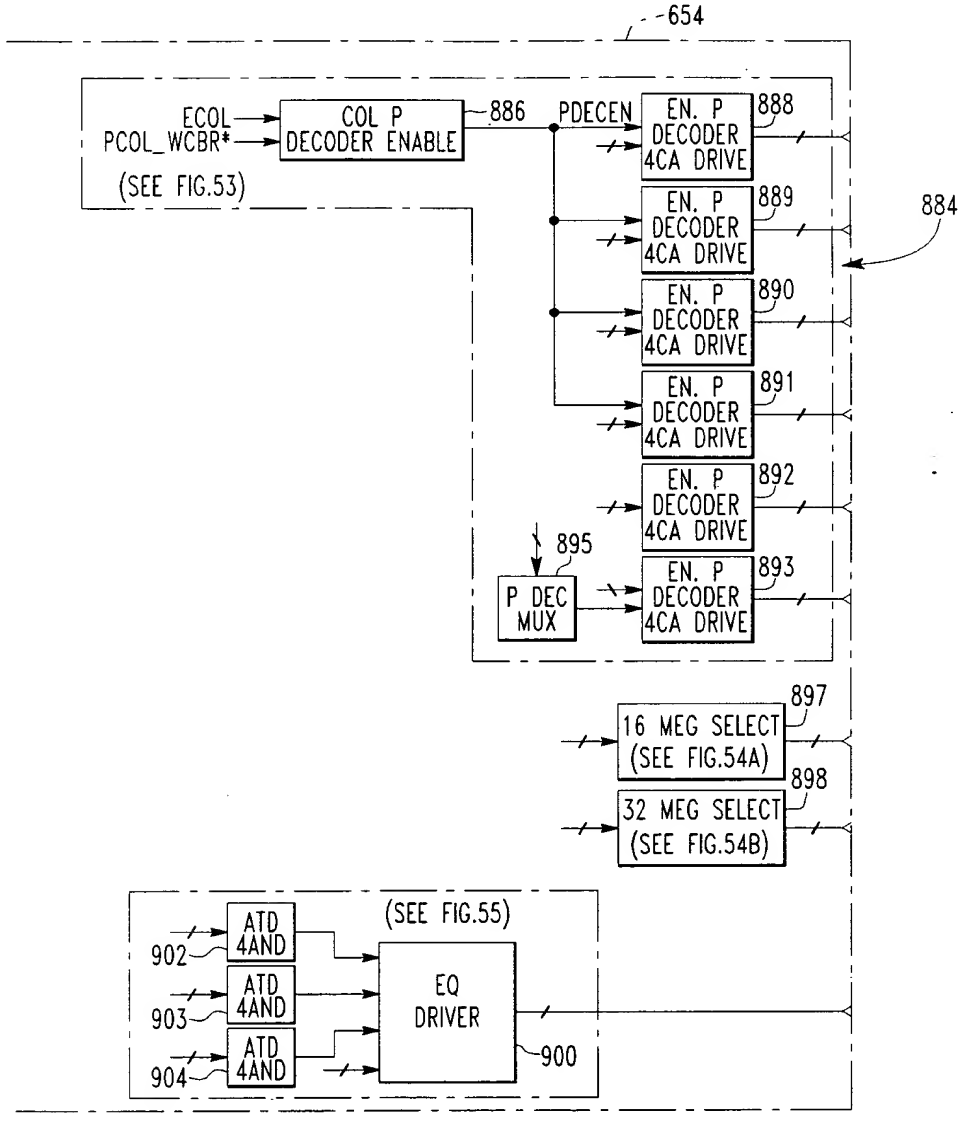

654
ECOL
PCOL_WCBR*
COL P DECODER ENABLE
886
PDECEN
EN. P DECODER 4CA DRIVE
888
889
890
891
892
893
884
(SEE FIG.53)
895
P DEC MUX
16 MEG SELECT (SEE FIG.54A)
897
32 MEG SELECT (SEE FIG.54B)
898
(SEE FIG.55)
ATD 4AND
902
903
904
EQ DRIVER
900

FIG. 51B

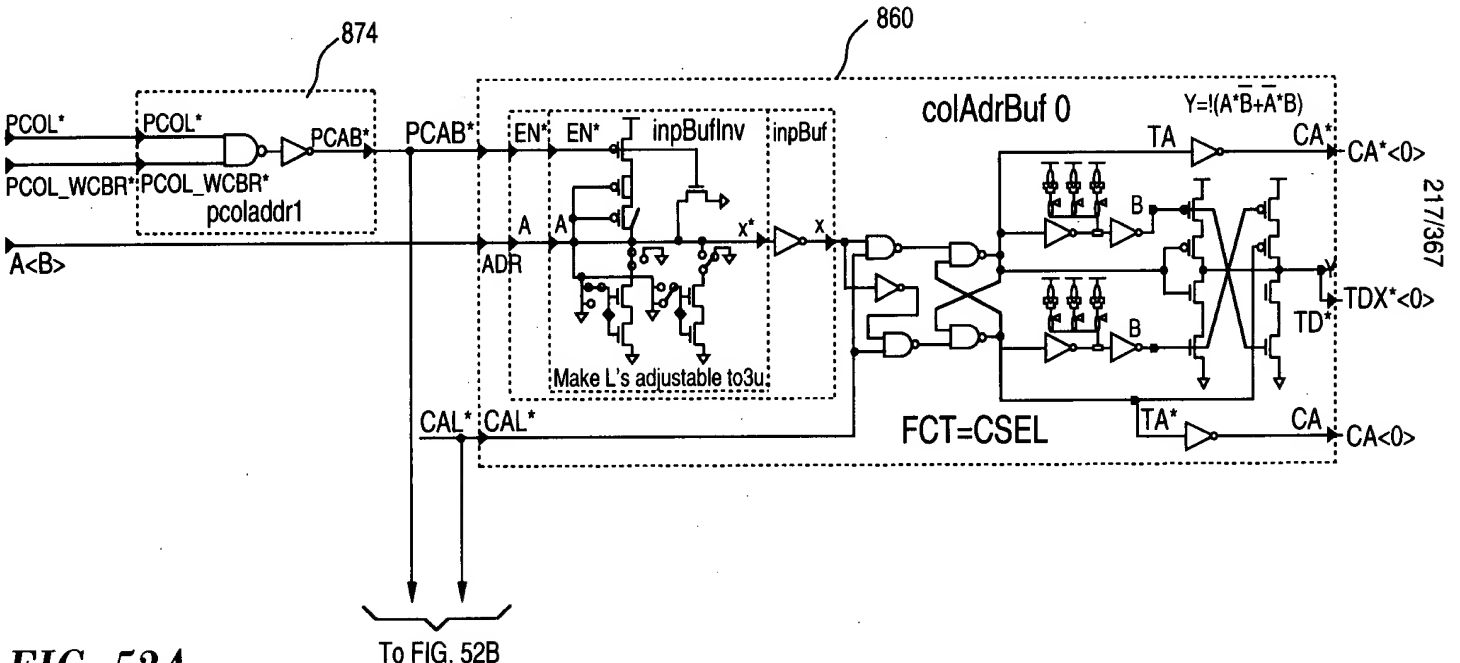

874
860
PCOL*
PCOL*
PCOL_WCBR*
PCOL_WCBR*
pcoladdr1
PCAB*
PCAB*
A<B>
ADR
EN*
EN*
inpBufInv
inpBuf
A
A
x*
x
Make L's adjustable to3u
colAdrBuf 0
Y=!(A*B+A*B)
TA
CA*
CA*<0>
B
B
TDX*<0>
TD*
CAL*
CAL*
FCT=CSEL
TA*
CA
CA<0>
To FIG. 52B

FIG. 52A

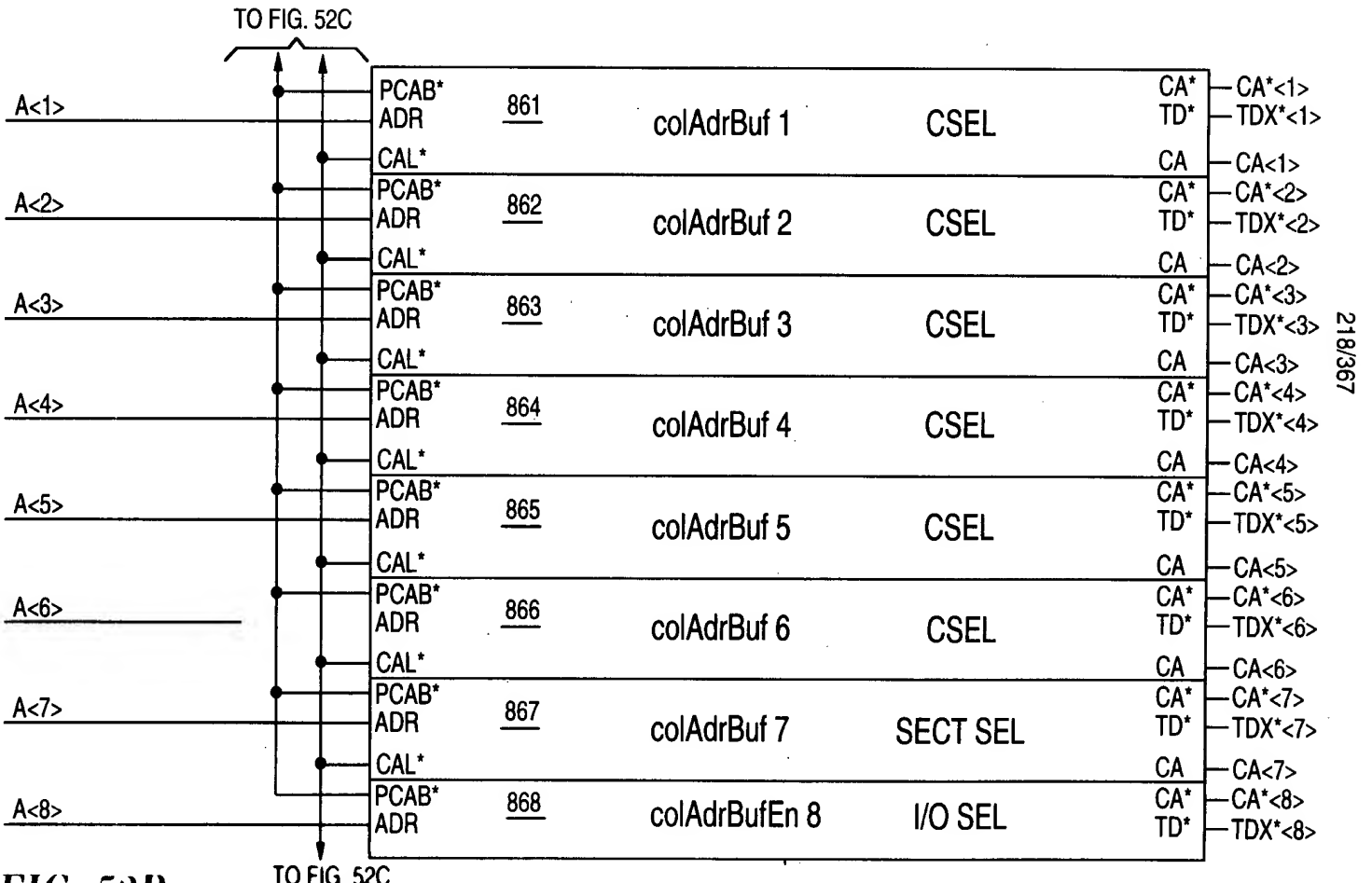

TO FIG. 52C
A<1>
A<2>
A<3>
A<4>
A<5>
A<6>
A<7>
A<8>
PCAB*
ADR
CAL*
861
862
863
864
865
866
867
868
colAdrBuf 1
colAdrBuf 2
colAdrBuf 3
colAdrBuf 4
colAdrBuf 5
colAdrBuf 6
colAdrBuf 7
colAdrBufEn 8
CSEL
SECT SEL
I/O SEL
CA*
TD*
CA
CA*<1>
TDX*<1>
CA<1>
CA*<2>
TDX*<2>
CA<2>
CA*<3>
TDX*<3>
CA<3>
CA*<4>
TDX*<4>
CA<4>
CA*<5>
TDX*<5>
CA<5>
CA*<6>
TDX*<6>
CA<6>
CA*<7>
TDX*<7>
CA<7>
CA*<8>
TDX*<8>
TO FIG. 52C

FIG. 52B

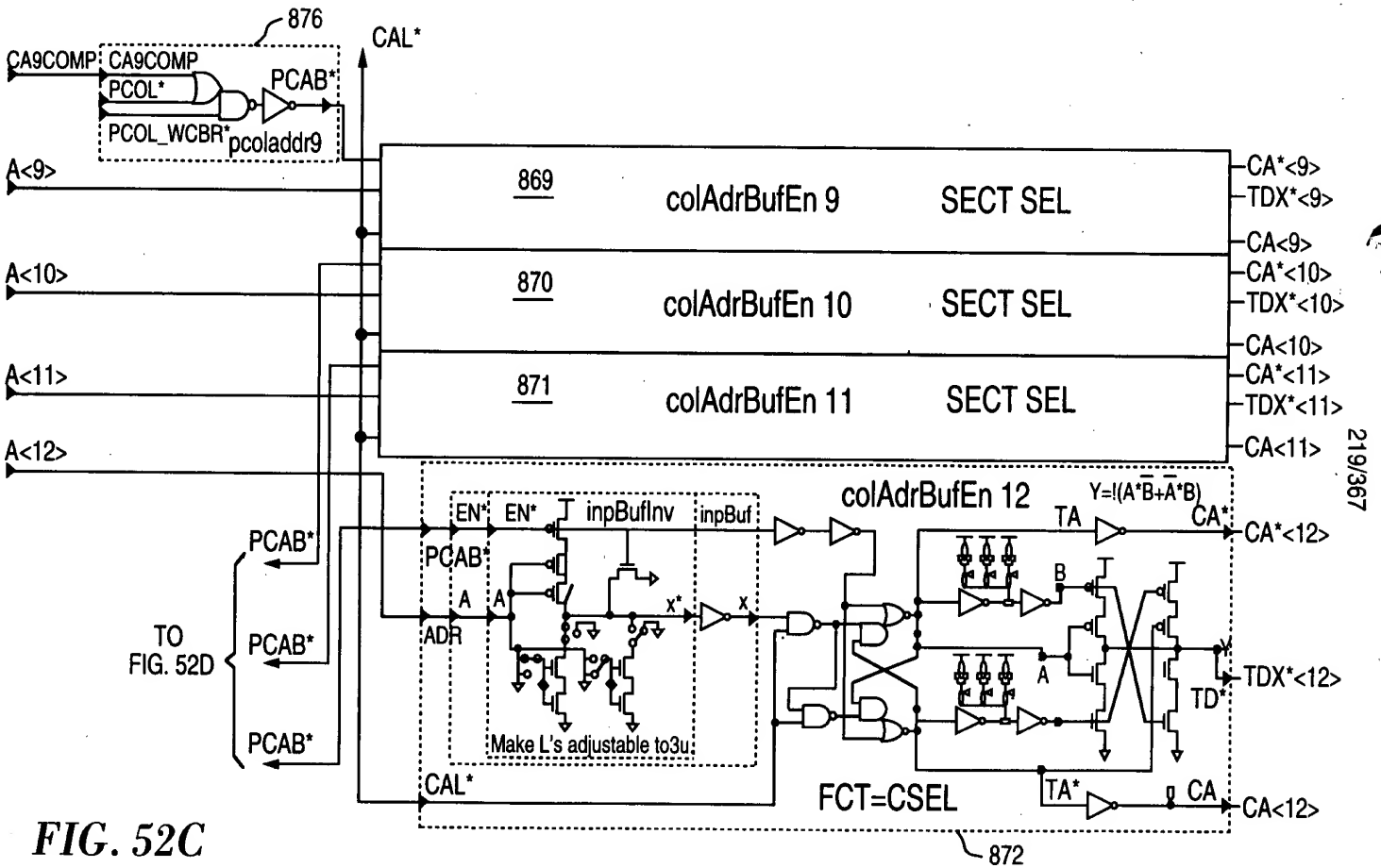

876
CA9COMP
CA9COMP
PCOL*
PCOL_WCBR*
PCAB*
pcoladdr9
CAL*
A<9>
A<10>
A<11>
A<12>
869
colAdrBufEn 9
SECT SEL
870
colAdrBufEn 10
SECT SEL
871
colAdrBufEn 11
SECT SEL
CA*<9>
TDX*<9>
CA9
CA*<10>
TDX*<10>
CA<10>
CA*<11>
TDX*<11>
CA<11>
colAdrBufEn 12
Y=!(A*B̄+Ā*B)
EN*
EN*
inpBufInv
inpBuf
PCAB*
A
A
X*
X
ADR
TA
CA*
CA*<12>
B
A
TDX*<12>
TD*
Make L's adjustable to3u
CAL*
FCT=CSEL
TA*
CA
CA<12>
TO
FIG. 52D
PCAB*
PCAB*
PCAB*
872

FIG. 52C

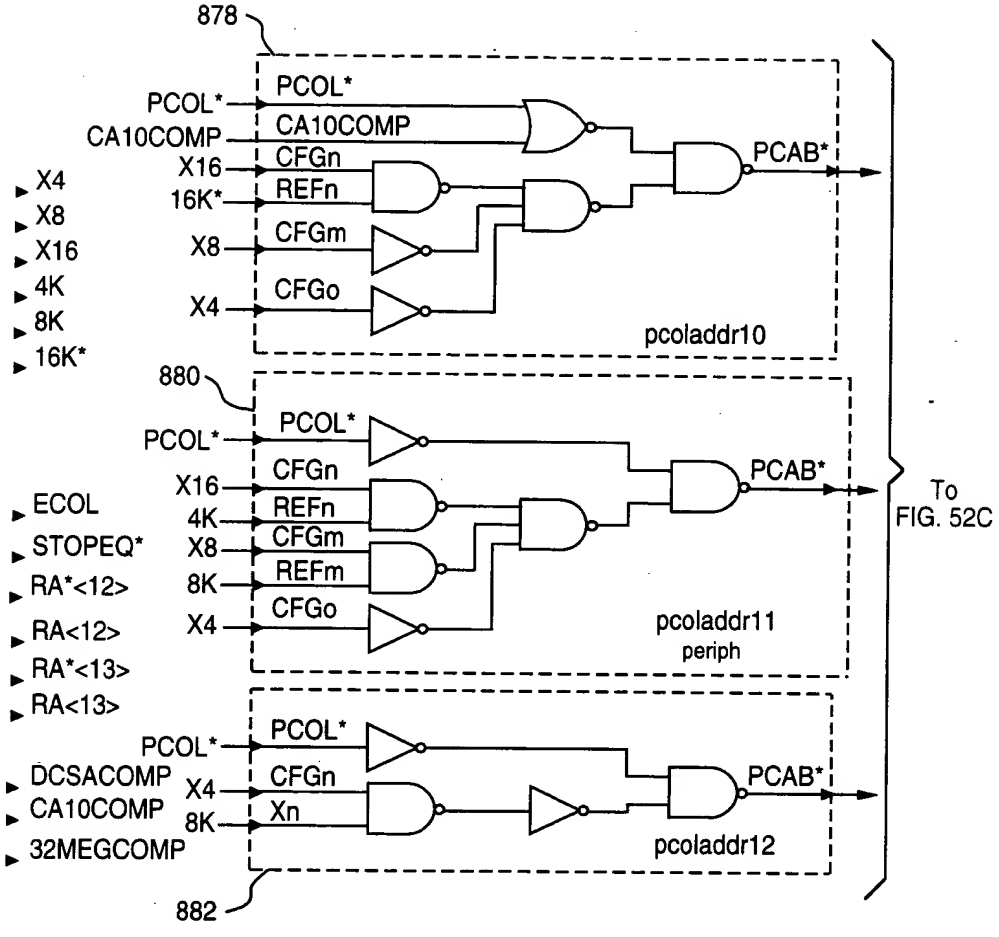

878
PCOL*
CA10COMP
X16
16K*
X8
X4
X4
X8
X16
4K
8K
16K*
CFGn
REFn
CFGm
CFGo
PCAB*
pcoladdr10
880
PCOL*
X16
4K
X8
8K
X4
ECOL
STOPEQ*
RA*<12>
RA<12>
RA*<13>
RA<13>
CFGn
REFn
CFGm
REFm
CFGo
PCAB*
pcoladdr11
periph
PCOL*
DCSACOMP
CA10COMP
32MEGCOMP
X4
8K
CFGn
Xn
PCAB*
pcoladdr12
882
To
FIG. 52C

FIG. 52D

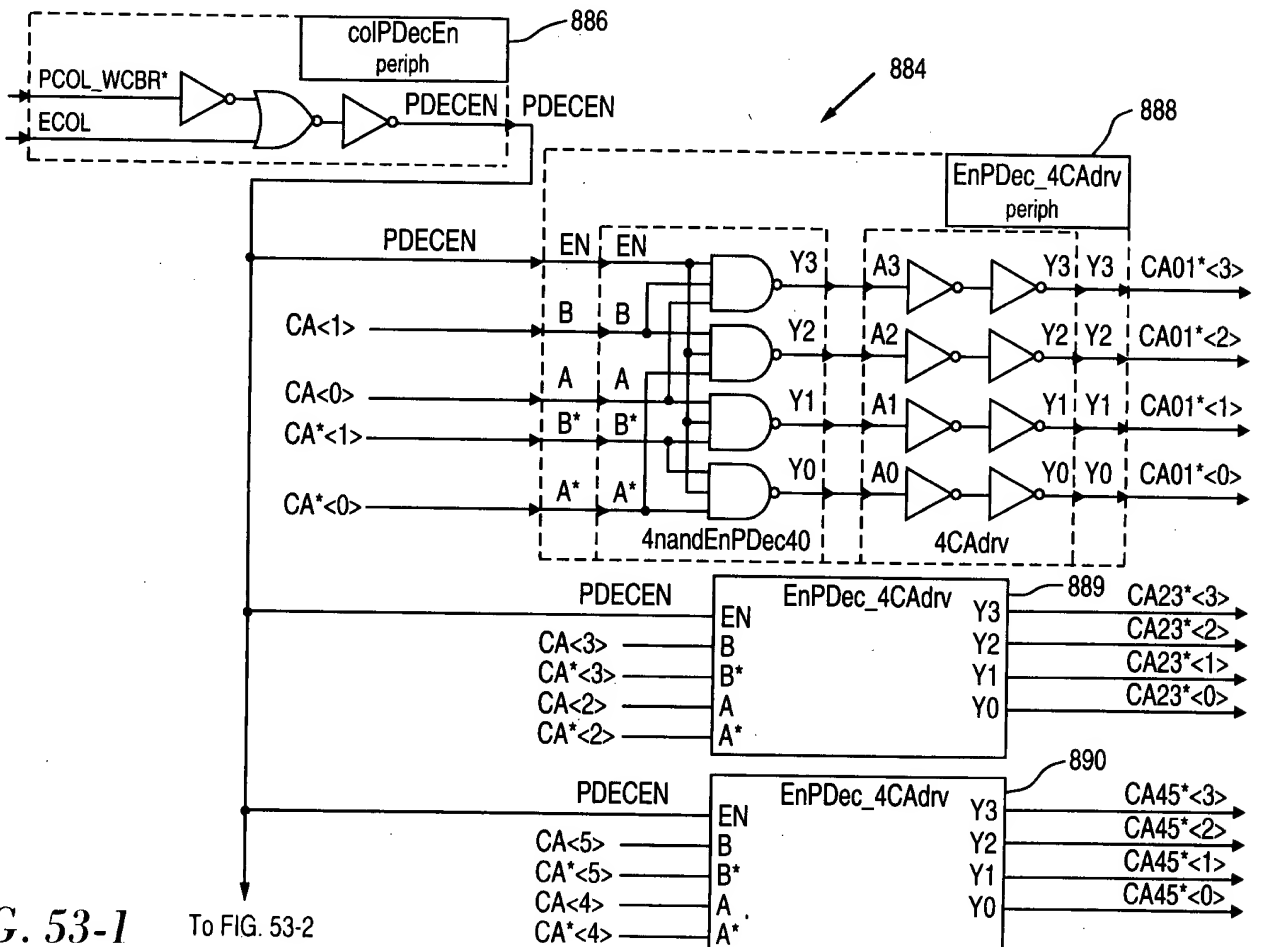

colPDecEn
periph
886
884
888
PCOL_WCBR*
ECOL
PDECEN
PDECEN
EnPDec_4CAdrv
periph
PDECEN
EN
EN
Y3
A3
Y3
Y3
CA01*<3>
CA<1>
B
B
Y2
A2
Y2
Y2
CA01*<2>
CA<0>
A
A
Y1
A1
Y1
Y1
CA01*<1>
CA*<1>
B*
B*
Y0
A0
Y0
Y0
CA01*<0>
CA*<0>
A*
A*
4nandEnPDec40
4CAdrv
PDECEN
EnPDec_4CAdrv
889
EN
B
B*
A
A*
Y3
Y2
Y1
Y0
CA<3>
CA*<3>
CA<2>
CA*<2>
CA23*<3>
CA23*<2>
CA23*<1>
CA23*<0>
PDECEN
EnPDec_4CAdrv
890
EN
B
B*
A
A*
Y3
Y2
Y1
Y0
CA<5>
CA*<5>
CA<4>
CA*<4>
CA45*<3>
CA45*<2>
CA45*<1>
CA45*<0>
To FIG. 53-2

FIG. 53-1

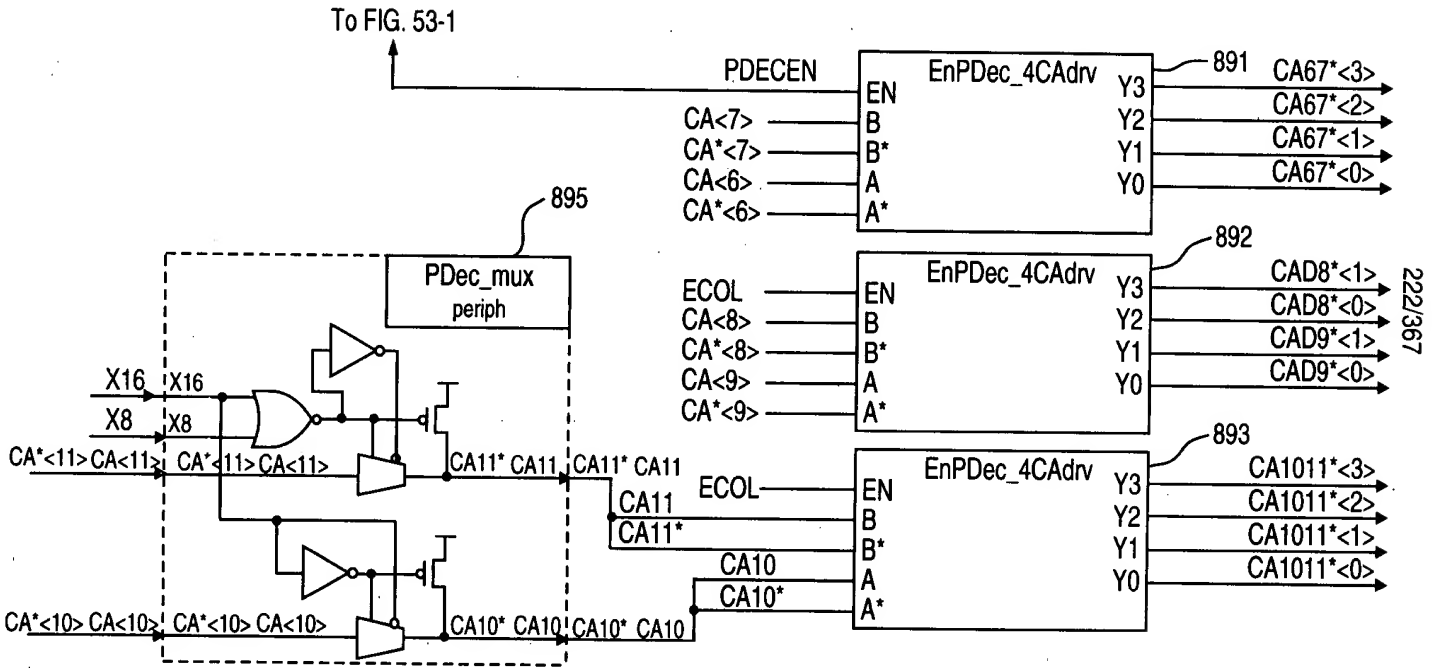

To FIG. 53-1
PDECEN
EnPDec_4CAdrv
EN
B
B*
A
A*
Y3
Y2
Y1
Y0
891
CA67*<3>
CA67*<2>
CA67*<1>
CA67*<0>
CA<7>
CA*<7>
CA<6>
CA*<6>
895
PDec_mux
periph
892
ECOL
CA<8>
CA*<8>
CA<9>
CA*<9>
CAD8*<1>
CAD8*<0>
CAD9*<1>
CAD9*<0>
X16
X8
CA*<11> CA<11>
CA*<11> CA<11>
CA11* CA11
CA11* CA11
CA11
CA11*
893
CA1011*<3>
CA1011*<2>
CA1011*<1>
CA1011*<0>
CA10
CA10*
CA*<10> CA<10>
CA*<10> CA<10>
CA10* CA10
CA10* CA10

FIG. 53-2

TOSHIBA 0010660

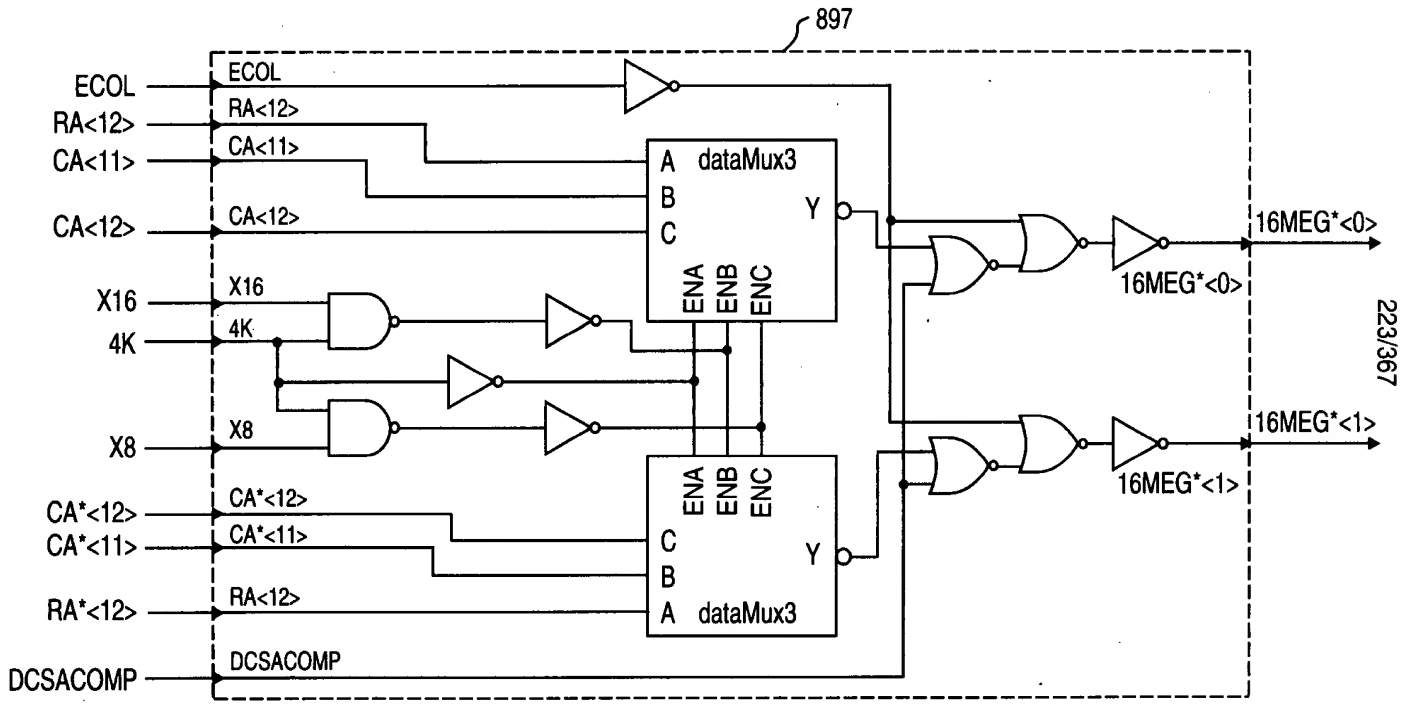


FIG. 54A

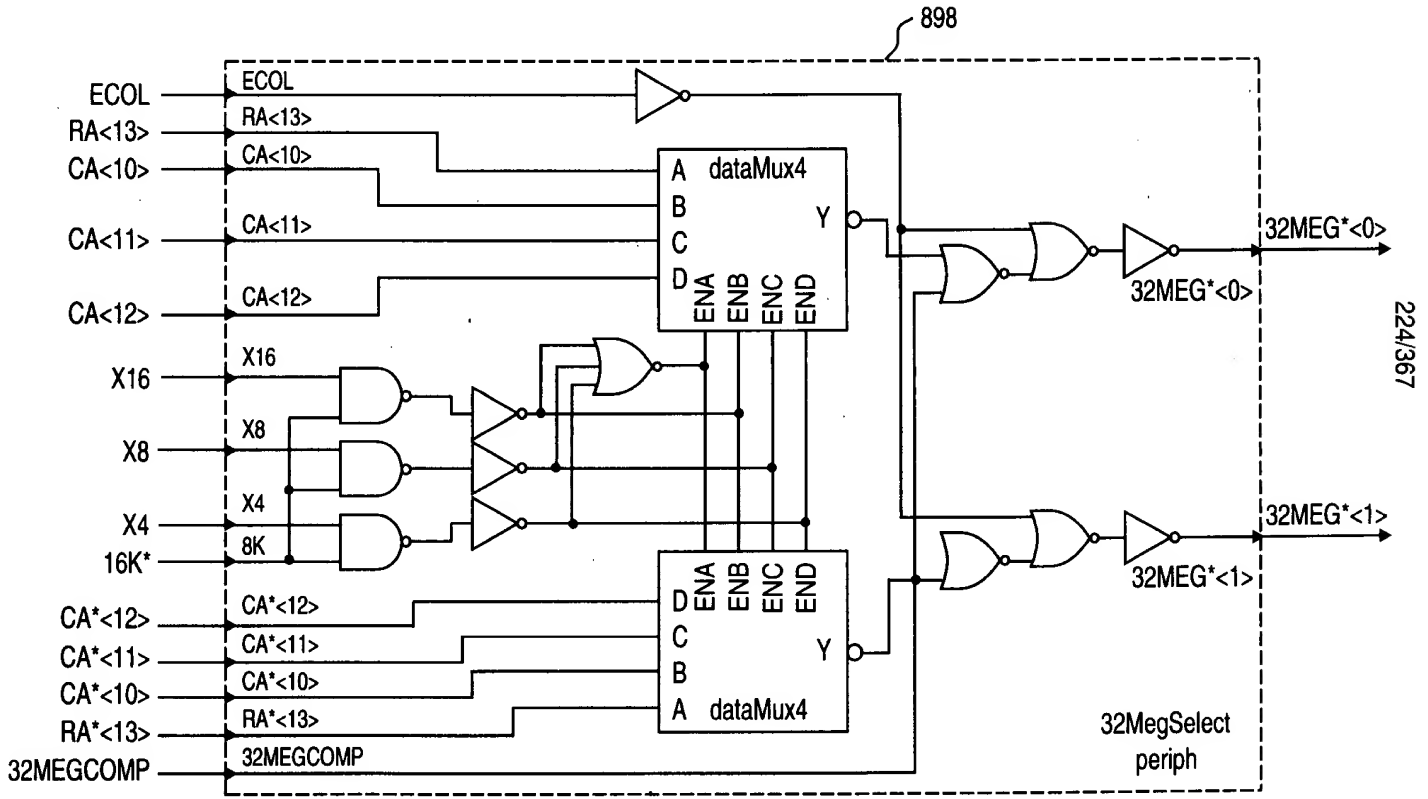

898
ECOL
RA<13>
CA<10>
CA<11>
CA<12>
X16
X8
X4
16K*
CA*<12>
CA*<11>
CA*<10>
RA*<13>
32MEGCOMP
A
B
C
D
dataMux4
Y
ENA
ENB
ENC
END
32MEG*<0>
32MEG*<1>
32MegSelect
periph
224/367

FIG. 54B

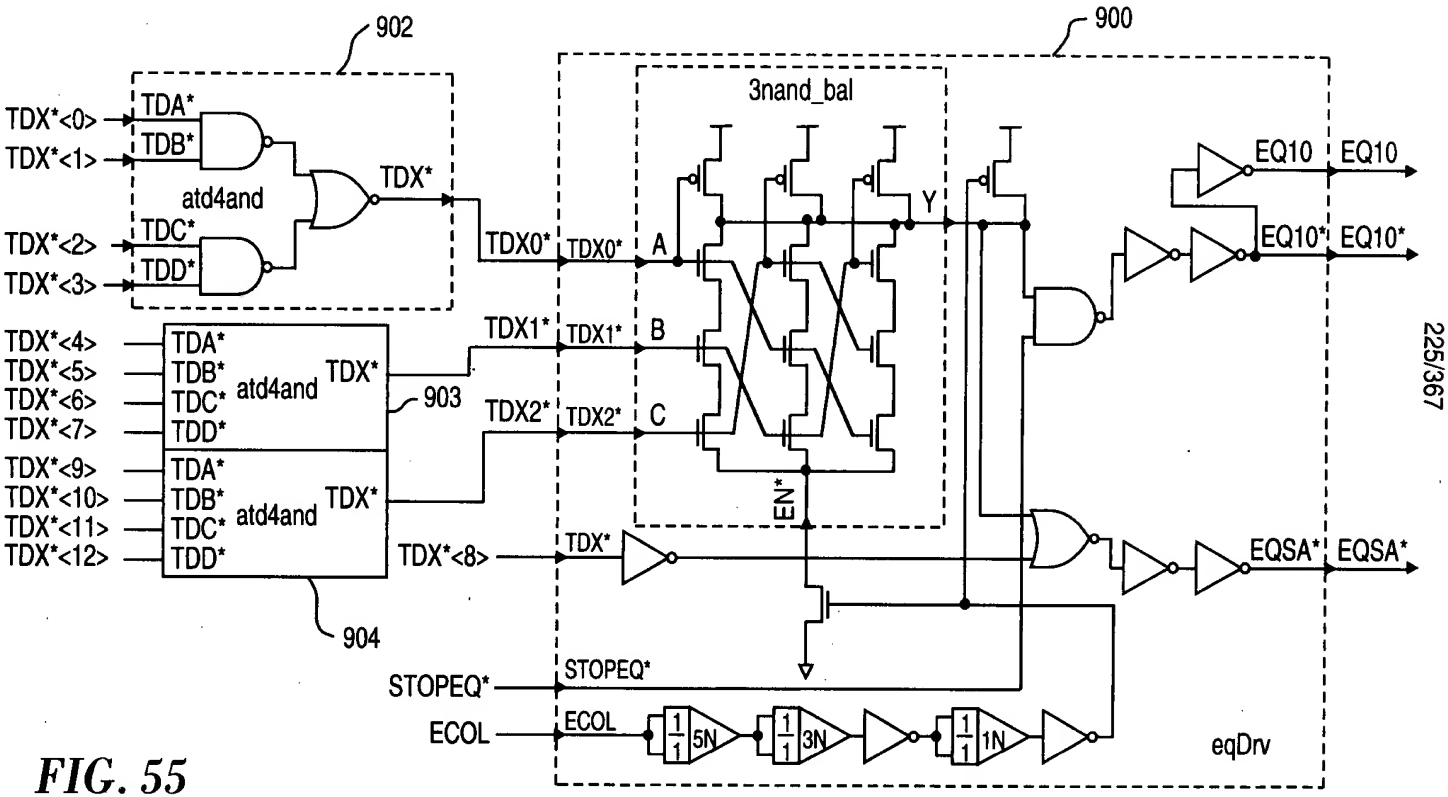

902
900
3nand_bal
TDX*<0>
TDX*<1>
TDX*<2>
TDX*<3>
TDA*
TDB*
TDC*
TDD*
atd4and
TDX*
TDX0*
TDX*<4>
TDX*<5>
TDX*<6>
TDX*<7>
TDX1*
903
TDX*<9>
TDX*<10>
TDX*<11>
TDX*<12>
TDX2*
904
TDX*<8>
A
B
C
Y
EN*
EQ10
EQ10*
EQSA*
STOPEQ*
ECOL
5N
3N
1N
eqDrv
225/367

FIG. 55

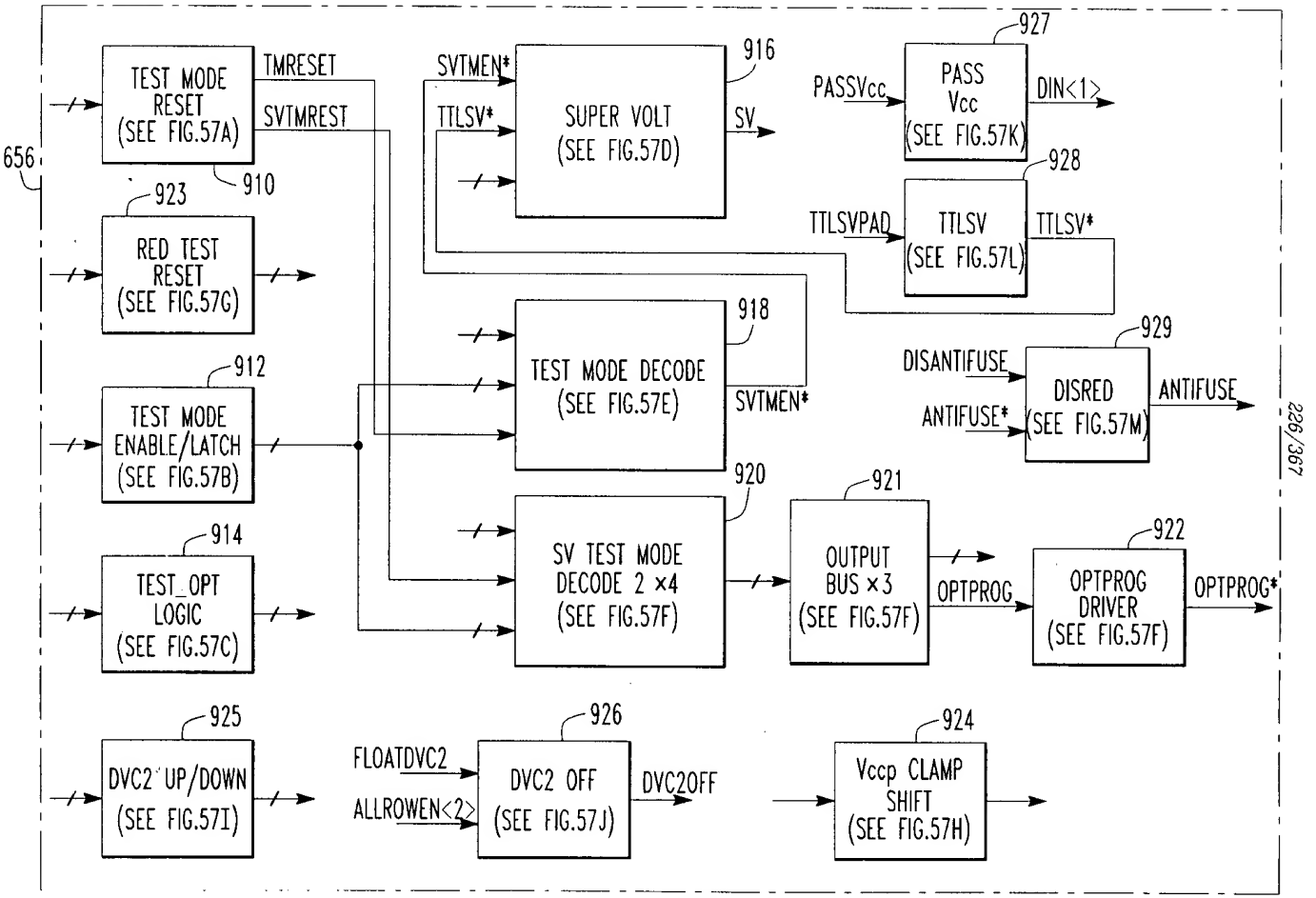

656
TEST MODE RESET (SEE FIG.57A)
TMRESET
SVTMREST
910
923
RED TEST RESET (SEE FIG.57G)
912
TEST MODE ENABLE/LATCH (SEE FIG.57B)
914
TEST_OPT LOGIC (SEE FIG.57C)
925
DVC2 UP/DOWN (SEE FIG.57I)
SVTMEN*
TTLSV*
916
SUPER VOLT (SEE FIG.57D)
SV
927
PASSVcc
PASS Vcc (SEE FIG.57K)
DIN<1>
928
TTLSVPAD
TTLSV (SEE FIG.57L)
TTLSV*
918
TEST MODE DECODE (SEE FIG.57E)
SVTMEN*
929
DISANTIFUSE
ANTIFUSE*
DISRED (SEE FIG.57M)
ANTIFUSE
920
SV TEST MODE DECODE 2 x4 (SEE FIG.57F)
921
OUTPUT BUS x3 (SEE FIG.57F)
OPTPROG
922
OPTPROG DRIVER (SEE FIG.57F)
OPTPROG*
FLOATDVC2
ALLROWEN<2>
926
DVC2 OFF (SEE FIG.57J)
DVC2OFF
924
Vccp CLAMP SHIFT (SEE FIG.57H)
226/367

FIG. 56

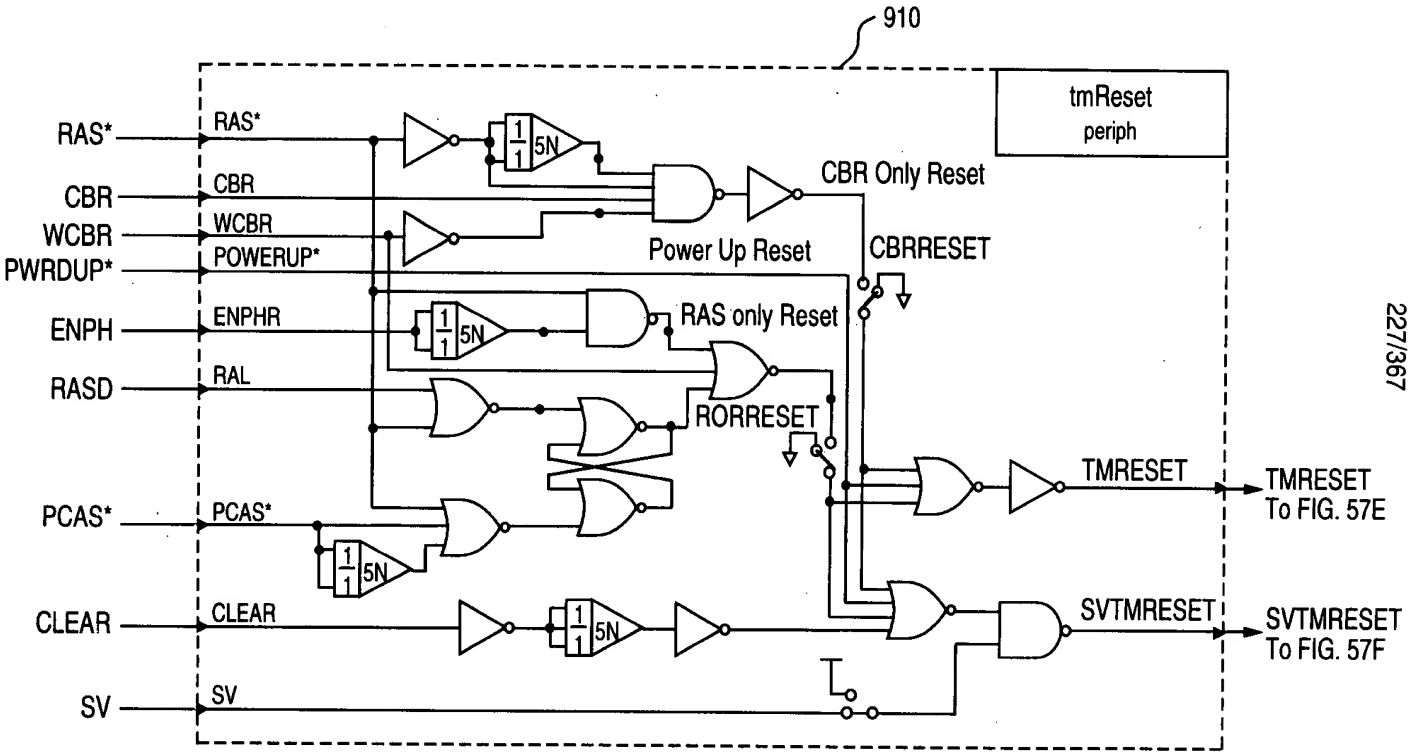

910
tmReset
periph
RAS*
CBR
WCBR
PWRDUP*
ENPH
RASD
PCAS*
CLEAR
SV
RAS*
CBR
WCBR
POWERUP*
ENPHR
RAL
PCAS*
CLEAR
SV
1/1 5N
CBR Only Reset
Power Up Reset
CBRRESET
RAS only Reset
RORRESET
TMRESET
TMRESET
To FIG. 57E
SVTMRESET
SVTMRESET
To FIG. 57F

FIG. 57A

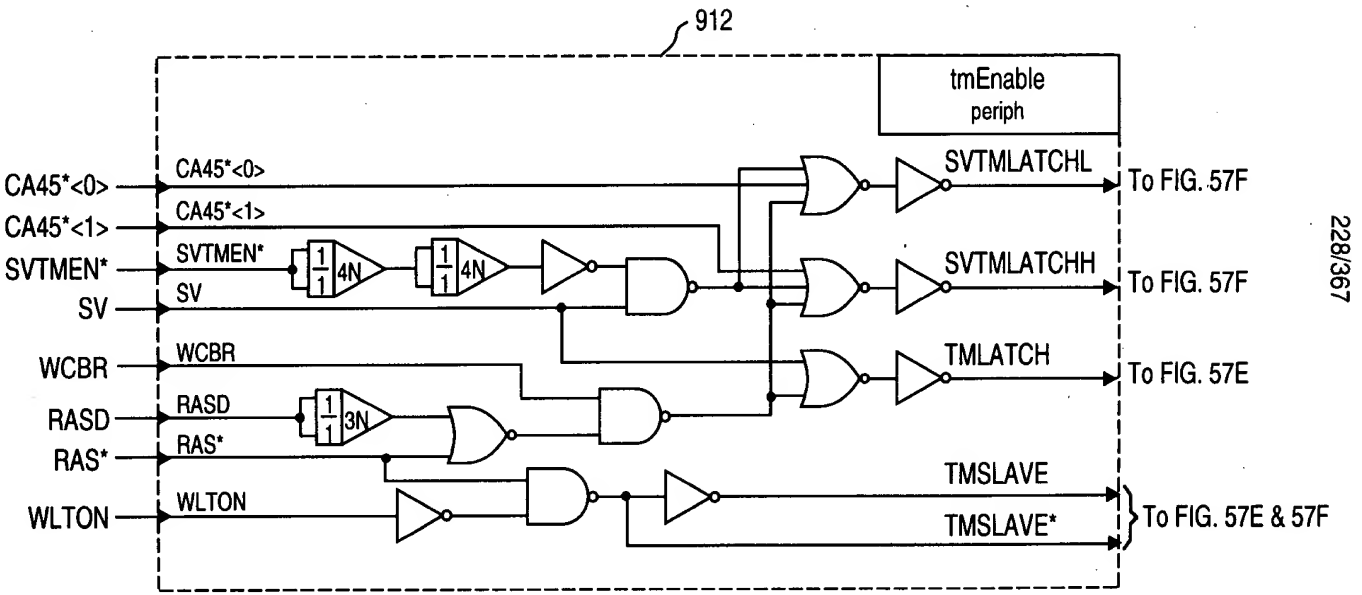

912
tmEnable
periph
CA45*<0>
CA45*<1>
SVTMEN*
SV
WCBR
RASD
RAS*
WLTON
CA45*<0>
CA45*<1>
SVTMEN*
SV
WCBR
RASD
RAS*
WLTON
1/1 4N
1/1 4N
1/1 3N
SVTMLATCHL
SVTMLATCHH
TMLATCH
TMSLAVE
TMSLAVE*
To FIG. 57F
To FIG. 57F
To FIG. 57E
To FIG. 57E & 57F

FIG. 57B

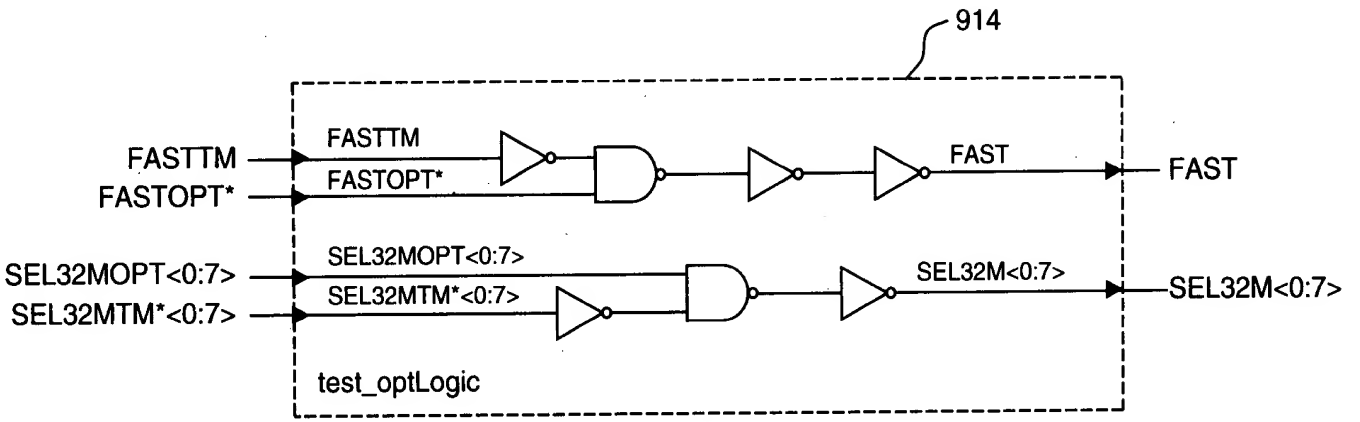

914
FASTTM
FASTOPT*
FASTTM
FASTOPT*
FAST
FAST
SEL32MOPT<0:7>
SEL32MTM*<0:7>
SEL32MOPT<0:7>
SEL32MTM*<0:7>
SEL32M<0:7>
SEL32M<0:7>
test_optLogic

FIG. 57C

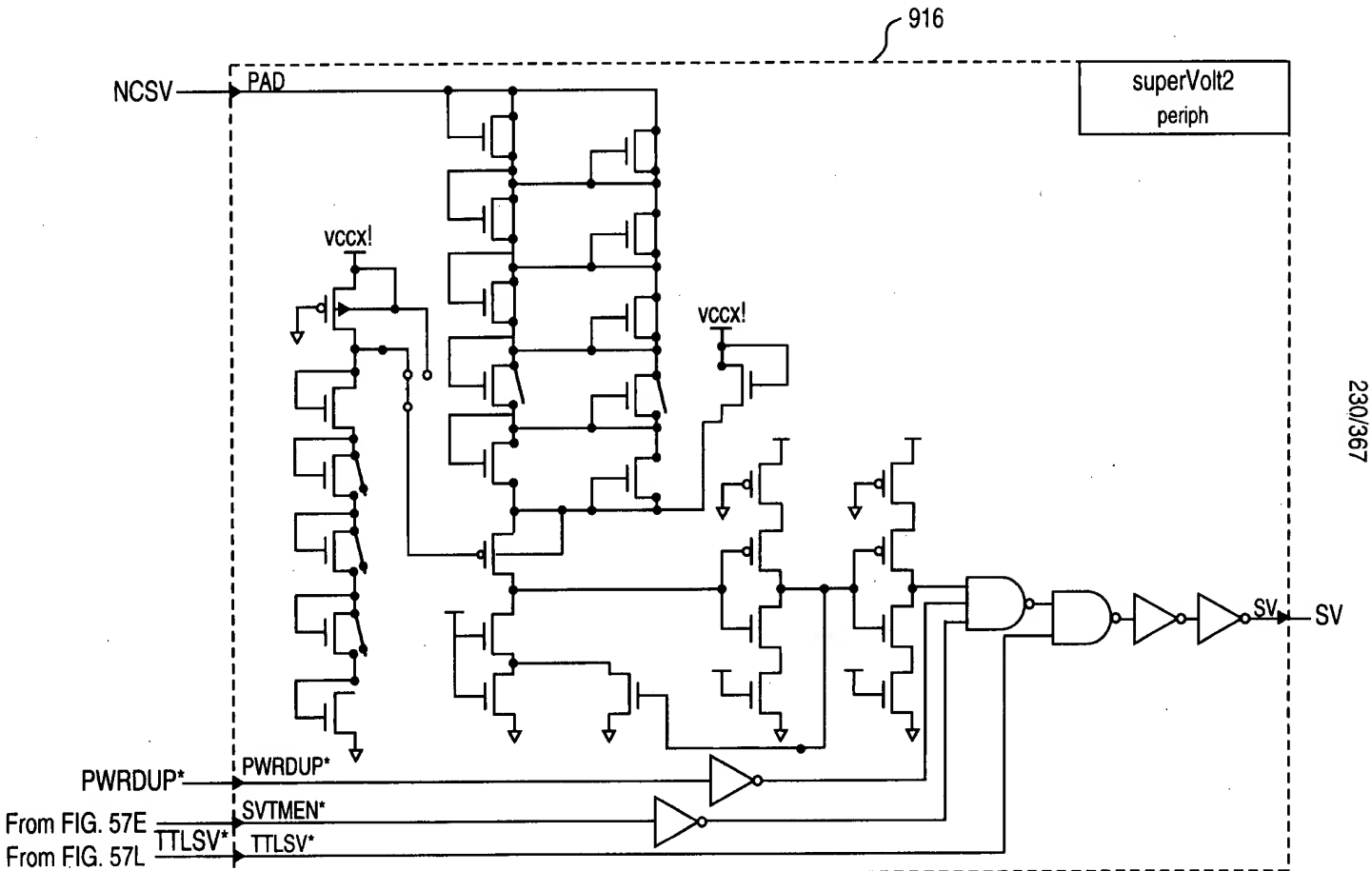

916
NCSV
PAD
superVolt2
periph
VCCX!
VCCX!
SV
SV
PWRDUP*
PWRDUP*
From FIG. 57E
SVTMEN*
From FIG. 57L
TTLSV*
TTLSV*

FIG. 57D

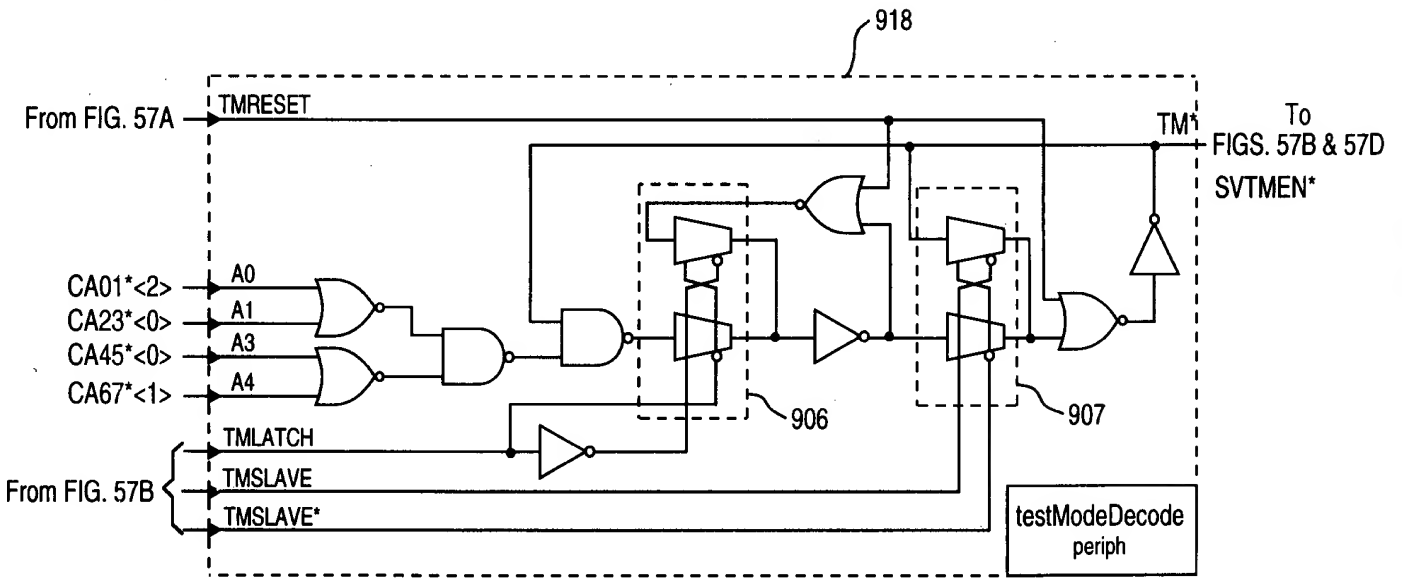

918
From FIG. 57A
TMRESET
TM*
To
FIGS. 57B & 57D
SVTMEN*
CA01*<2>
CA23*<0>
CA45*<0>
CA67*<1>
A0
A1
A3
A4
906
907
TMLATCH
From FIG. 57B
TMSLAVE
TMSLAVE*
testModeDecode
periph

FIG. 57E

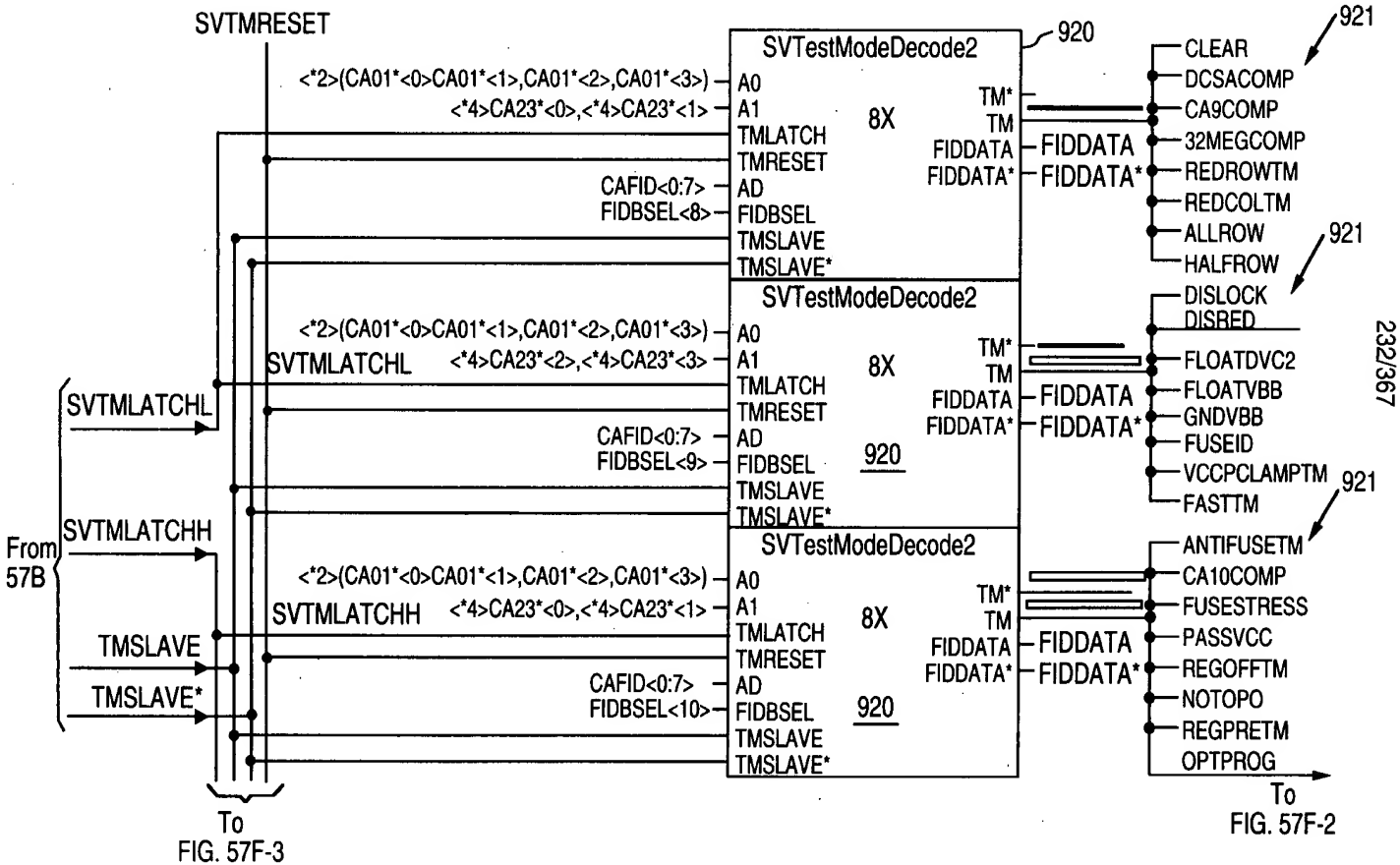

SVTMRESET
SVTestModeDecode2
920
921
A0
A1
TMLATCH
TMRESET
AD
FIDBSEL
TMSLAVE
TMSLAVE*
8X
TM*
TM
FIDDATA
FIDDATA*
CLEAR
DCSACOMP
CA9COMP
32MEGCOMP
REDROWTM
REDCOLTM
ALLROW
HALFROW
DISLOCK
DISRED
FLOATDVC2
FLOATVBB
GNDVBB
FUSEID
VCCPCLAMPTM
FASTTM
ANTIFUSETM
CA10COMP
FUSESTRESS
PASSVCC
REGOFFTM
NOTOPO
REGPRETM
OPTPROG
<*2>(CA01*<0>CA01*<1>,CA01*<2>,CA01*<3>)
<*4>CA23*<0>,<*4>CA23*<1>
<*4>CA23*<2>,<*4>CA23*<3>
CAFID<0:7>
FIDBSEL<8>
FIDBSEL<9>
FIDBSEL<10>
SVTMLATCHL
SVTMLATCHH
From 57B
TMSLAVE
TMSLAVE*
To FIG. 57F-3
To FIG. 57F-2
232/367

FIG. 57F-1

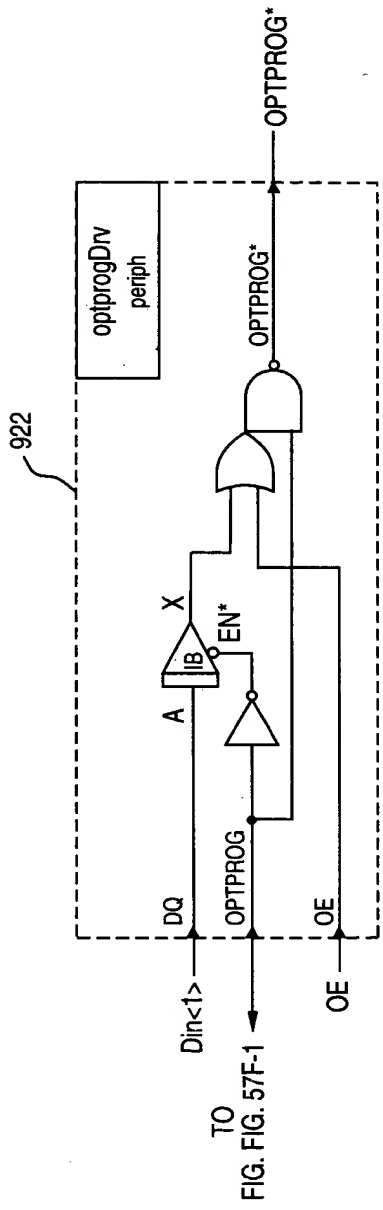

922
optprogDrv
periph
OPTPROG*
OPTPROG*
X
A
IB
EN*
DQ
OPTPROG
OE
Din<1>
OE
TO
FIG. FIG. 57F-1

FIG. 57F-2

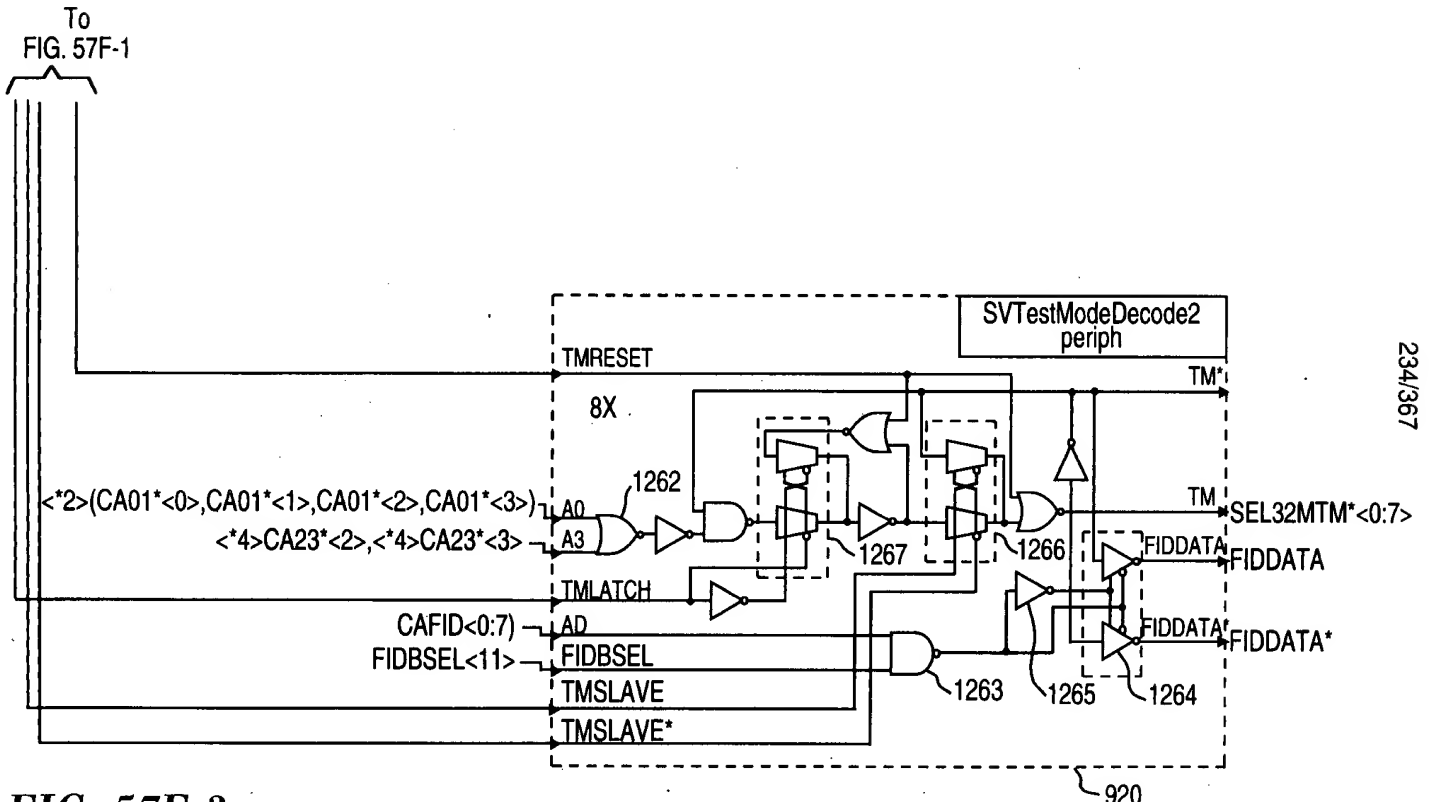

To
FIG. 57F-1
SVTestModeDecode2
periph
TMRESET
8X
TM*
1262
<*2>(CA01*<0>,CA01*<1>,CA01*<2>,CA01*<3>)
A0
A3
<*4>CA23*<2>,<*4>CA23*<3>
TM
SEL32MTM*<0:7>
1267
1266
FIDDATA
FIDDATA
TMLATCH
CAFID<0:7)
AD
FIDBSEL<11>
FIDBSEL
FIDDATA*
FIDDATA*
TMSLAVE
TMSLAVE*
1263
1265
1264
920

FIG. 57F-3

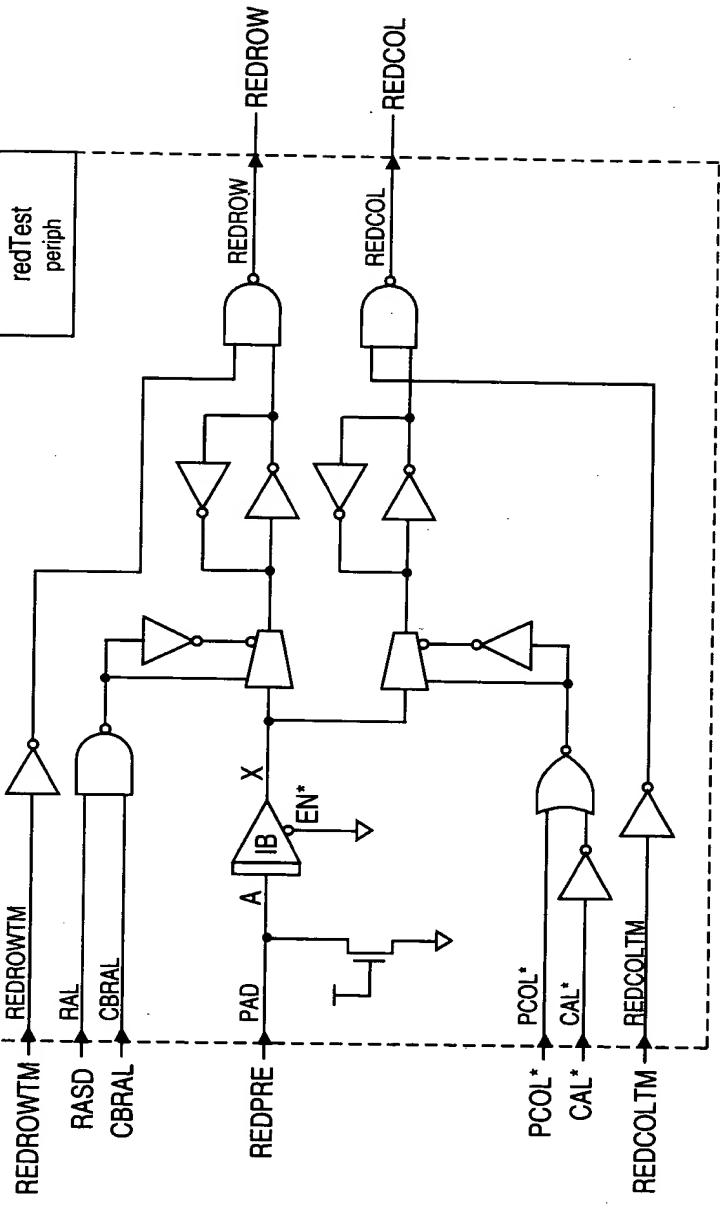

923
redTest
periph
REDROW
REDCOL
REDROWTM
RASD
CBRAL
REDPRE
PCOL*
CAL*
REDCOLTM
RAL
PAD
A
X
IB
EN*
PCOL*
CAL*
REDCOLTM

FIG. 57G

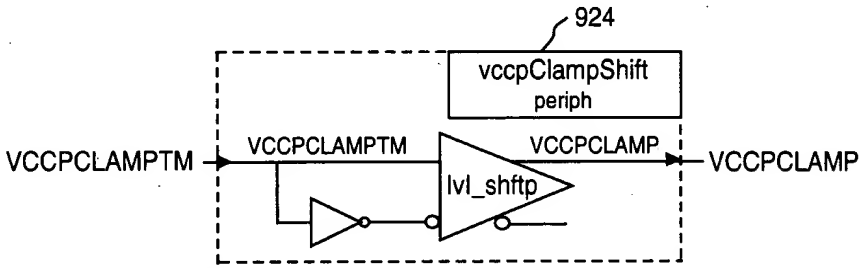


FIG. 57H

09815229 - 020801

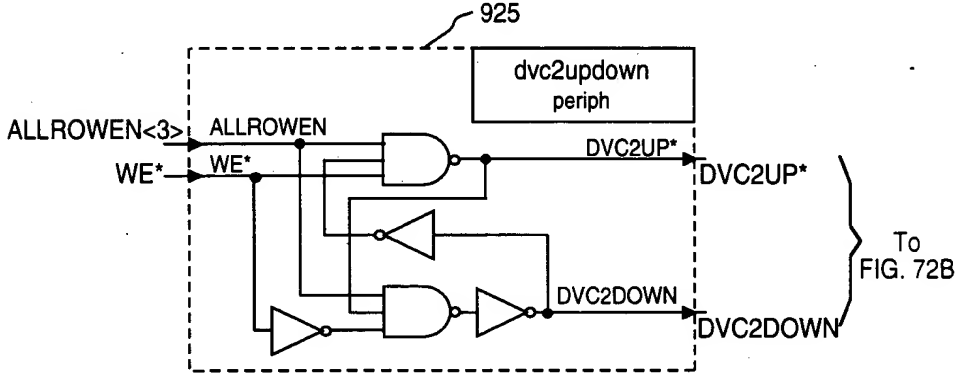

925
dvc2updown
periph
ALLROWEN<3>
ALLROWEN
WE*
WE*
DVC2UP*
DVC2UP*
DVC2DOWN
DVC2DOWN
To
FIG. 72B

FIG. 57I

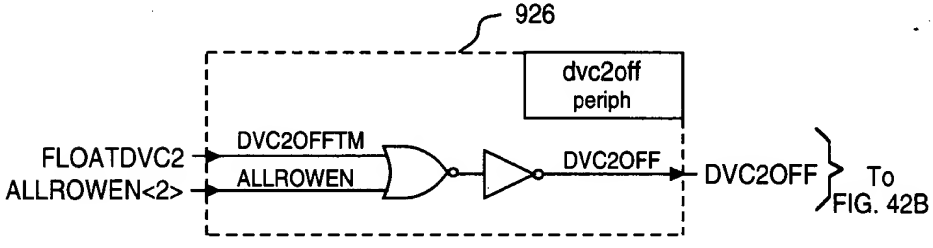


FIG. 57J

Petitioner - Ex. 1003 - Page 238

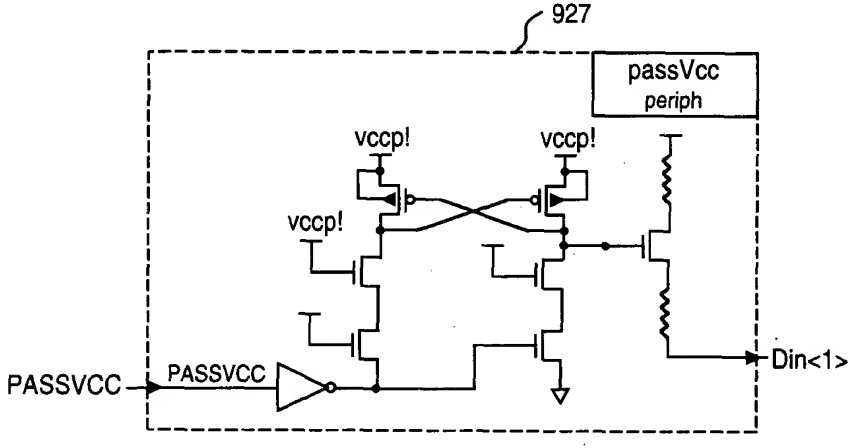


FIG. 57K

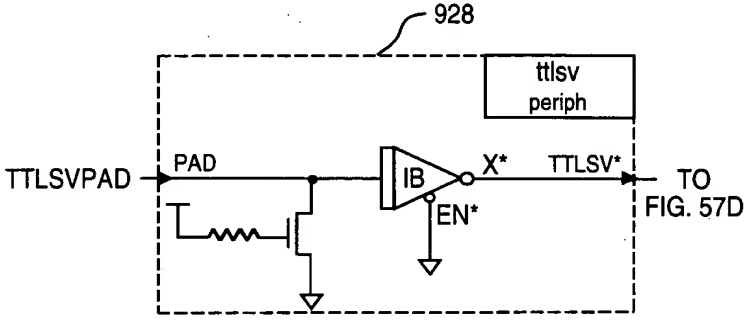


FIG. 57L

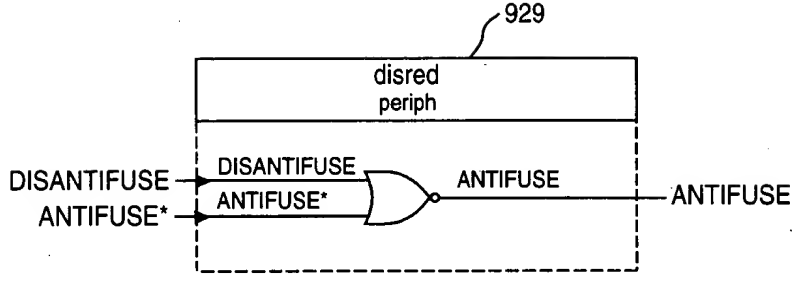

929
disred
periph
DISANTIFUSE
ANTIFUSE*
DISANTIFUSE
ANTIFUSE*
ANTIFUSE
ANTIFUSE

FIG. 57M

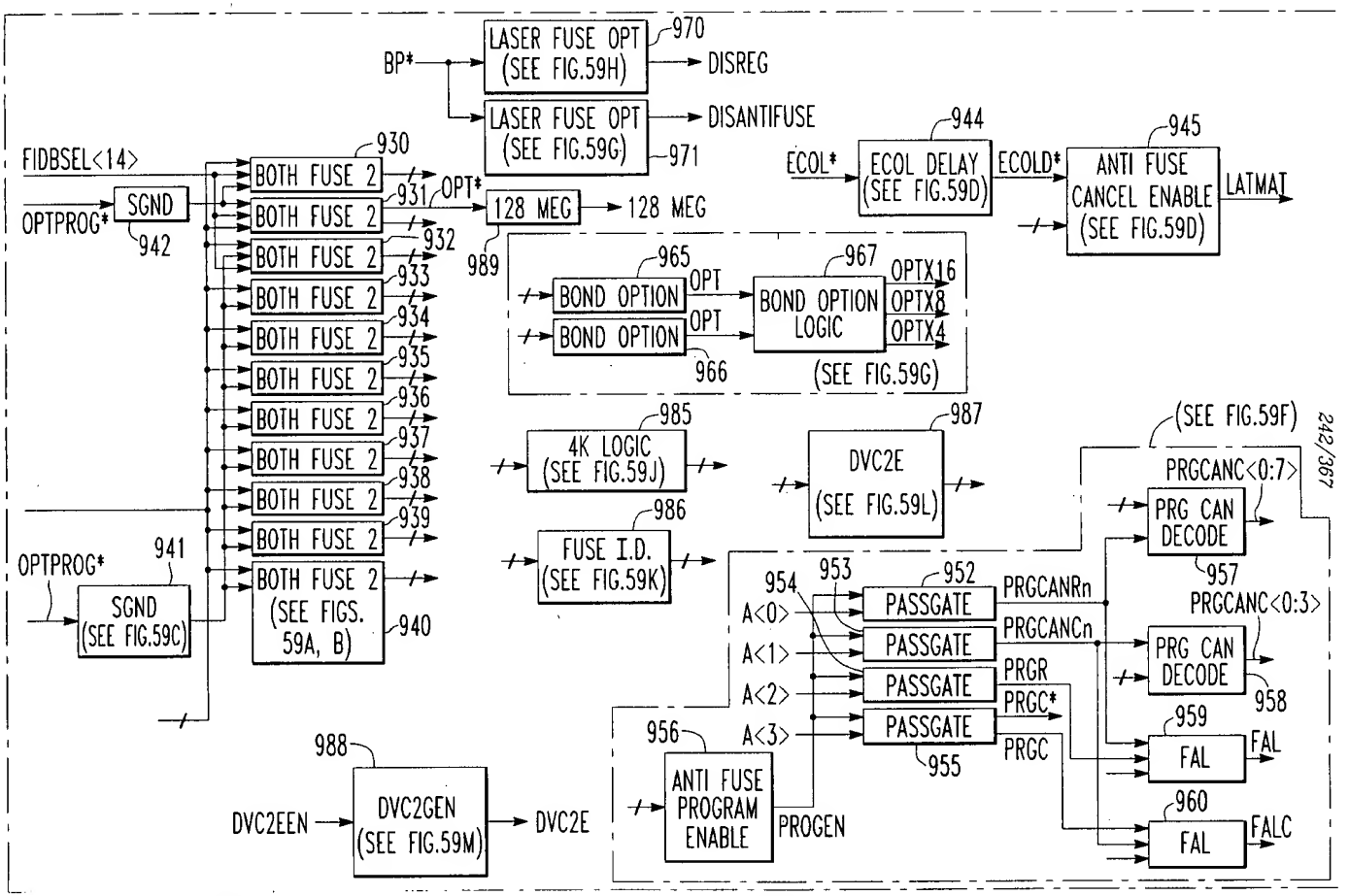

LASER FUSE OPT (SEE FIG.59H)
970
BP*
DISREG
LASER FUSE OPT (SEE FIG.59G)
971
DISANTIFUSE
944
ECOL*
ECOL DELAY (SEE FIG.59D)
ECOLD*
945
ANTI FUSE CANCEL ENABLE (SEE FIG.59D)
LATMAT
FIDBSEL<14>
OPTPROG*
SGND
942
930
BOTH FUSE 2
931
932
933
934
935
936
937
938
939
OPT*
128 MEG
128 MEG
989
965
BOND OPTION
966
967
BOND OPTION LOGIC
OPTX16
OPTX8
OPTX4
(SEE FIG.59G)
985
4K LOGIC (SEE FIG.59J)
987
DVC2E (SEE FIG.59L)
986
FUSE I.D. (SEE FIG.59K)
(SEE FIG.59F)
242/367
PRGCANC<0:7>
PRG CAN DECODE
957
PRGCANC<0:3>
PRG CAN DECODE
958
941
OPTPROG*
SGND (SEE FIG.59C)
940
BOTH FUSE 2 (SEE FIGS. 59A, B)
954
953
952
A<0>
A<1>
A<2>
A<3>
PASSGATE
PASSGATE
PASSGATE
PASSGATE
955
PRGCANRn
PRGCANCn
PRGR
PRGC*
PRGC
959
FAL
FAL
960
FAL
FALC
956
ANTI FUSE PROGRAM ENABLE
PROGEN
988
DVC2EEN
DVC2GEN (SEE FIG.59M)
DVC2E

FIG. 58A

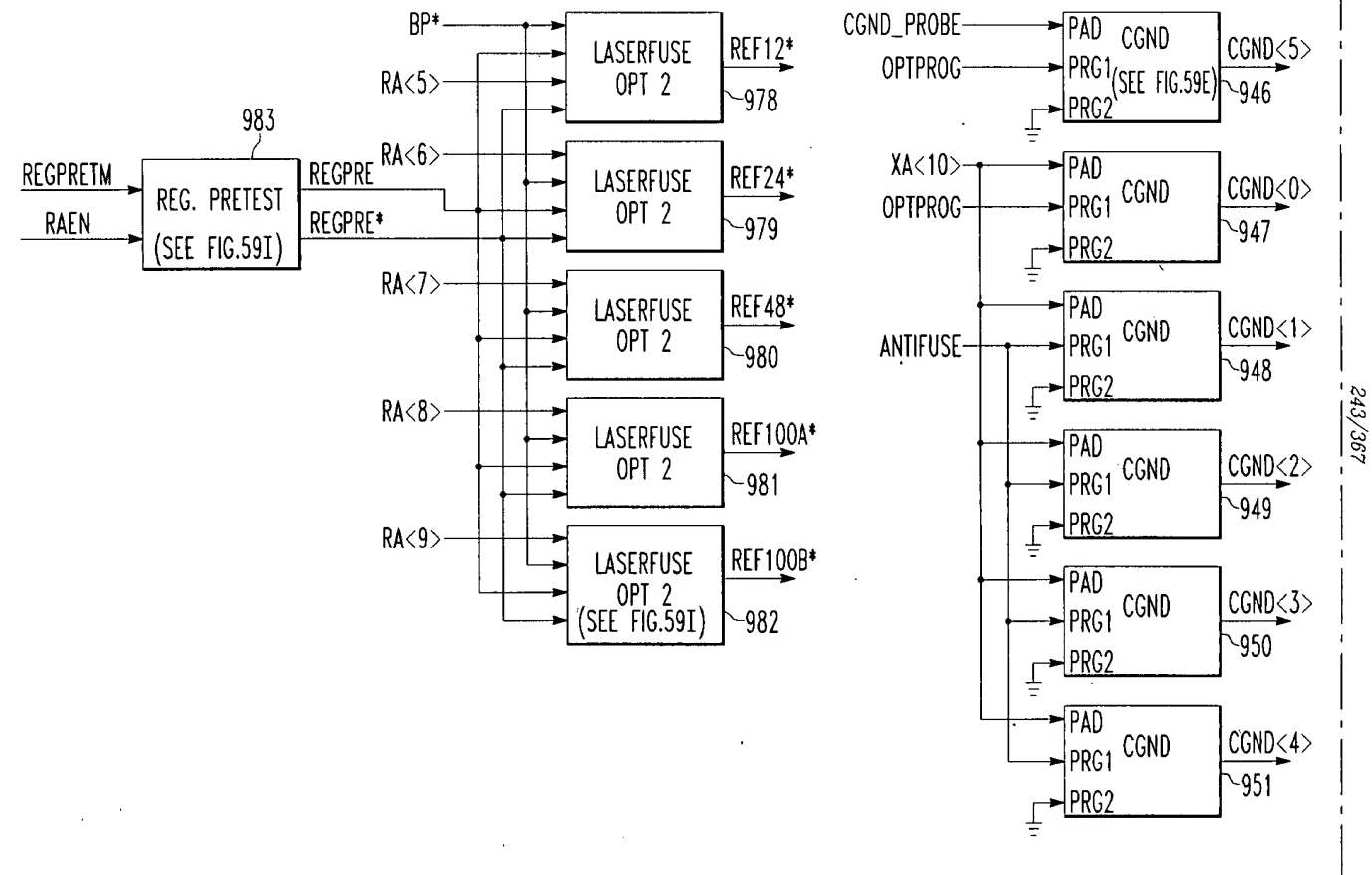

983
REGPRETM
RAEN
REG. PRETEST
(SEE FIG.59I)
REGPRE
REGPRE*
BP*
RA<5>
RA<6>
RA<7>
RA<8>
RA<9>
LASERFUSE OPT 2
LASERFUSE OPT 2
LASERFUSE OPT 2
LASERFUSE OPT 2
LASERFUSE OPT 2 (SEE FIG.59I)
REF12*
978
REF24*
979
REF48*
980
REF100A*
981
REF100B*
982
CGND_PROBE
OPTPROG
XA<10>
OPTPROG
ANTIFUSE
PAD
PRG1
PRG2
CGND
(SEE FIG.59E)
CGND<5>
946
CGND<0>
947
CGND<1>
948
CGND<2>
949
CGND<3>
950
CGND<4>
951
658

FIG. 58B

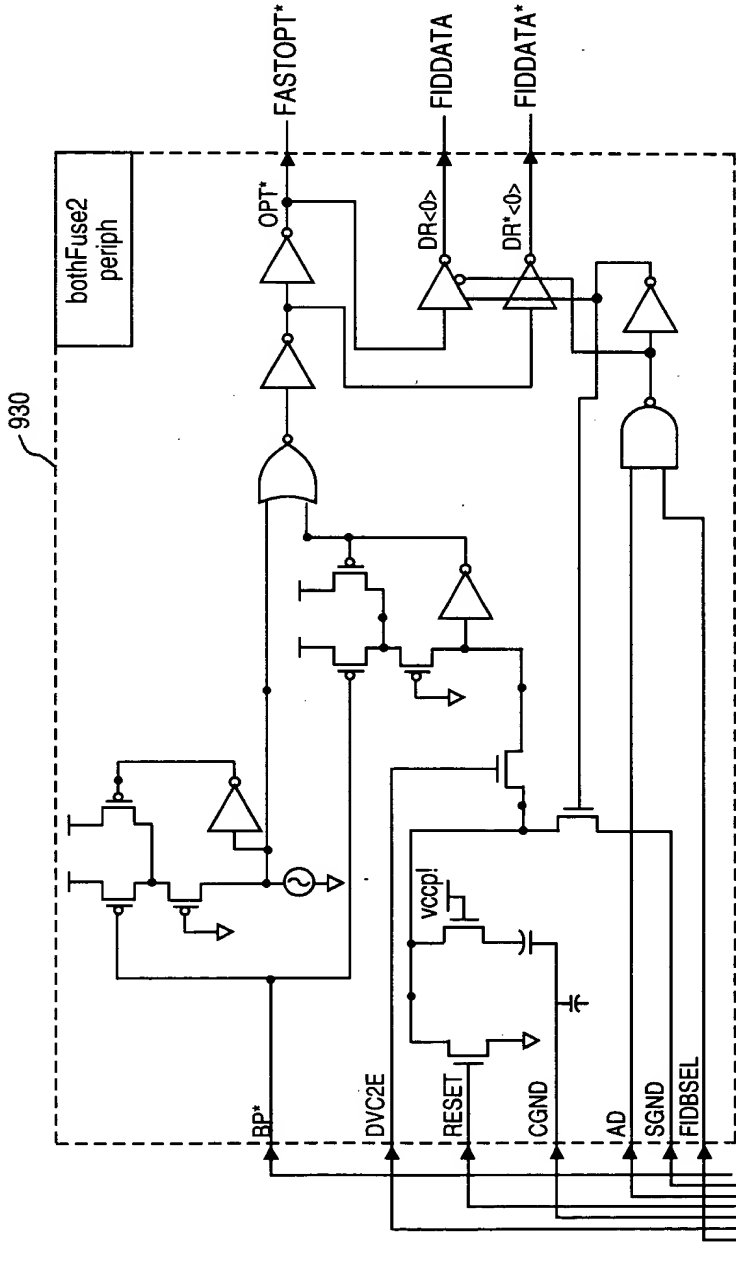

930
bothFuse2
periph
FASTOPT*
FIDDATA
FIDDATA*
OPT*
DR<0>
DR*<0>
vccp!
BP*
DVC2E
RESET
CGND
AD
SGND
FIDBSEL
To
FIG. 59B

FIG. 59A

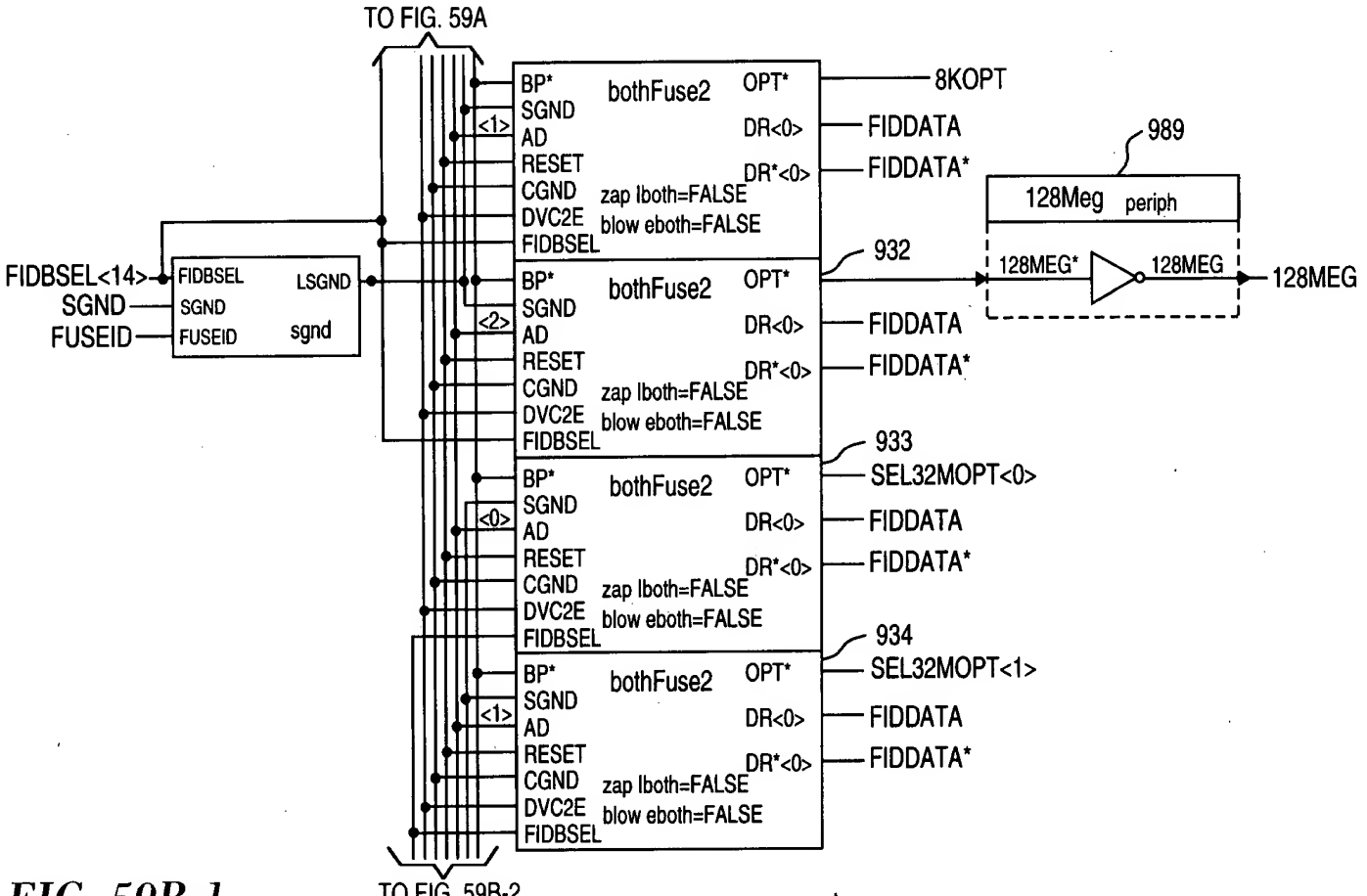

TO FIG. 59A
FIDBSEL<14>
SGND
FUSEID
FIDBSEL
SGND
FUSEID
LSGND
sgnd
BP*
SGND
AD
RESET
CGND
DVC2E
FIDBSEL
bothFuse2
OPT*
DR<0>
DR*<0>
zap Iboth=FALSE
blow eboth=FALSE
<1>
<2>
<0>
8KOPT
FIDDATA
FIDDATA*
989
128Meg periph
932
128MEG*
128MEG
933
SEL32MOPT<0>
934
SEL32MOPT<1>
TO FIG. 59B-2

FIG. 59B-1

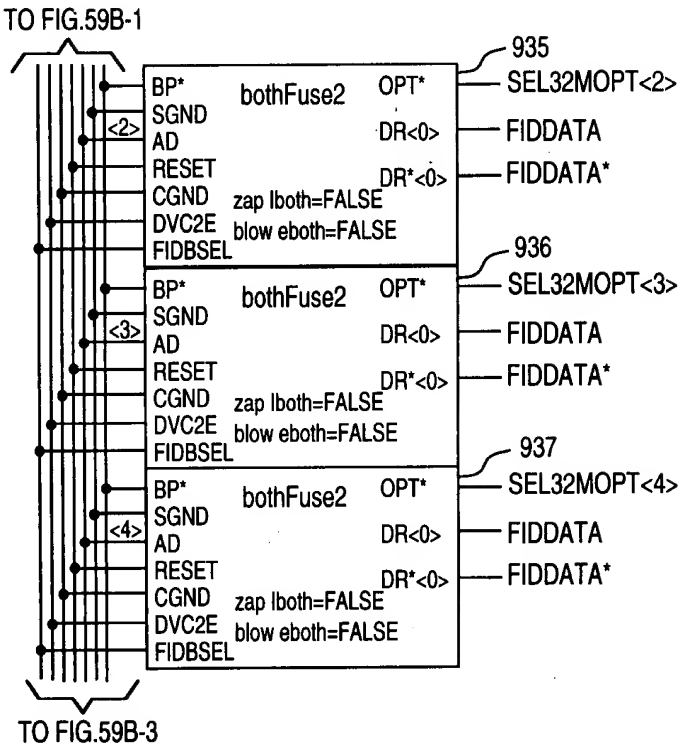

TO FIG.59B-1
935
936
937
BP*
SGND
AD
RESET
CGND
DVC2E
FIDBSEL
bothFuse2
OPT*
DR<0>
DR*<0>
zap Iboth=FALSE
blow eboth=FALSE
<2>
<3>
<4>
SEL32MOPT<2>
SEL32MOPT<3>
SEL32MOPT<4>
FIDDATA
FIDDATA*
TO FIG.59B-3

FIG. 59B-2

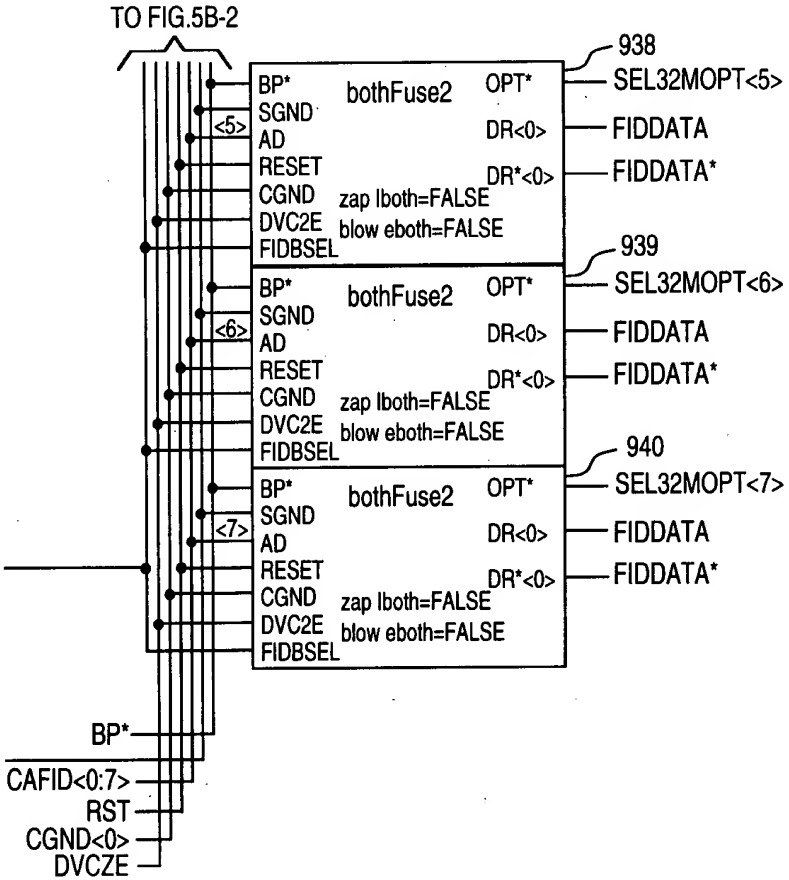

TO FIG.5B-2
938
939
940
bothFuse2
BP*
SGND
AD
RESET
CGND
DVC2E
FIDBSEL
OPT*
DR<0>
DR*<0>
zap Iboth=FALSE
blow eboth=FALSE
<5>
<6>
<7>
SEL32MOPT<5>
SEL32MOPT<6>
SEL32MOPT<7>
FIDDATA
FIDDATA*
BP*
CAFID<0:7>
RST
CGND<0>
DVCZE

FIG. 59B-3

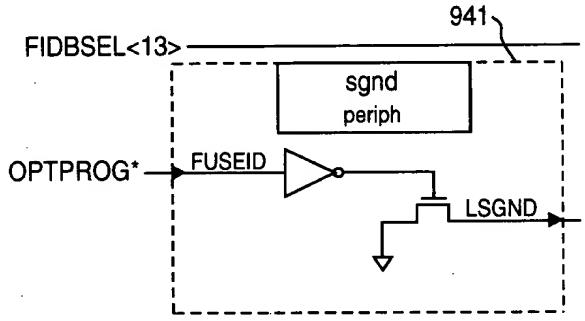


FIG. 59C

0090152.0020014

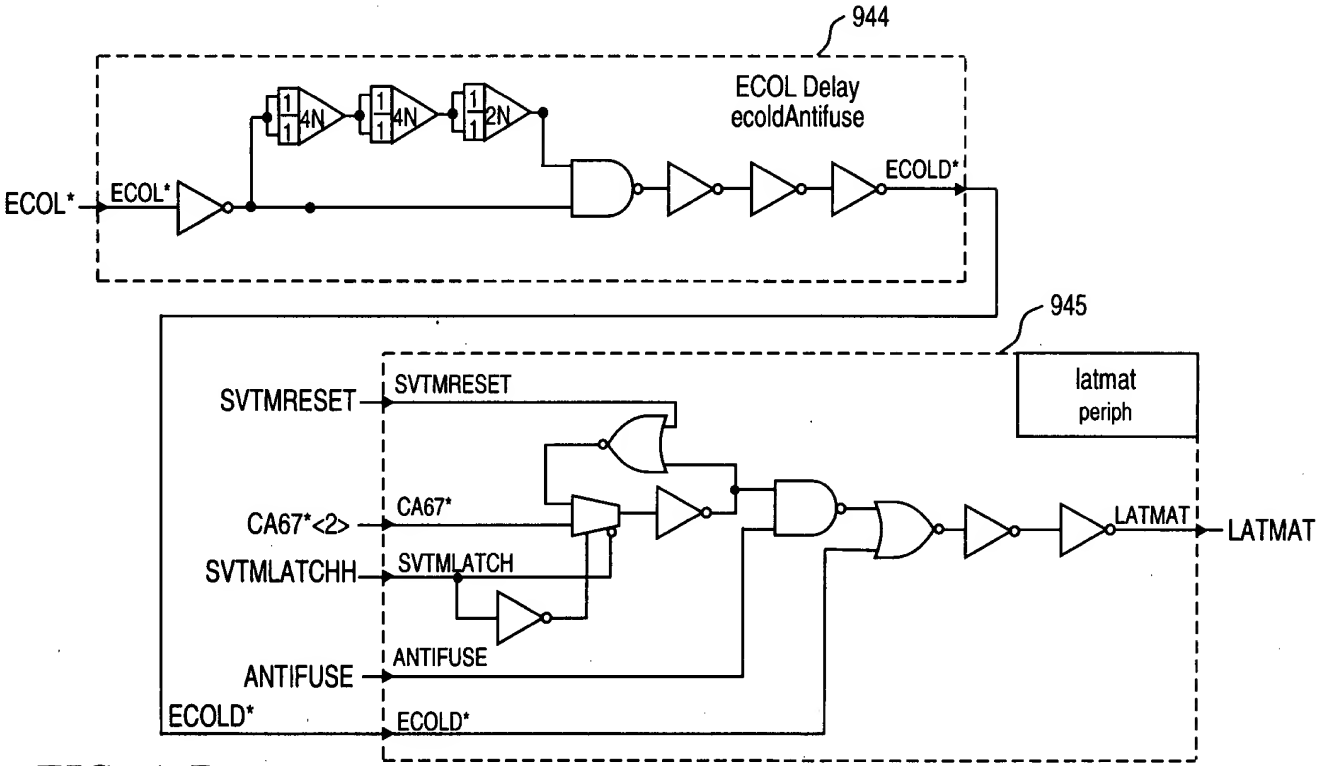

944
ECOL Delay
ecoldAntifuse
4N
4N
2N
ECOL*
ECOL*
ECOLD*
945
latmat
periph
SVTMRESET
SVTMRESET
CA67*<2>
CA67*
SVTMLATCHH
SVTMLATCH
LATMAT
LATMAT
ANTIFUSE
ANTIFUSE
ECOLD*
ECOLD*

FIG. 59D

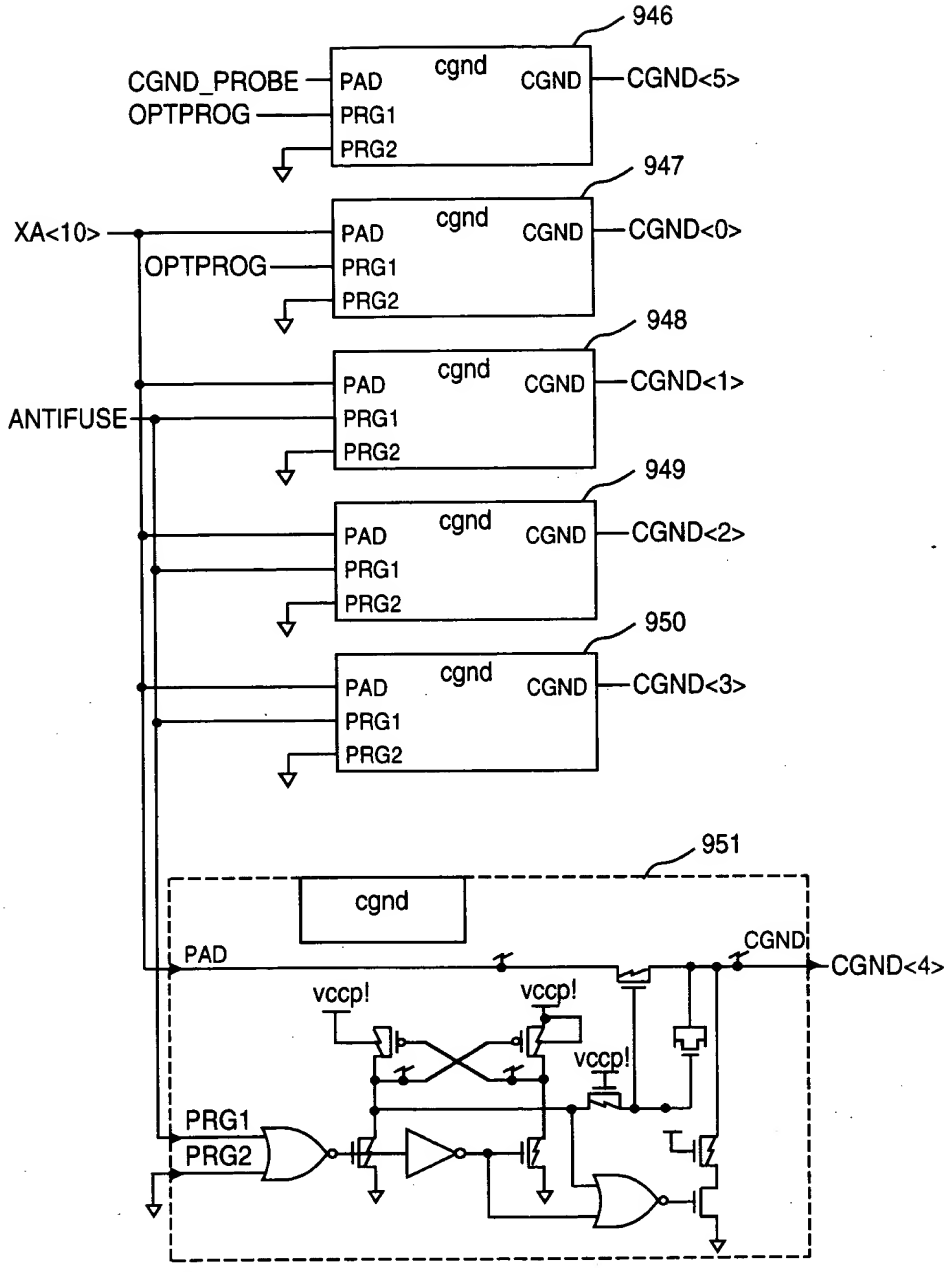

946
cgnd
CGND_PROBE
OPTPROG
PAD
PRG1
PRG2
CGND
CGND<5>
947
XA<10>
OPTPROG
CGND<0>
948
ANTIFUSE
CGND<1>
949
CGND<2>
950
CGND<3>
951
PAD
CGND
CGND<4>
vccp!
PRG1
PRG2

FIG. 59E

TOSCO 82570360

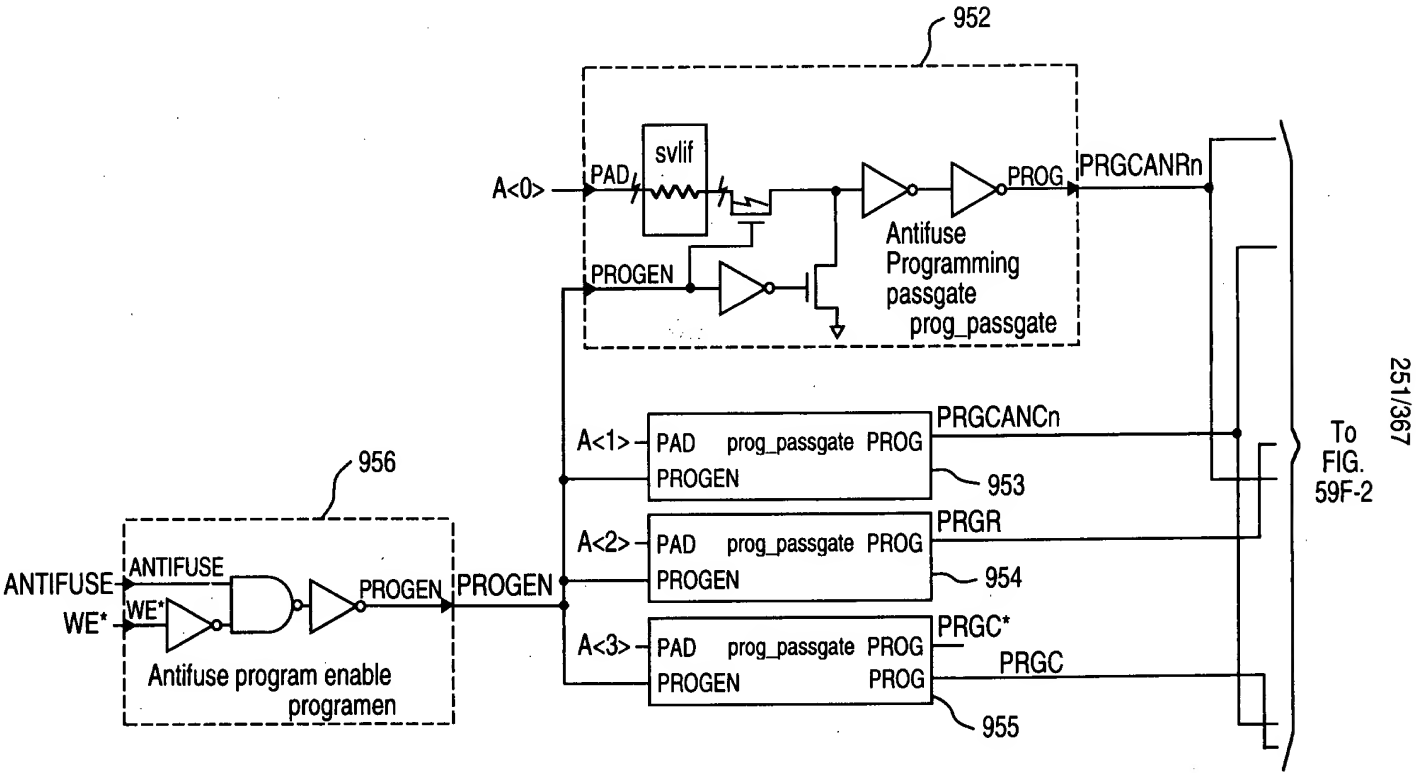


FIG. 59F-1

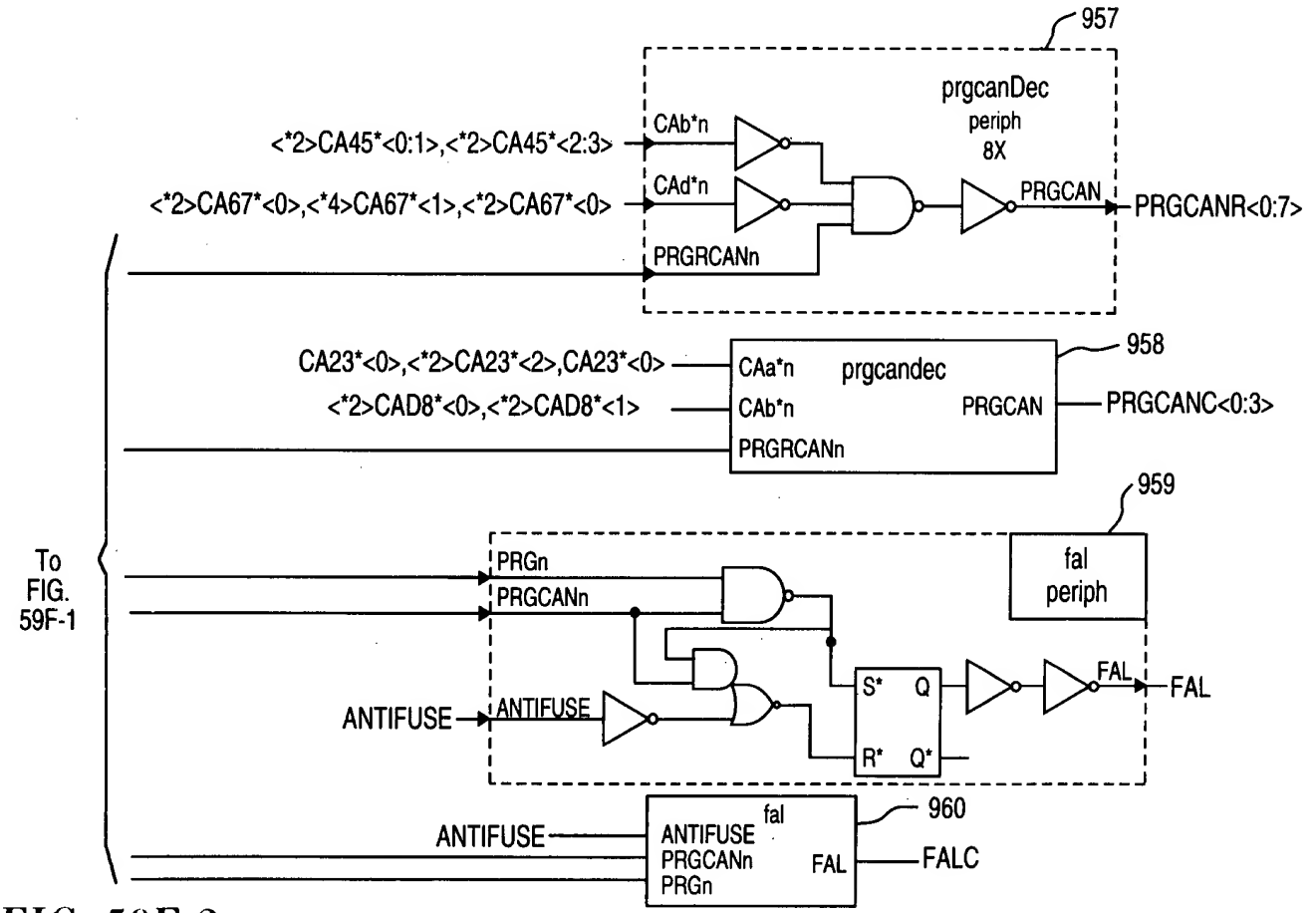

957
prgcanDec
periph
8X
CAb*n
CAd*n
PRGRCANn
PRGCAN
<*2>CA45*<0:1>,<*2>CA45*<2:3>
<*2>CA67*<0>,<*4>CA67*<1>,<*2>CA67*<0>
PRGCANR<0:7>
958
prgcandec
CAa*n
CAb*n
PRGRCANn
PRGCAN
CA23*<0>,<*2>CA23*<2>,CA23*<0>
<*2>CAD8*<0>,<*2>CAD8*<1>
PRGCANC<0:3>
959
fal
periph
PRGn
PRGCANn
ANTIFUSE
S*
Q
R*
Q*
FAL
To
FIG.
59F-1
960
fal
ANTIFUSE
PRGCANn
PRGn
FAL
FALC

FIG. 59F-2

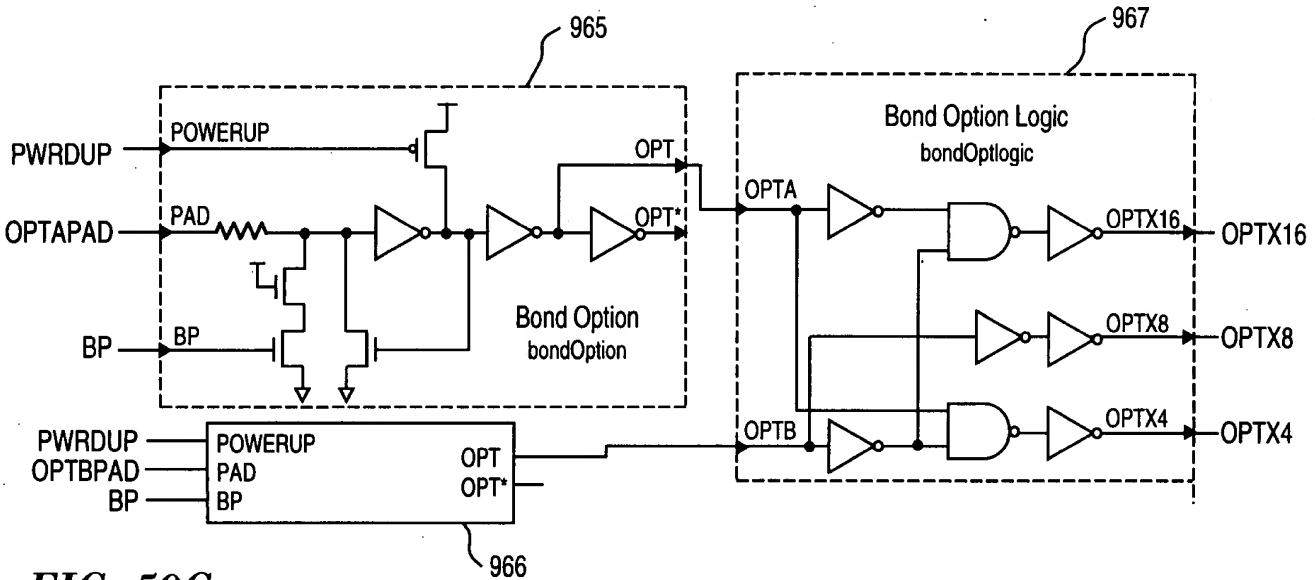

965
967
PWRDUP
POWERUP
OPT
OPTAPAD
PAD
OPT*
Bond Option
bondOption
BP
BP
Bond Option Logic
bondOptlogic
OPTA
OPTX16
OPTX16
OPTX8
OPTX8
OPTB
OPTX4
OPTX4
PWRDUP
OPTBPAD
BP
POWERUP
PAD
BP
OPT
OPT*
966

FIG. 59G

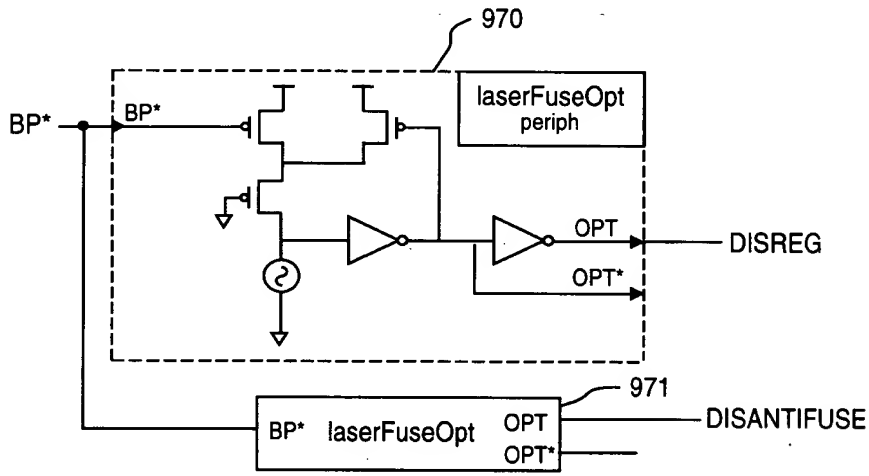

970
laserFuseOpt
periph
BP*
BP*
OPT
OPT*
DISREG
971
BP*
laserFuseOpt
OPT
OPT*
DISANTIFUSE

FIG. 59H

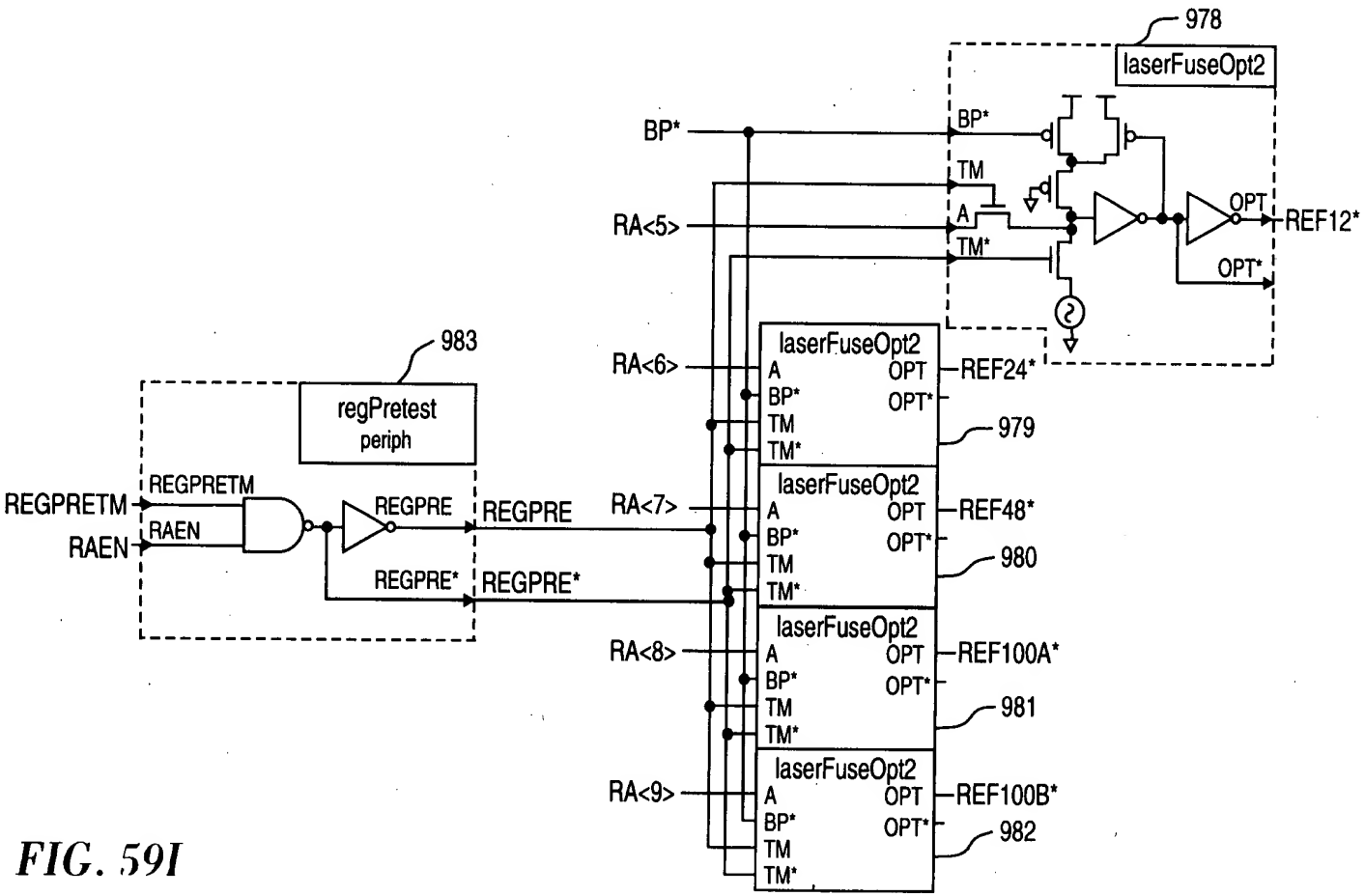

978
laserFuseOpt2
BP*
TM
A
TM*
OPT
OPT*
REF12*
983
regPretest
periph
REGPRETM
RAEN
REGPRE
REGPRE*
RA<5>
RA<6>
RA<7>
RA<8>
RA<9>
laserFuseOpt2
A
BP*
TM
TM*
OPT
OPT*
REF24*
979
REF48*
980
REF100A*
981
REF100B*
982

FIG. 59I

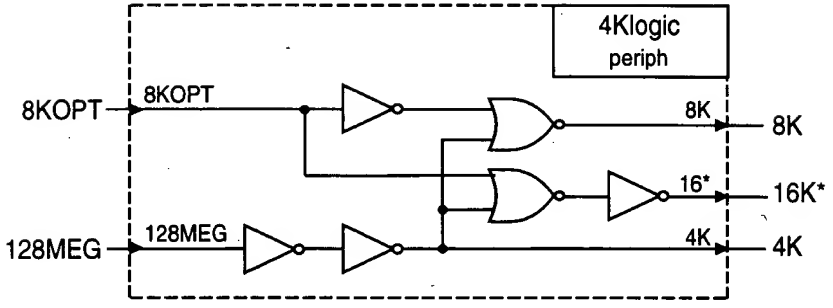


FIG. 59J

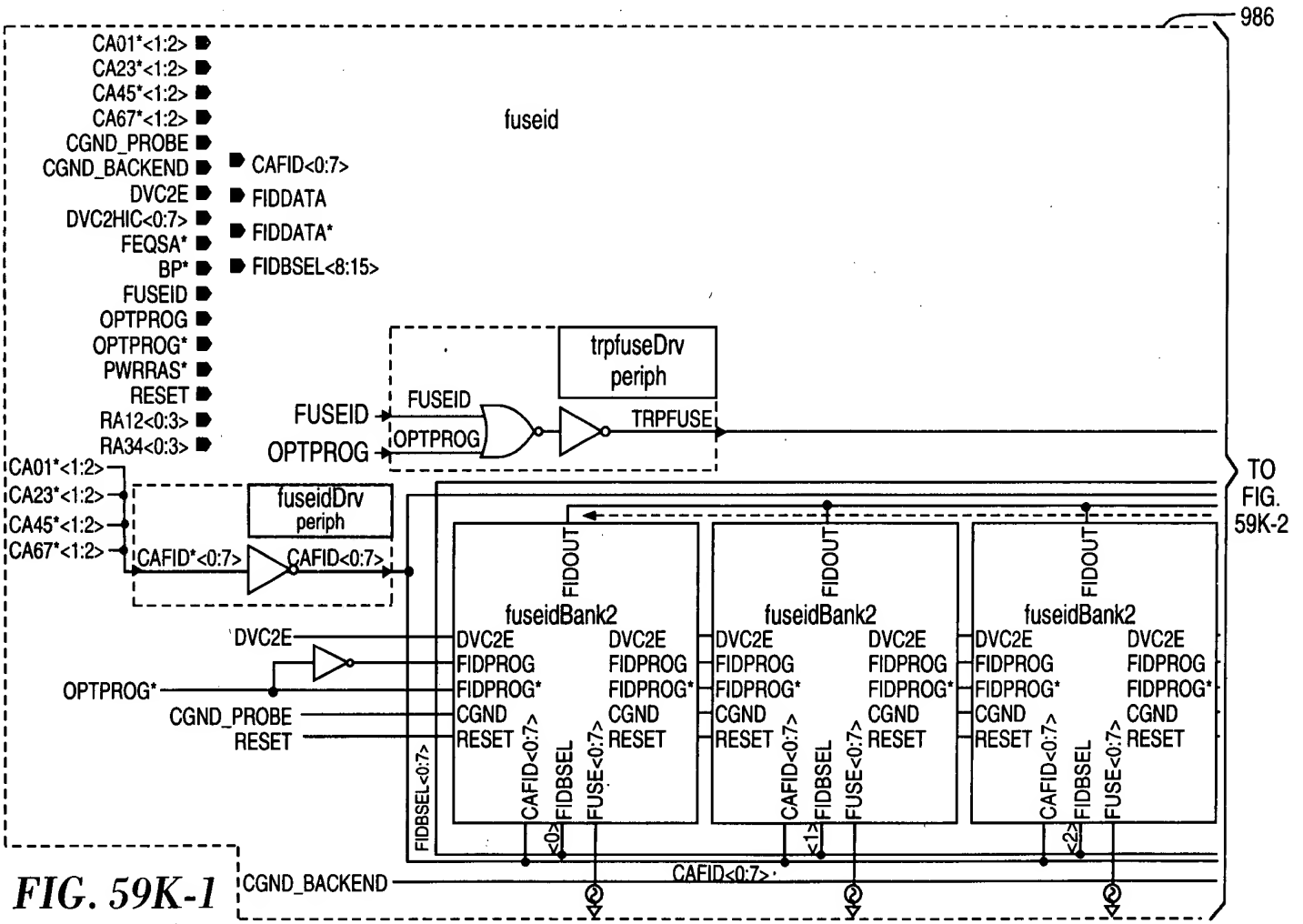

986
fuseid
CA01*<1:2>
CA23*<1:2>
CA45*<1:2>
CA67*<1:2>
CGND_PROBE
CGND_BACKEND
DVC2E
DVC2HIC<0:7>
FEQSA*
BP*
FUSEID
OPTPROG
OPTPROG*
PWRRAS*
RESET
RA12<0:3>
RA34<0:3>
CAFID<0:7>
FIDDATA
FIDDATA*
FIDBSEL<8:15>
trpfuseDrv
periph
FUSEID
OPTPROG
TRPFUSE
fuseidDrv
periph
CAFID*<0:7>
CAFID<0:7>
fuseidBank2
FIDOUT
DVC2E
FIDPROG
FIDPROG*
CGND
RESET
CAFID<0:7>
FIDBSEL
FUSE<0:7>
FIDBSEL<0:7>
<0>
<1>
<2>
TO
FIG.
59K-2

FIG. 59K-1

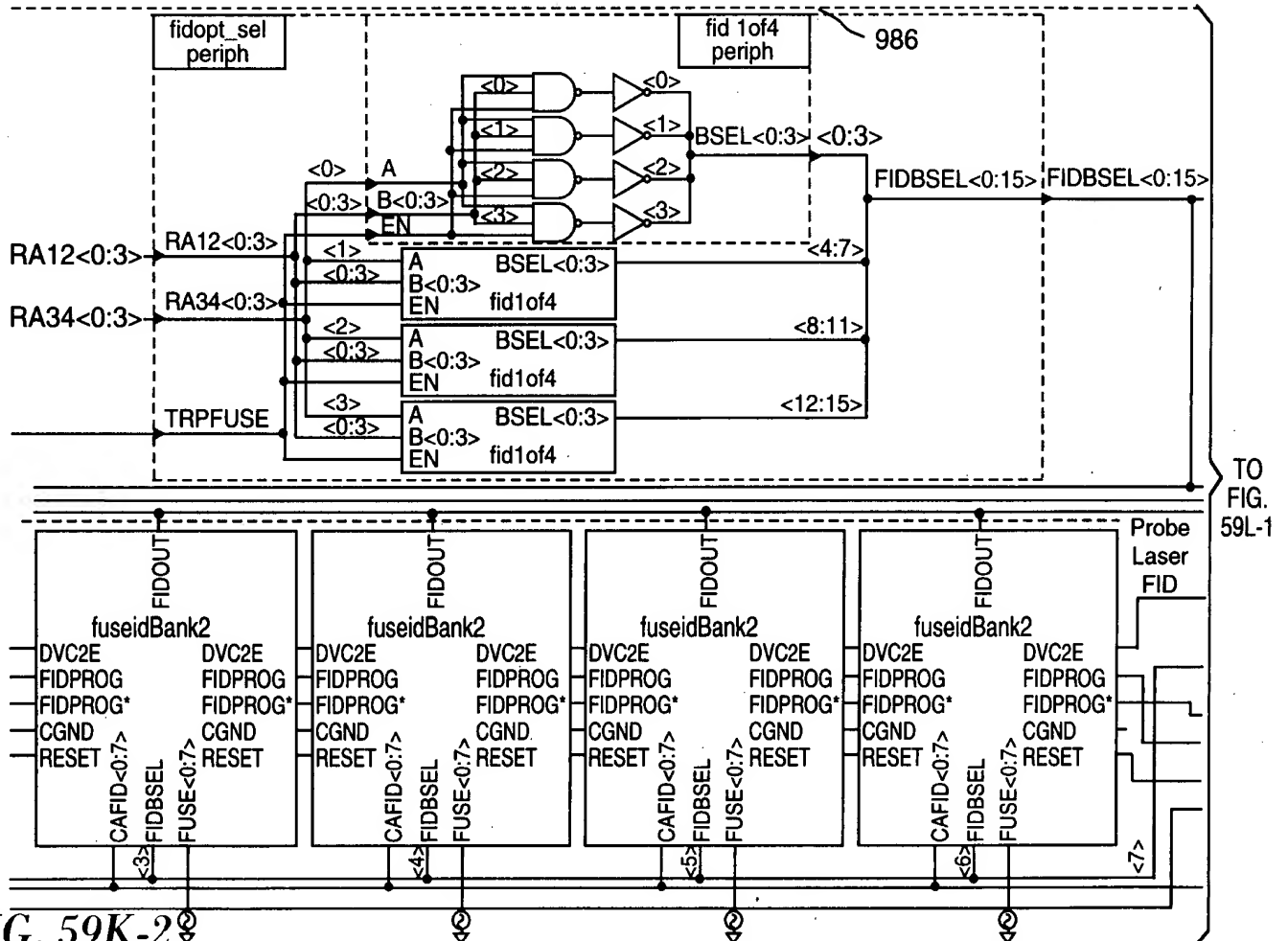

fidopt_sel periph
fid 1of4 periph
986
<0>
<1>
<2>
<3>
BSEL<0:3>
<0:3>
FIDBSEL<0:15>
FIDBSEL<0:15>
A
B<0:3>
EN
RA12<0:3>
RA34<0:3>
TRPFUSE
<4:7>
<8:11>
<12:15>
fid1of4
TO FIG. 59L-1
Probe Laser FID
FIDOUT
fuseidBank2
DVC2E
FIDPROG
FIDPROG*
CGND
RESET
CAFID<0:7>
FIDBSEL
FUSE<0:7>

FIG. 59K-2

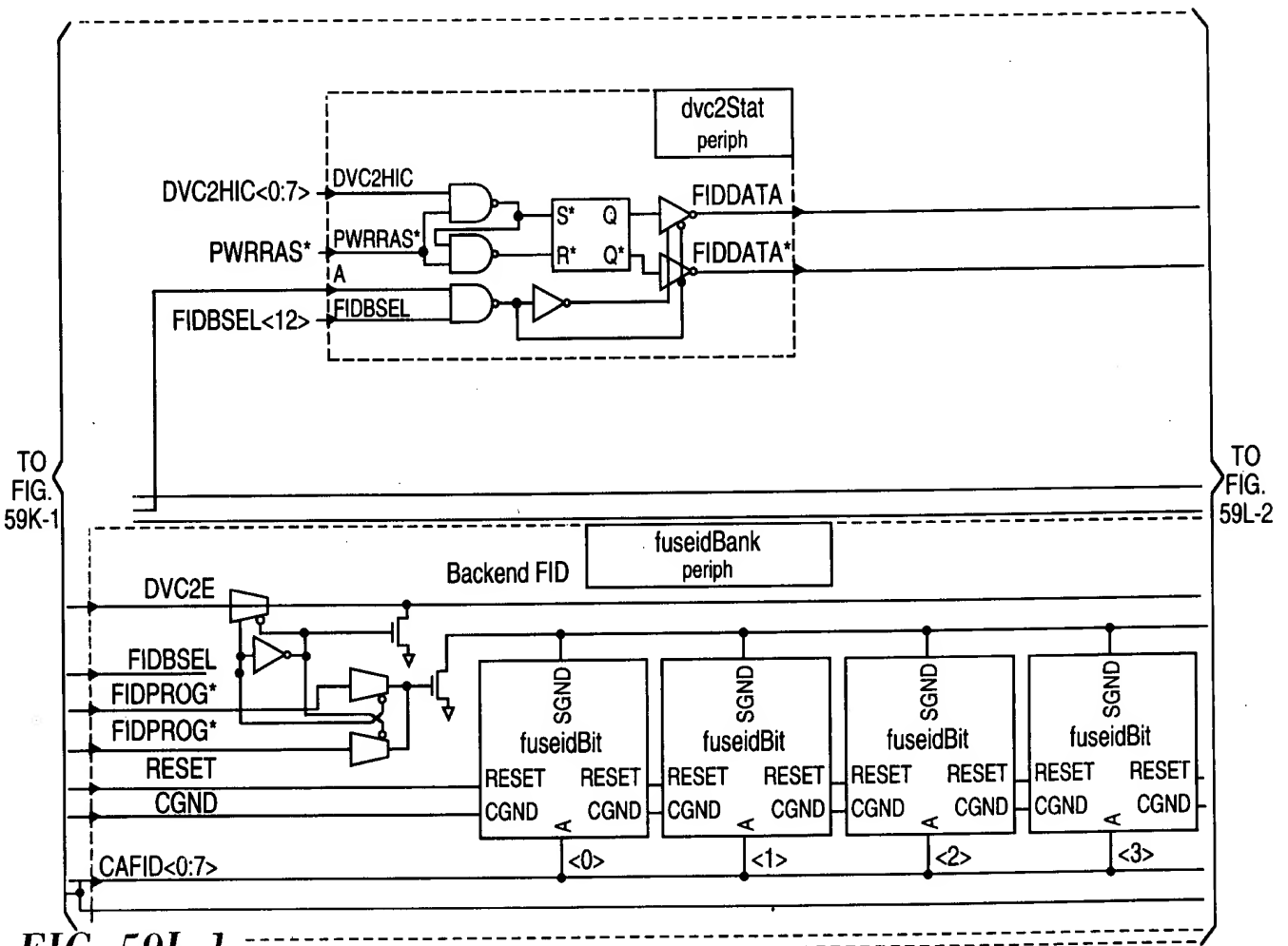
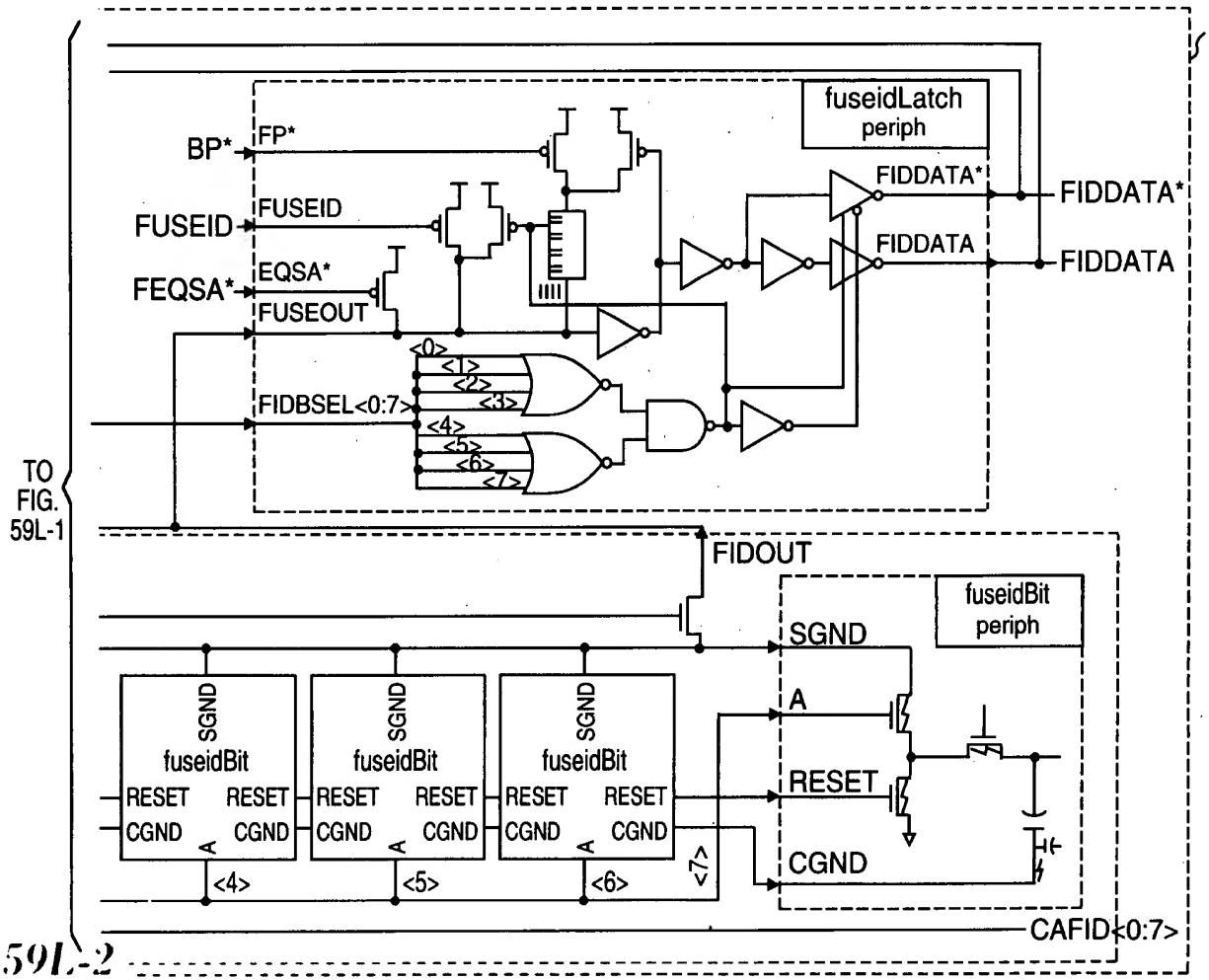

dvc2Stat
periph
DVC2HIC<0:7>
DVC2HIC
PWRRAS*
PWRRAS*
A
FIDBSEL<12>
FIDBSEL
S*
Q
R*
Q*
FIDDATA
FIDDATA*
TO
FIG.
59K-1
TO
FIG.
59L-2
fuseidBank
periph
Backend FID
DVC2E
FIDBSEL
FIDPROG*
FIDPROG*
RESET
CGND
CAFID<0:7>
SGND
fuseidBit
RESET
CGND
A
<0>
<1>
<2>
<3>

FIG. 59L-1



260/367

FIG. 59L-2

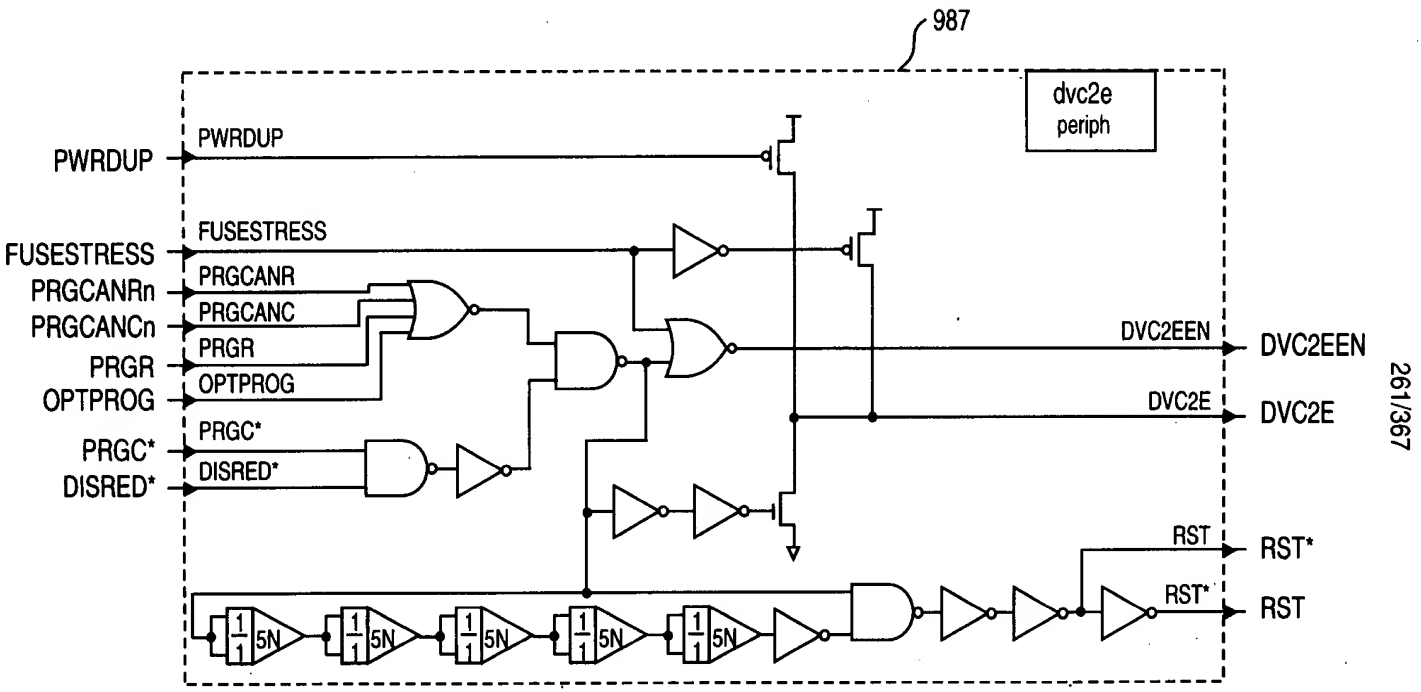

987
dvc2e
periph
PWRDUP
PWRDUP
FUSESTRESS
FUSESTRESS
PRGCANR
PRGCANRn
PRGCANC
PRGCANCn
PRGR
PRGR
OPTPROG
OPTPROG
PRGC*
PRGC*
DISRED*
DISRED*
DVC2EEN
DVC2EEN
DVC2E
DVC2E
RST
RST*
RST*
RST
1/1 5N
1/1 5N
1/1 5N
1/1 5N
1/1 5N

FIG. 59M

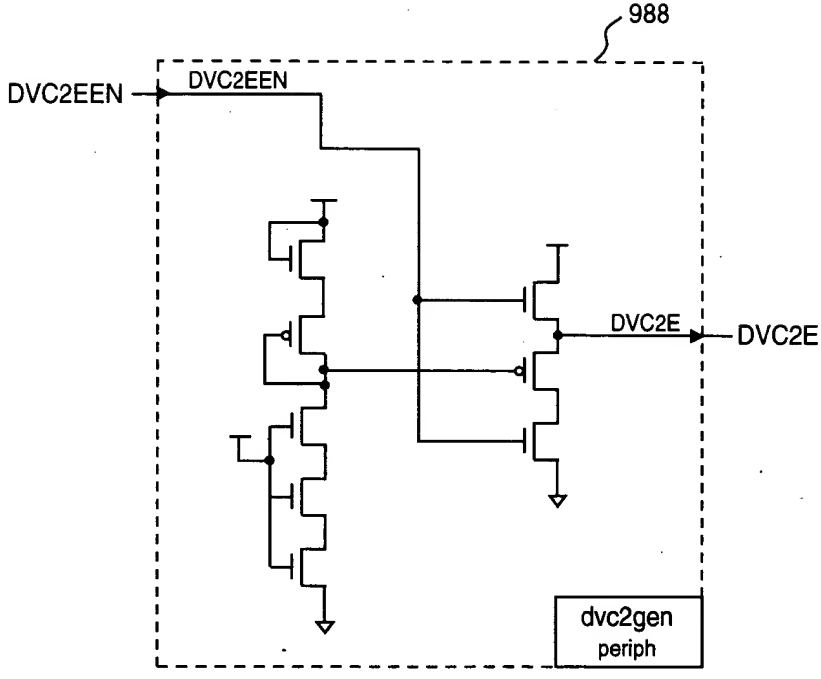


FIG. 59N

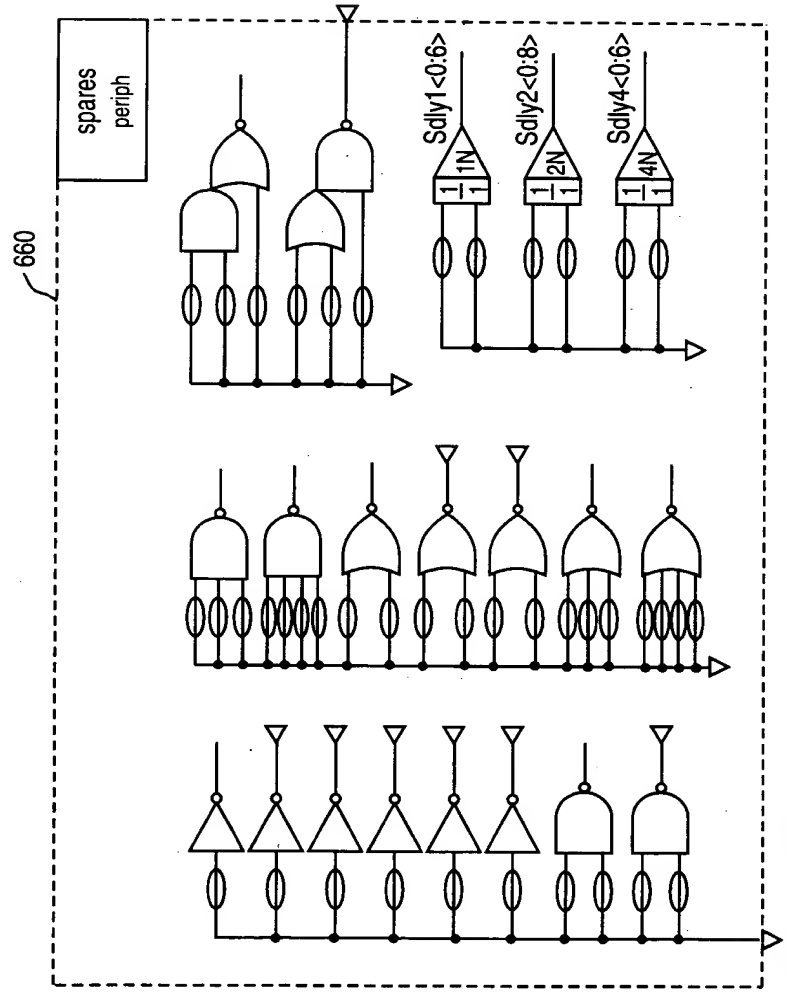


FIG. 590

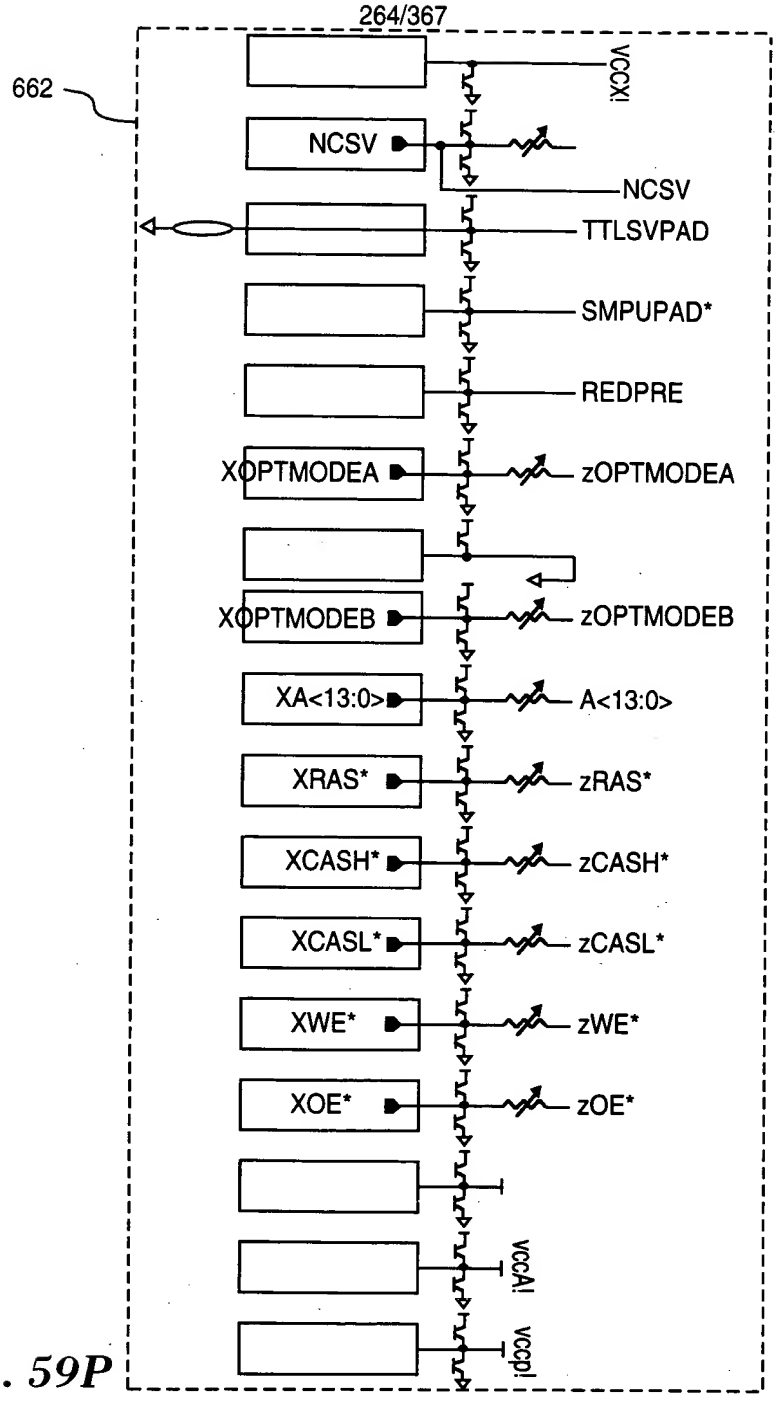

662
VCCX!
NCSV
NCSV
TTLSVPAD
SMPUPAD*
REDPRE
XOPTMODEA
zOPTMODEA
XOPTMODEB
zOPTMODEB
XA<13:0>
A<13:0>
XRAS*
zRAS*
XCASH*
zCASH*
XCASL*
zCASL*
XWE*
zWE*
XOE*
zOE*
VCCA!
VCCP!

FIG. 59P

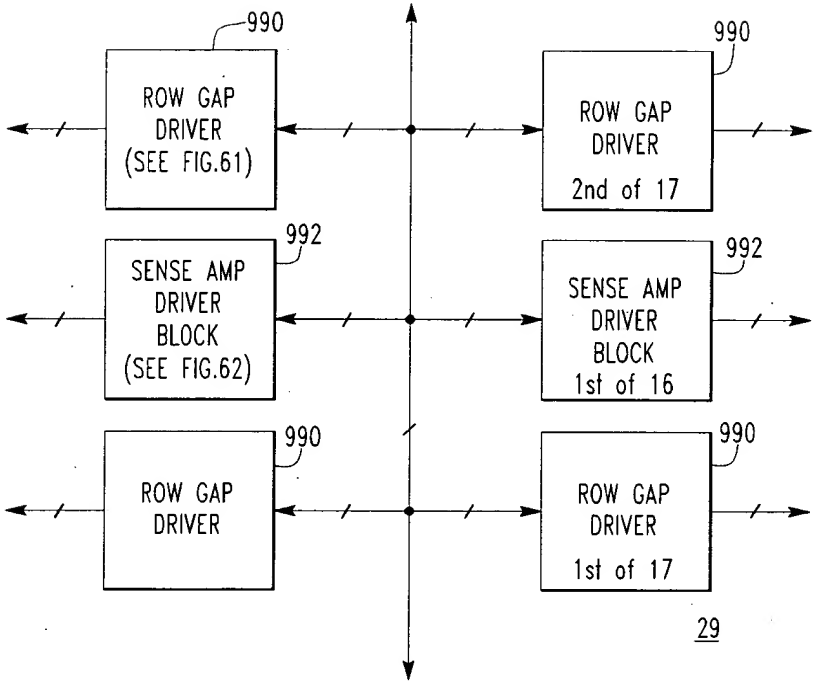

990
ROW GAP DRIVER (SEE FIG.61)
990
ROW GAP DRIVER 2nd of 17
992
SENSE AMP DRIVER BLOCK (SEE FIG.62)
992
SENSE AMP DRIVER BLOCK 1st of 16
990
ROW GAP DRIVER
990
ROW GAP DRIVER 1st of 17
29

FIG. 60

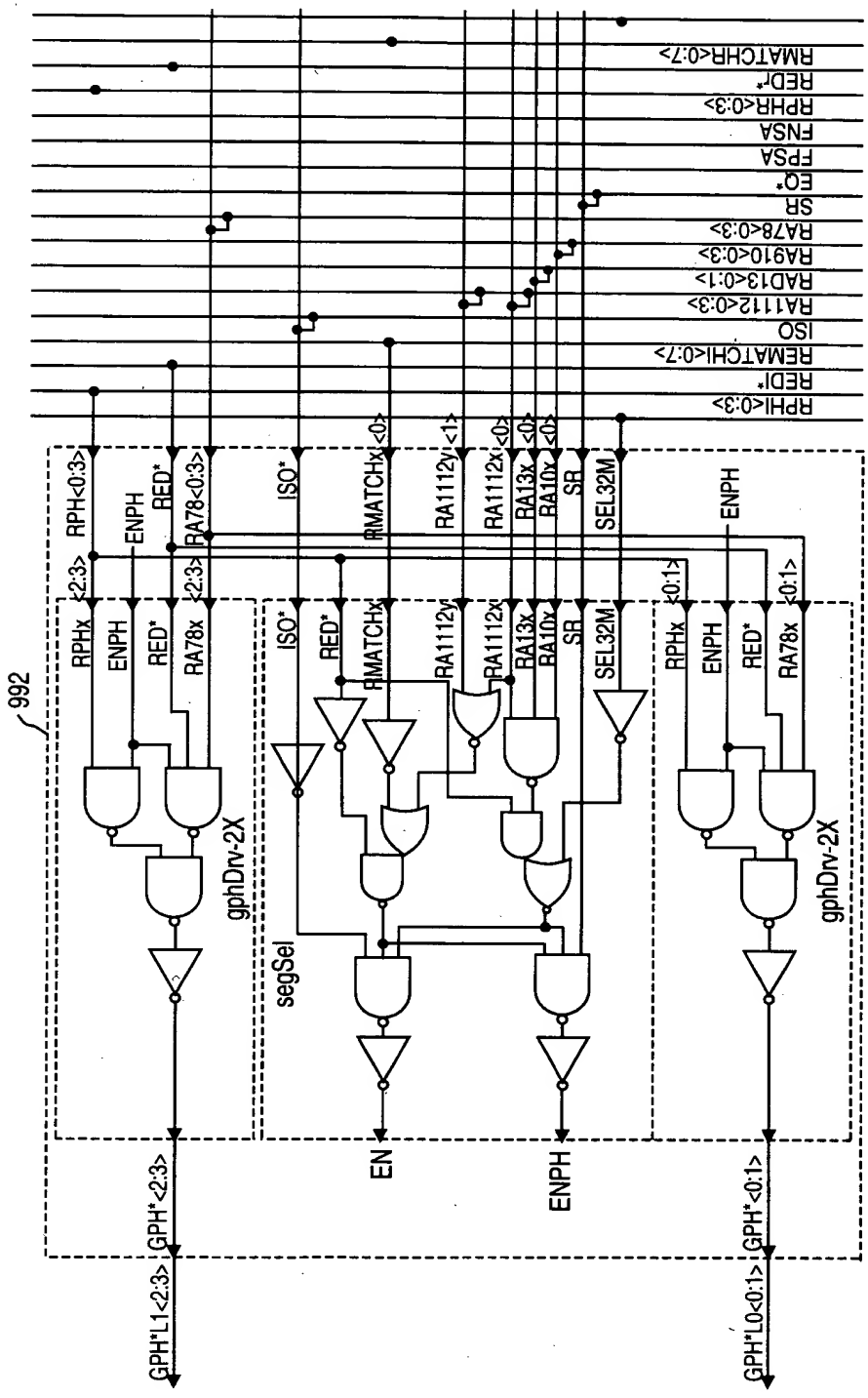

992
RPHI<0:3>
REDI*
REMATCHI<0:7>
ISO
RA1112<0:3>
RAD13<0:1>
RA910<0:3>
RA78<0:3>
SR
EO*
FPSA
FNSA
RPHR<0:3>
REDR*
RMATCHR<0:7>
RPH<0:3>
ENPH
RED*
RA78<0:3>
ISO*
RMATCHx<0>
RA1112y<1>
RA1112x<0>
RA13x<0>
RA10x<0>
SR
SEL32M
ENPH
RPHx<2:3>
ENPH
RED*
RA78x<2:3>
ISO*
RED*
RMATCHx
RA1112y
RA1112x
RA13x
RA10x
SR
SEL32M
RPHx<0:1>
ENPH
RED*
RA78x<0:1>
gphDrv-2X
segSel
gphDrv-2X
EN
ENPH
GPH*L1<2:3>
GPH*<2:3>
GPH*L0<0:1>
GPH*<0:1>

FIG. 61

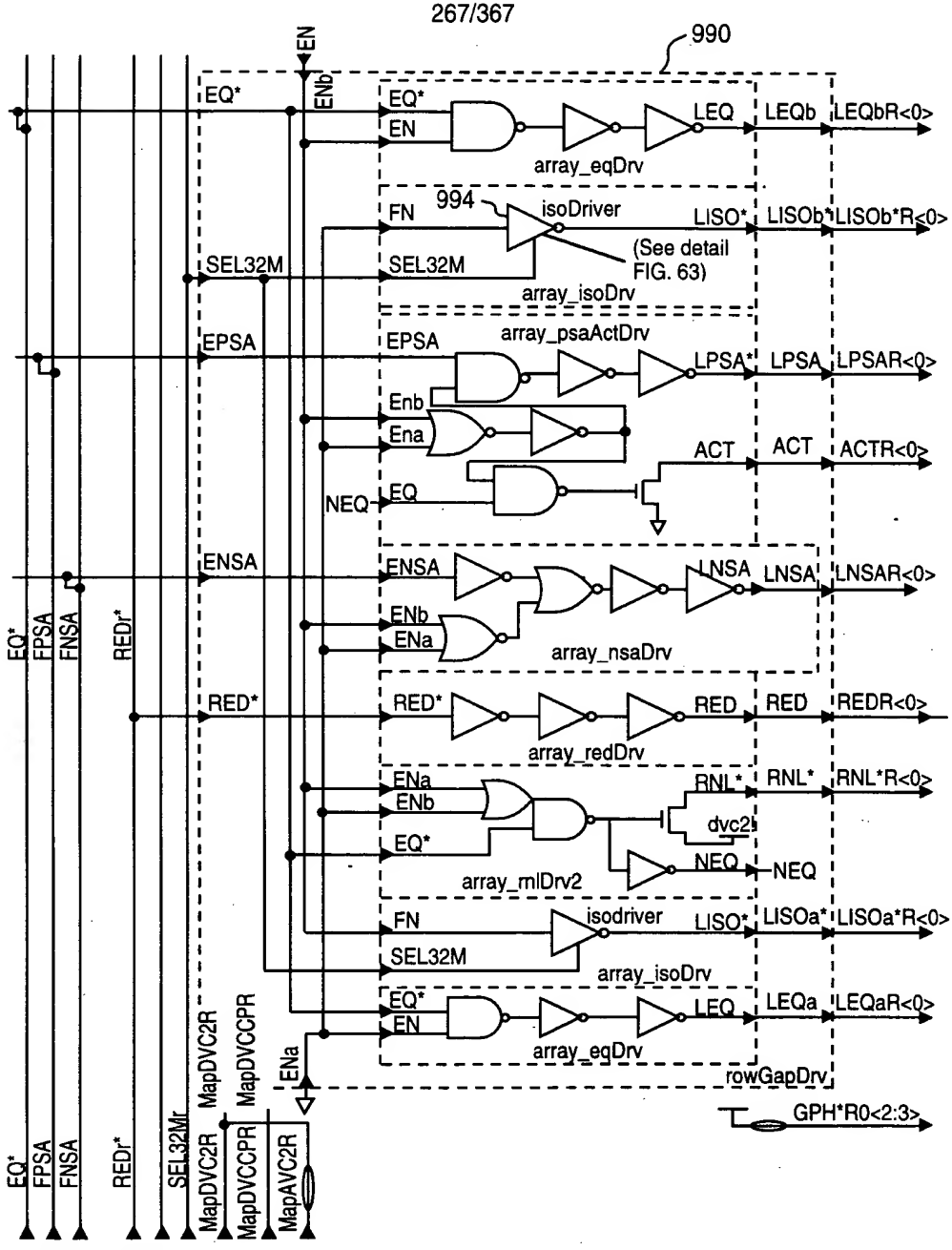

990
EN
ENb
EQ*
EN
LEQ
LEQb
LEQbR<0>
array_eqDrv
994
FN
isoDriver
LISO*
LISOb*
LISOb*R<0>
(See detail FIG. 63)
SEL32M
array_isoDrv
EPSA
array_psaActDrv
LPSA*
LPSA
LPSAR<0>
Enb
Ena
ACT
ACTR<0>
NEQ
EQ
ENSA
LNSA
LNSAR<0>
array_nsaDrv
RED*
RED
REDR<0>
array_redDrv
RNL*
RNL*R<0>
dvc2
array_rnlDrv2
LISOa*
LISOa*R<0>
LEQa
LEQaR<0>
rowGapDrv
GPH*R0<2:3>
FPSA
FNSA
REDr*
SEL32Mr
MapDVC2R
MapDVCCPR
MapAVC2R
ENa

FIG. 62

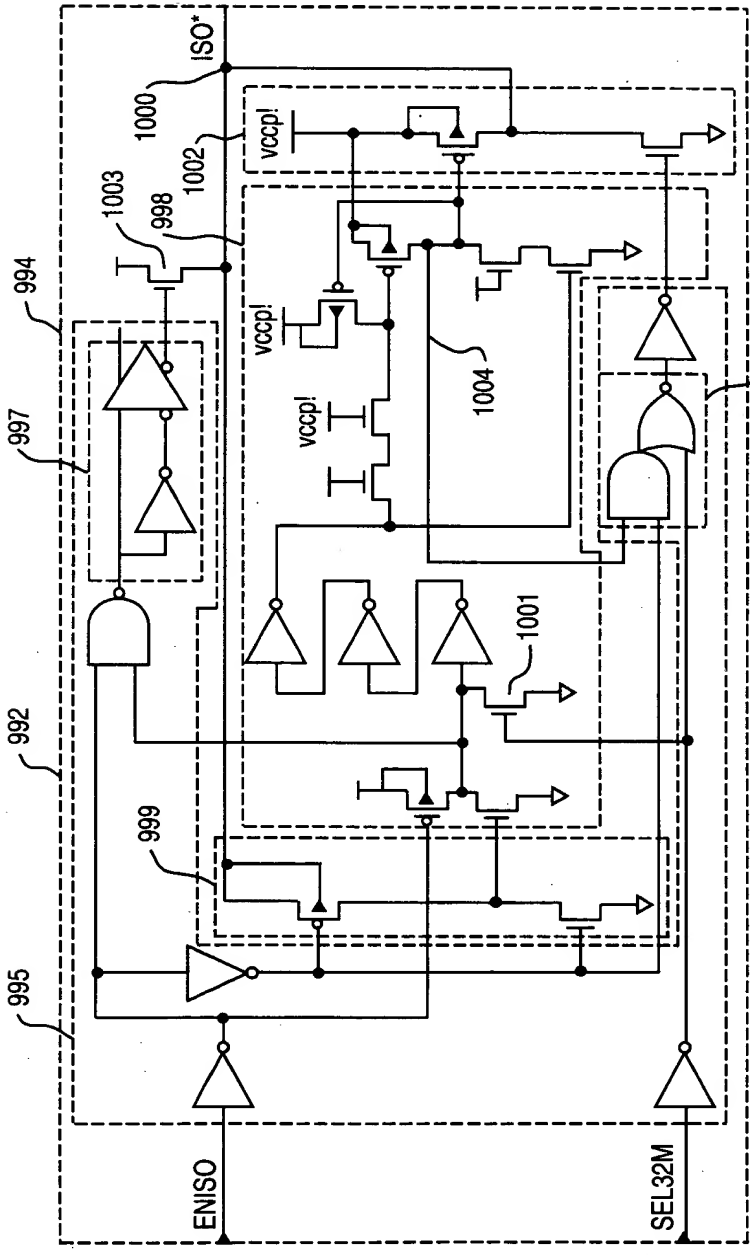

ISO*
1000
1002
1003
998
994
997
992
999
995
996
1004
1001
vccp!
vccp!
vccp!
ENISO
SEL32M

FIG. 63

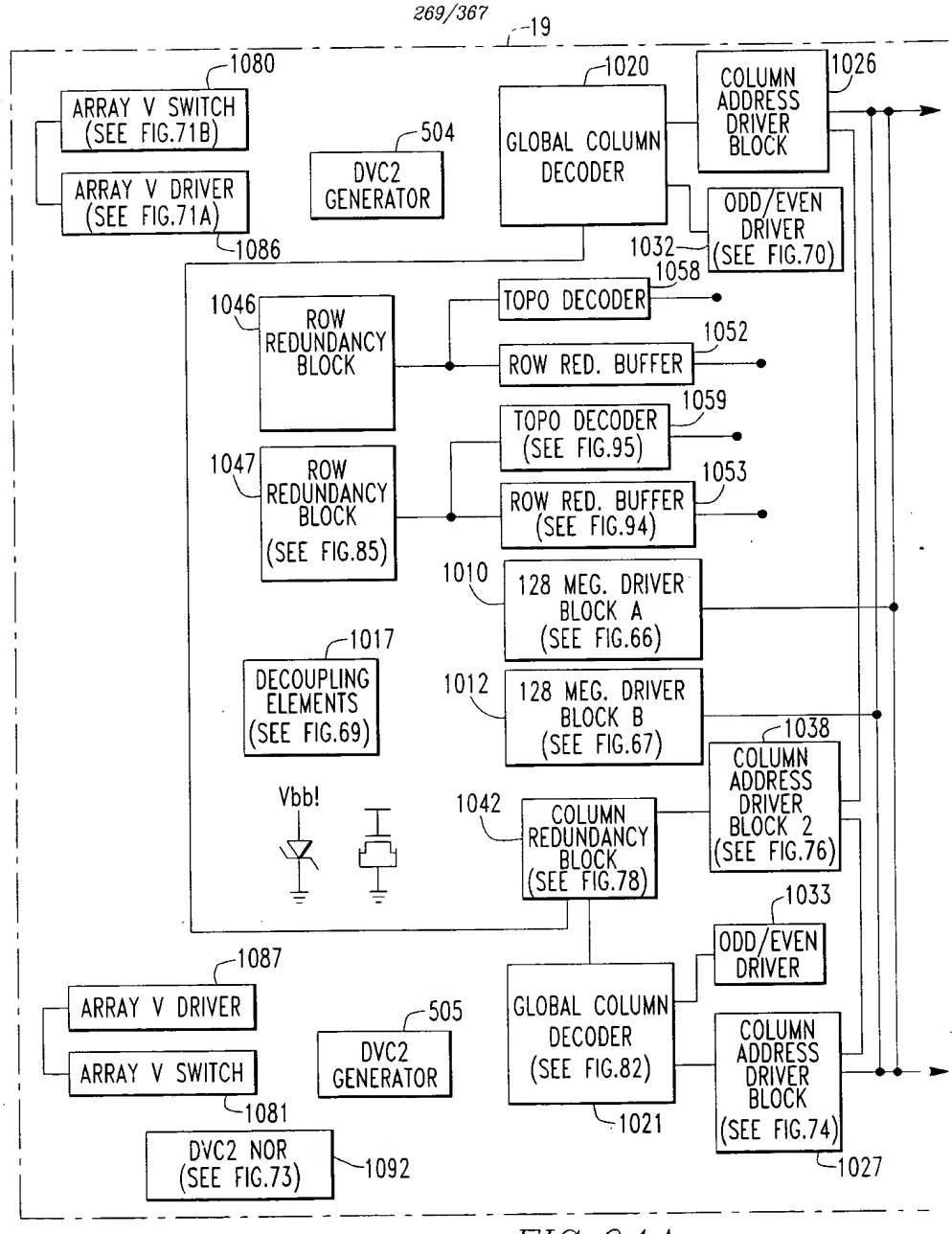

19
1080
ARRAY V SWITCH (SEE FIG.71B)
ARRAY V DRIVER (SEE FIG.71A)
1086
504
DVC2 GENERATOR
1020
GLOBAL COLUMN DECODER
1026
COLUMN ADDRESS DRIVER BLOCK
1032
ODD/EVEN DRIVER (SEE FIG.70)
1058
TOPO DECODER
1046
ROW REDUNDANCY BLOCK
1052
ROW RED. BUFFER
1059
TOPO DECODER (SEE FIG.95)
1047
ROW REDUNDANCY BLOCK (SEE FIG.85)
1053
ROW RED. BUFFER (SEE FIG.94)
1010
128 MEG. DRIVER BLOCK A (SEE FIG.66)
1017
DECOUPLING ELEMENTS (SEE FIG.69)
1012
128 MEG. DRIVER BLOCK B (SEE FIG.67)
1038
COLUMN ADDRESS DRIVER BLOCK 2 (SEE FIG.76)
Vbb!
1042
COLUMN REDUNDANCY BLOCK (SEE FIG.78)
1033
ODD/EVEN DRIVER
1087
ARRAY V DRIVER
ARRAY V SWITCH
1081
505
DVC2 GENERATOR
GLOBAL COLUMN DECODER (SEE FIG.82)
1021
COLUMN ADDRESS DRIVER BLOCK (SEE FIG.74)
1027
DVC2 NOR (SEE FIG.73)
1092

FIG. 64A

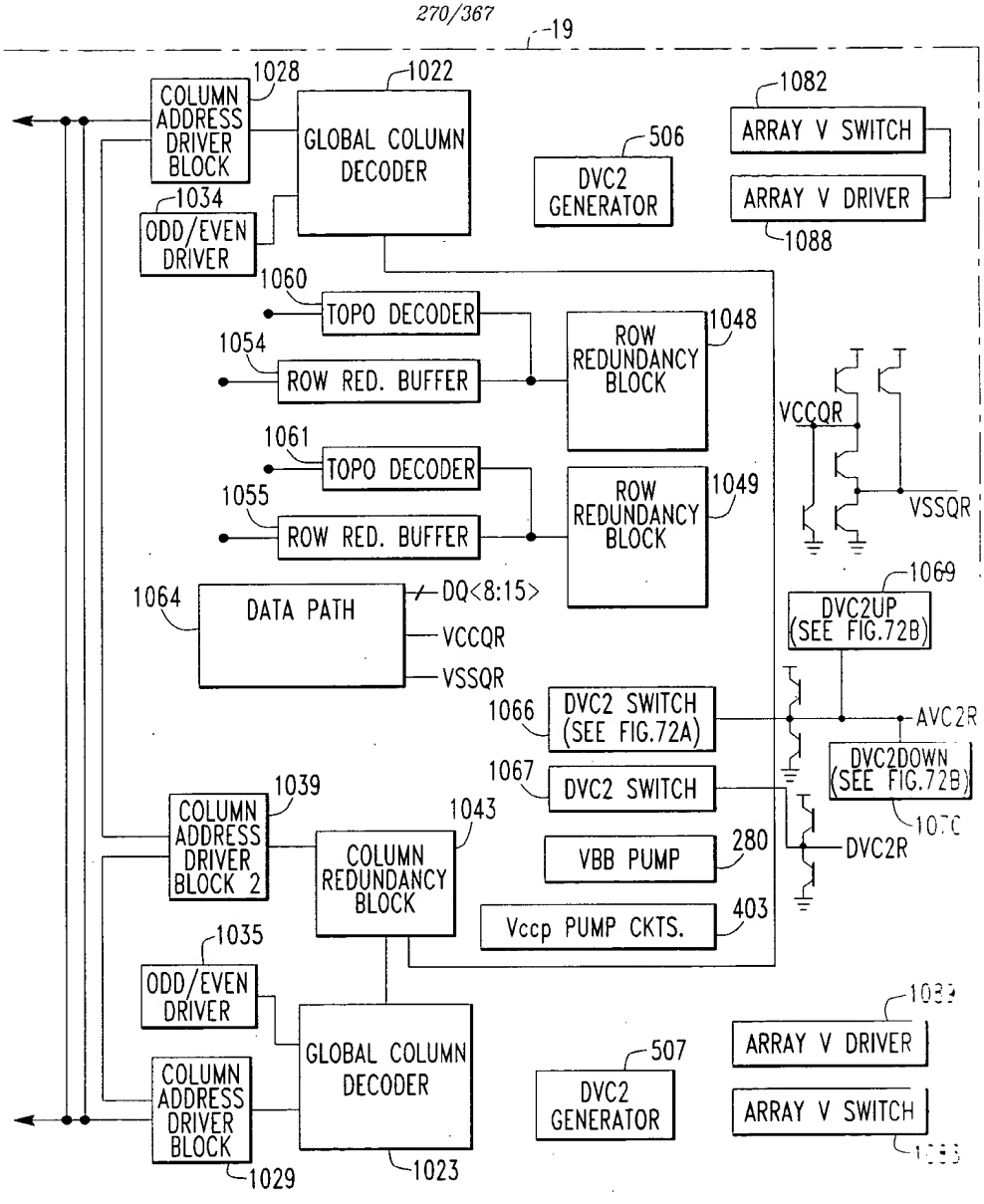

19
COLUMN ADDRESS DRIVER BLOCK
1028
GLOBAL COLUMN DECODER
1022
DVC2 GENERATOR
506
ARRAY V SWITCH
1082
ARRAY V DRIVER
1088
ODD/EVEN DRIVER
1034
TOPO DECODER
1060
ROW RED. BUFFER
1054
ROW REDUNDANCY BLOCK
1048
TOPO DECODER
1061
ROW RED. BUFFER
1055
ROW REDUNDANCY BLOCK
1049
VCCQR
VSSQR
DATA PATH
1064
DQ<8:15>
VCCQR
VSSQR
DVC2UP (SEE FIG.72B)
1069
DVC2 SWITCH (SEE FIG.72A)
1066
AVC2R
DVC2DOWN (SEE FIG.72B)
DVC2 SWITCH
1067
DVC2R
VBB PUMP
280
Vccp PUMP CKTS.
403
COLUMN ADDRESS DRIVER BLOCK 2
1039
COLUMN REDUNDANCY BLOCK
1043
ODD/EVEN DRIVER
1035
GLOBAL COLUMN DECODER
COLUMN ADDRESS DRIVER BLOCK
1029
1023
DVC2 GENERATOR
507
ARRAY V DRIVER
ARRAY V SWITCH

FIG. 64B

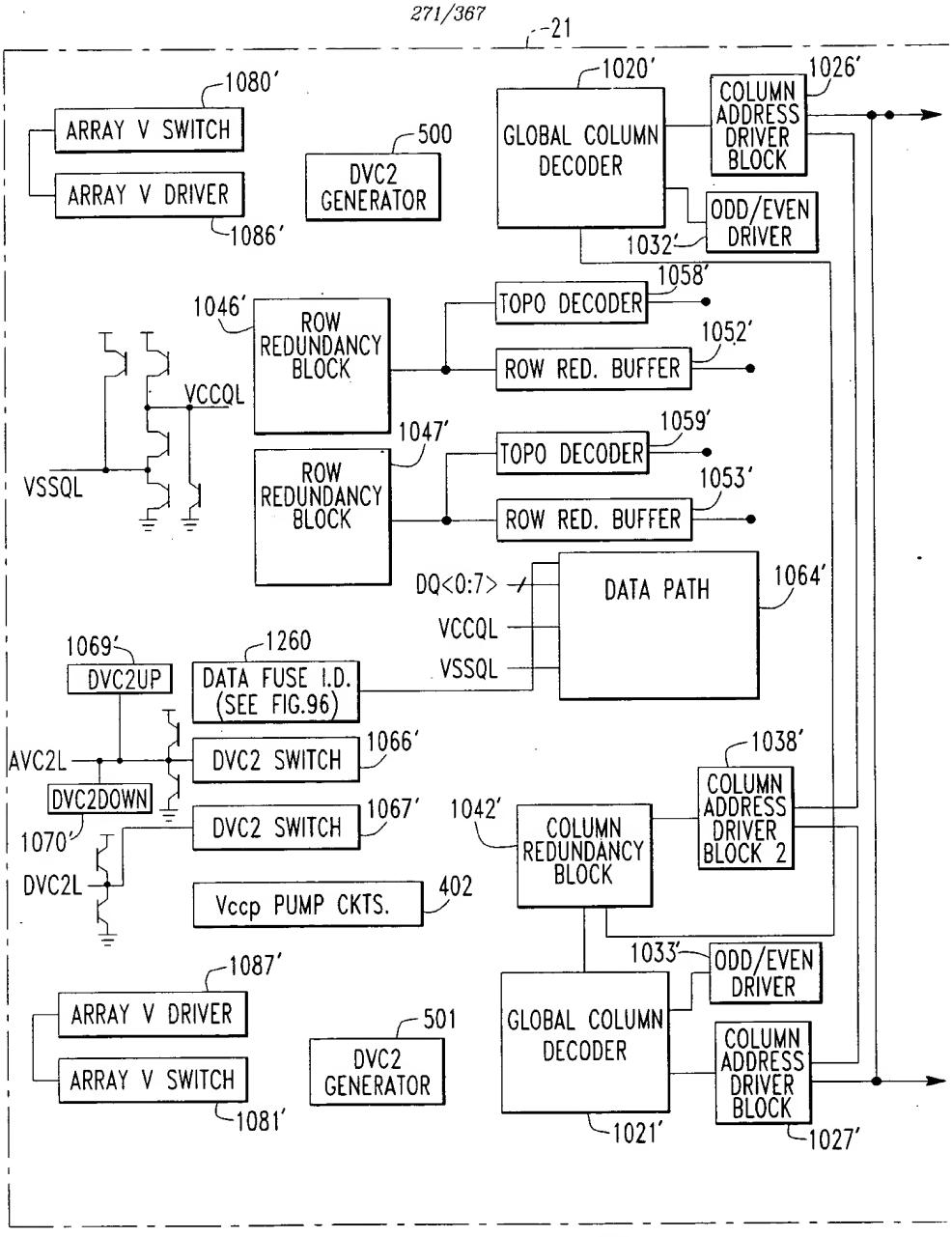

21
1080'
ARRAY V SWITCH
ARRAY V DRIVER
1086'
500
DVC2 GENERATOR
1020'
GLOBAL COLUMN DECODER
1026'
COLUMN ADDRESS DRIVER BLOCK
ODD/EVEN DRIVER
1032'
1046'
ROW REDUNDANCY BLOCK
TOPO DECODER
1058'
ROW RED. BUFFER
1052'
VCCQL
VSSQL
1047'
ROW REDUNDANCY BLOCK
TOPO DECODER
1059'
ROW RED. BUFFER
1053'
DQ<0:7>
VCCQL
VSSQL
DATA PATH
1064'
1069'
DVC2UP
1260
DATA FUSE I.D. (SEE FIG.96)
AVC2L
DVC2 SWITCH
1066'
DVC2DOWN
1070'
DVC2 SWITCH
1067'
DVC2L
Vccp PUMP CKTS.
402
1038'
COLUMN ADDRESS DRIVER BLOCK 2
1042'
COLUMN REDUNDANCY BLOCK
1033'
ODD/EVEN DRIVER
1087'
ARRAY V DRIVER
ARRAY V SWITCH
1081'
501
DVC2 GENERATOR
GLOBAL COLUMN DECODER
1021'
COLUMN ADDRESS DRIVER BLOCK
1027'

FIG. 65A

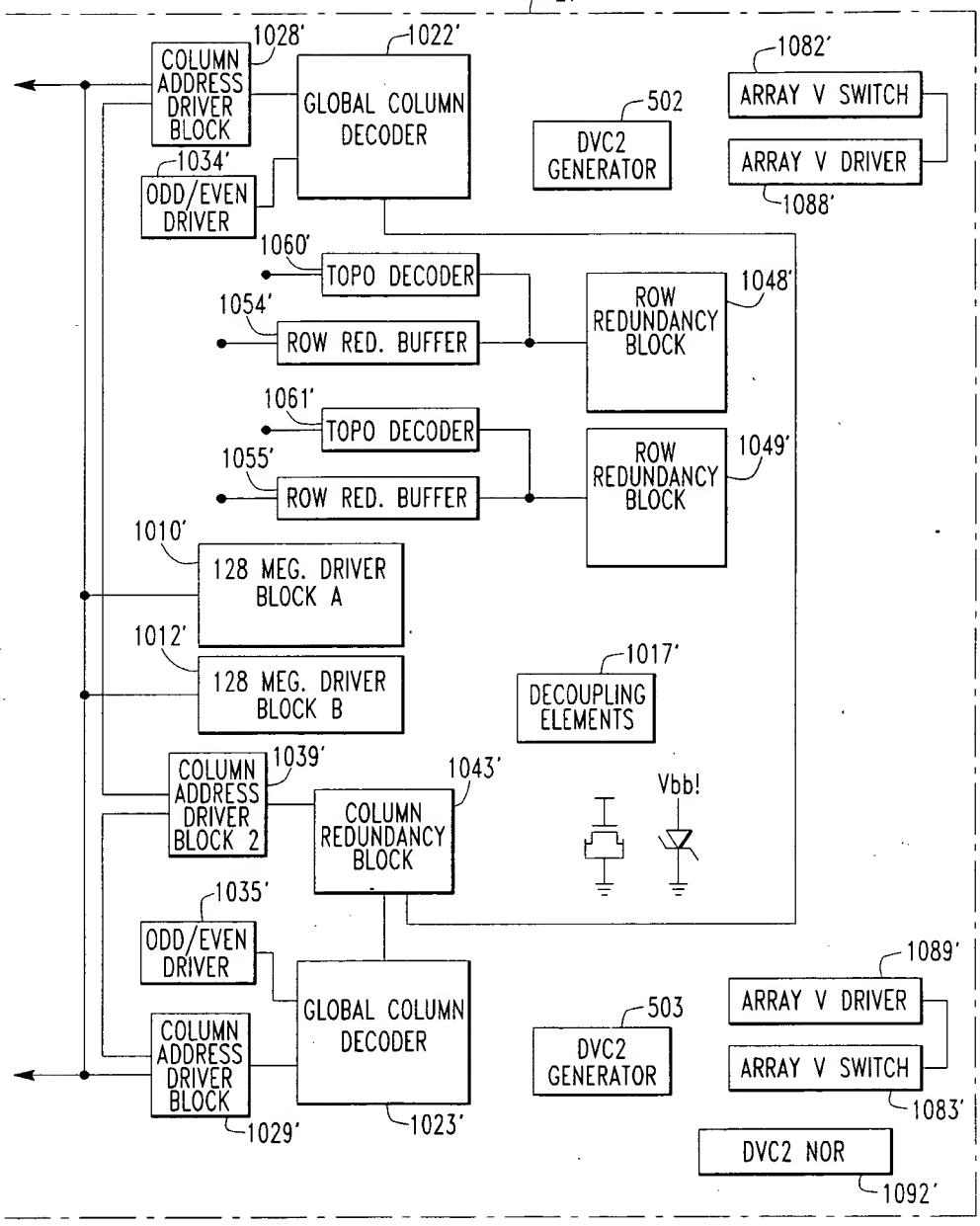

21
COLUMN ADDRESS DRIVER BLOCK
1028'
GLOBAL COLUMN DECODER
1022'
DVC2 GENERATOR
502
ARRAY V SWITCH
1082'
ARRAY V DRIVER
1088'
ODD/EVEN DRIVER
1034'
TOPO DECODER
1060'
ROW RED. BUFFER
1054'
ROW REDUNDANCY BLOCK
1048'
TOPO DECODER
1061'
ROW RED. BUFFER
1055'
ROW REDUNDANCY BLOCK
1049'
128 MEG. DRIVER BLOCK A
1010'
128 MEG. DRIVER BLOCK B
1012'
DECOUPLING ELEMENTS
1017'
COLUMN ADDRESS DRIVER BLOCK 2
1039'
COLUMN REDUNDANCY BLOCK
1043'
Vbb!
ODD/EVEN DRIVER
1035'
GLOBAL COLUMN DECODER
COLUMN ADDRESS DRIVER BLOCK
1029'
1023'
DVC2 GENERATOR
503
ARRAY V DRIVER
1089'
ARRAY V SWITCH
1083'
DVC2 NOR
1092'

FIG. 65B

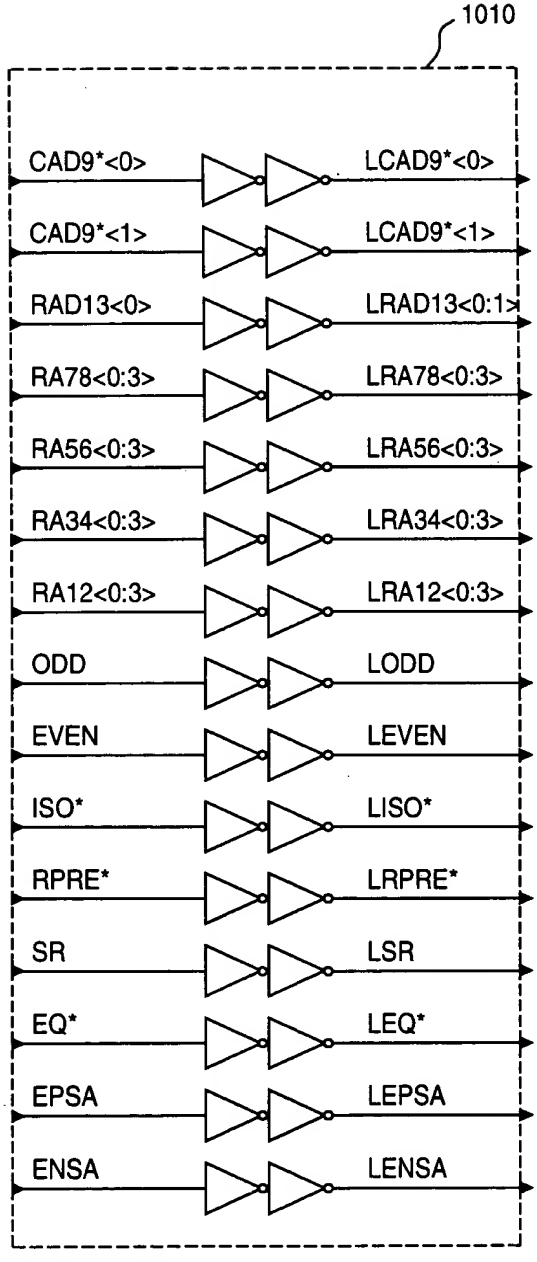

1010
CAD9*<0>
LCAD9*<0>
CAD9*<1>
LCAD9*<1>
RAD13<0>
LRAD13<0:1>
RA78<0:3>
LRA78<0:3>
RA56<0:3>
LRA56<0:3>
RA34<0:3>
LRA34<0:3>
RA12<0:3>
LRA12<0:3>
ODD
LODD
EVEN
LEVEN
ISO*
LISO*
RPRE*
LRPRE*
SR
LSR
EQ*
LEQ*
EPSA
LEPSA
ENSA
LENSA

FIG. 66

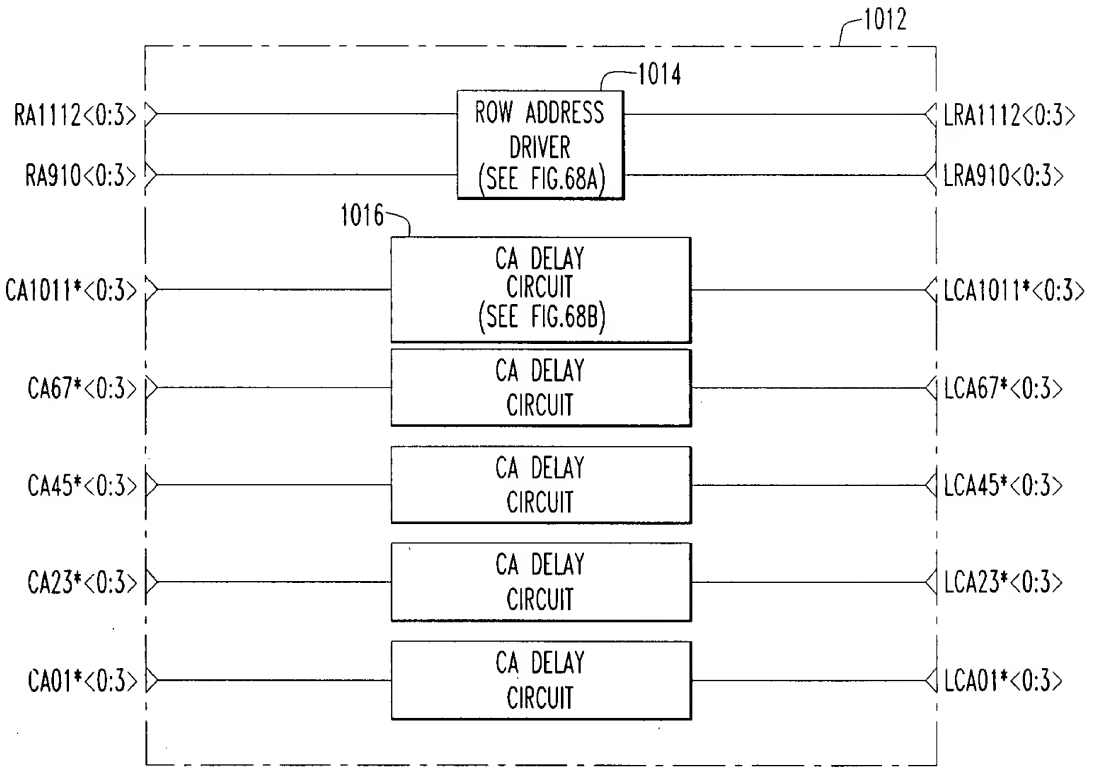

1012
1014
ROW ADDRESS DRIVER (SEE FIG.68A)
RA1112<0:3>
RA910<0:3>
LRA1112<0:3>
LRA910<0:3>
1016
CA DELAY CIRCUIT (SEE FIG.68B)
CA1011*<0:3>
LCA1011*<0:3>
CA DELAY CIRCUIT
CA67*<0:3>
LCA67*<0:3>
CA DELAY CIRCUIT
CA45*<0:3>
LCA45*<0:3>
CA DELAY CIRCUIT
CA23*<0:3>
LCA23*<0:3>
CA DELAY CIRCUIT
CA01*<0:3>
LCA01*<0:3>

FIG. 67

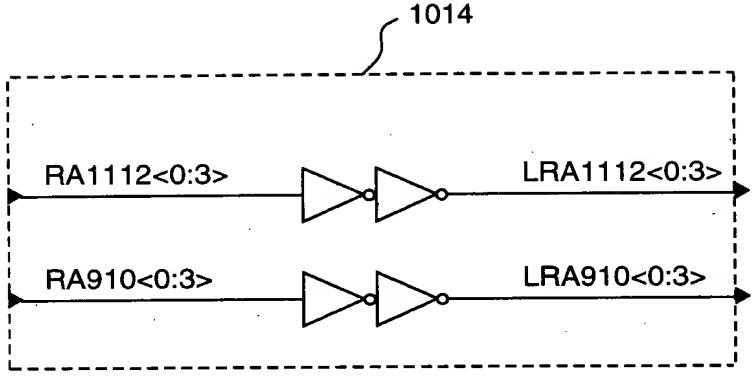


FIG. 68A

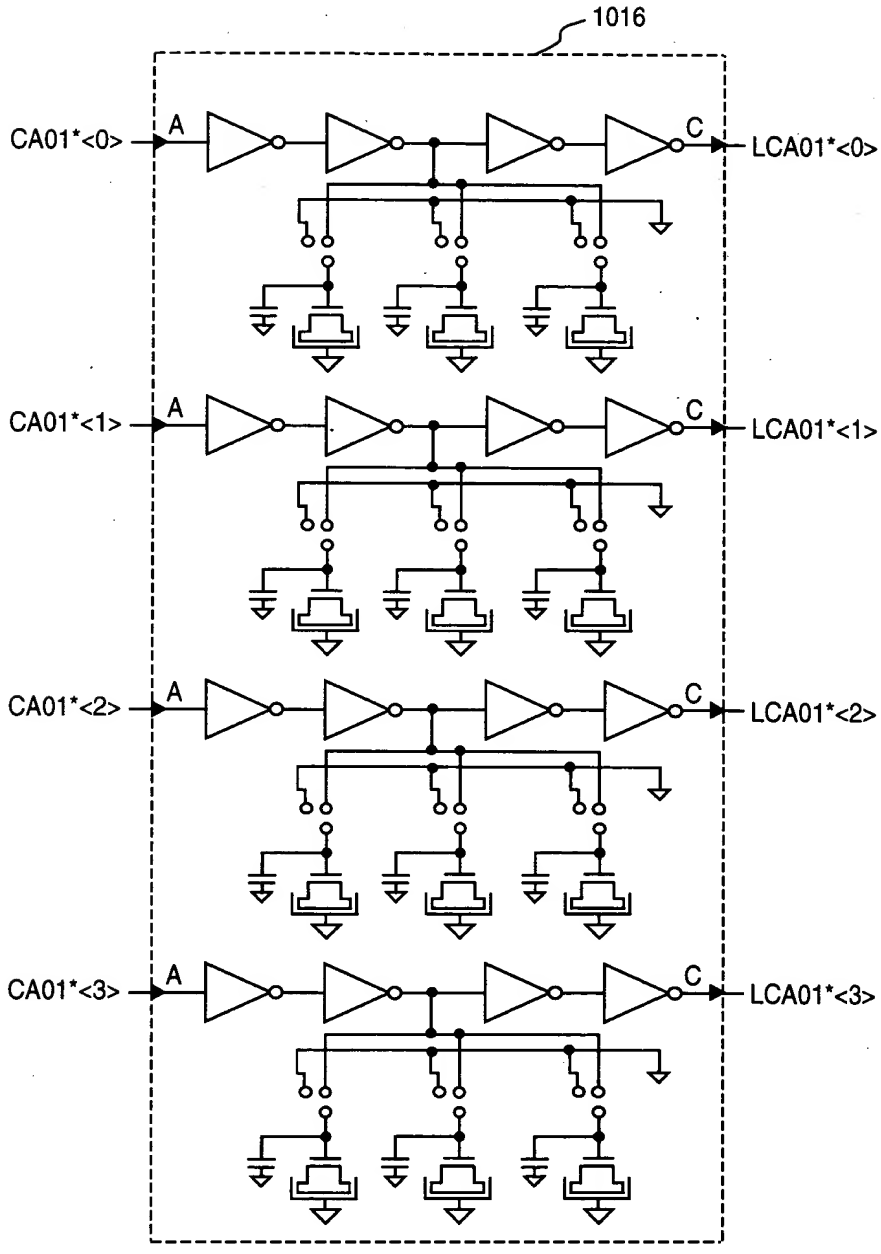

1016
CA01*<0>
A
C
LCA01*<0>
CA01*<1>
A
C
LCA01*<1>
CA01*<2>
A
C
LCA01*<2>
CA01*<3>
A
C
LCA01*<3>

FIG. 68B

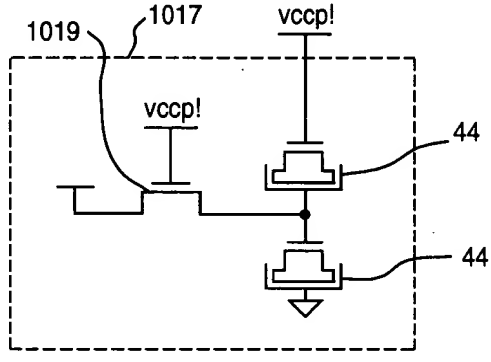


FIG. 69

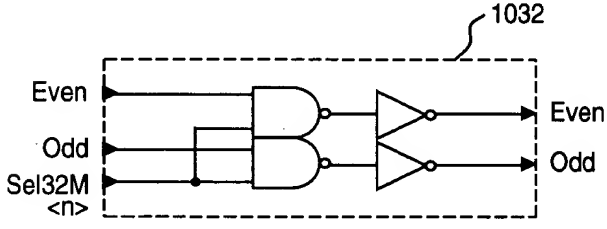


FIG. 70

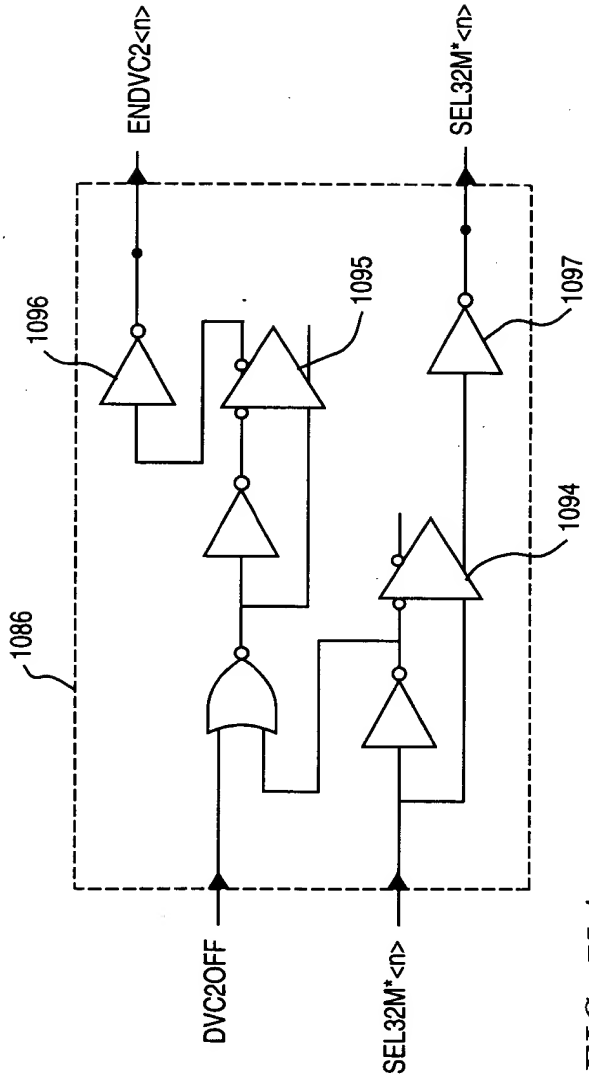


FIG. 71A

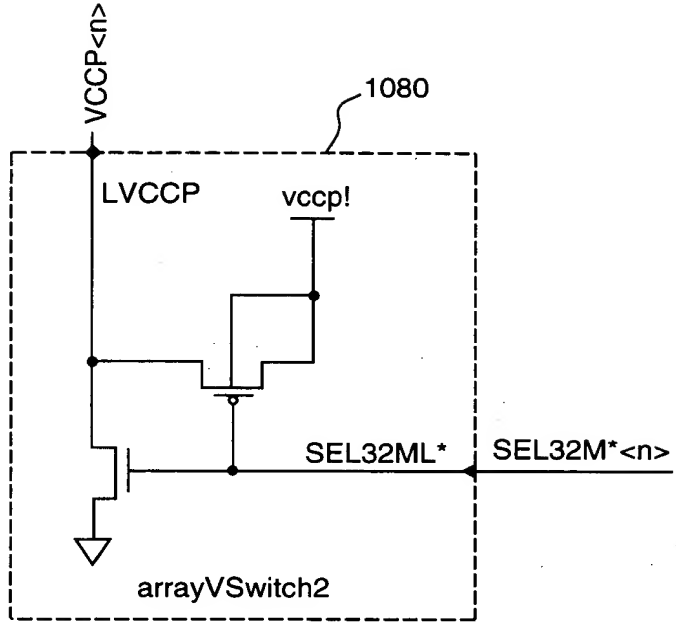


FIG. 71B

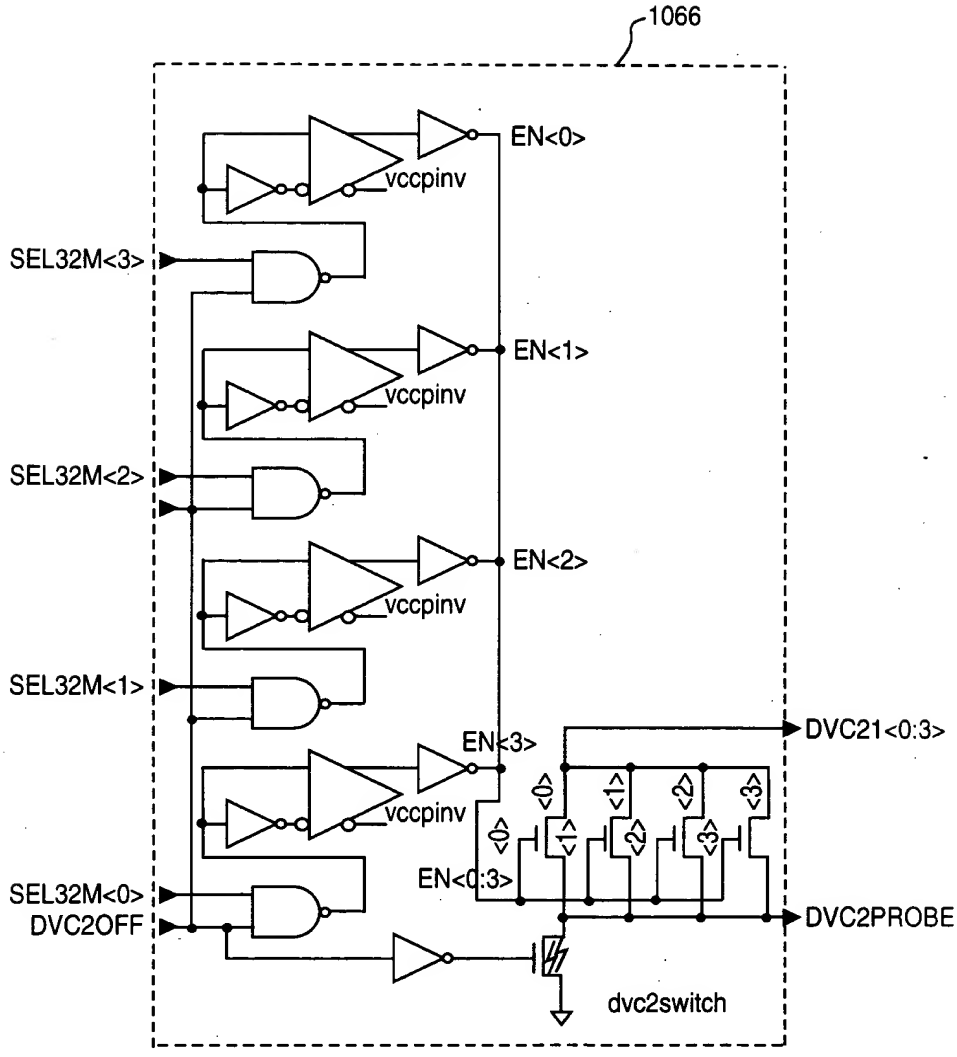

1066
EN<0>
vccpinv
SEL32M<3>
EN<1>
vccpinv
SEL32M<2>
EN<2>
vccpinv
SEL32M<1>
EN<3>
vccpinv
SEL32M<0>
DVC2OFF
EN<0:3>
DVC21<0:3>
DVC2PROBE
dvc2switch

FIG. 72A

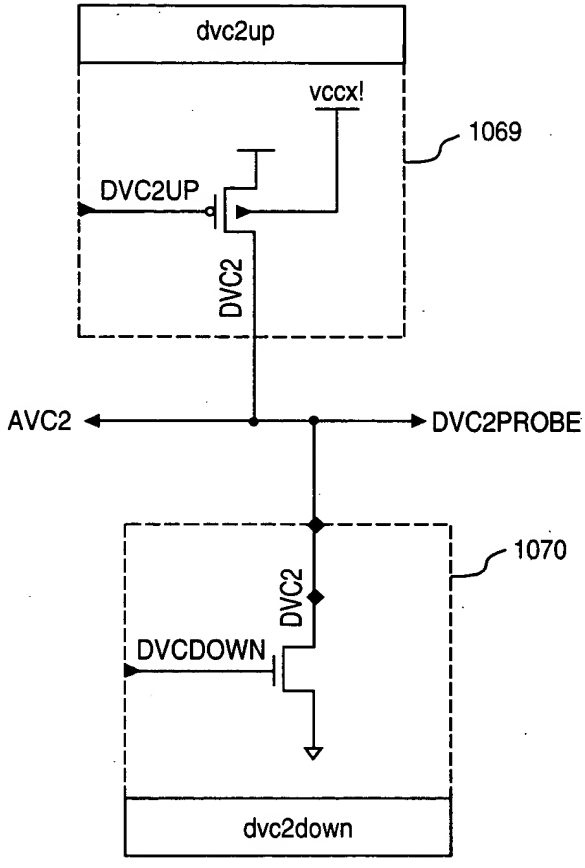

dvc2up
vccx!
1069
DVC2UP
DVC2
AVC2
DVC2PROBE
1070
DVC2
DVCDOWN
dvc2down

FIG. 72B

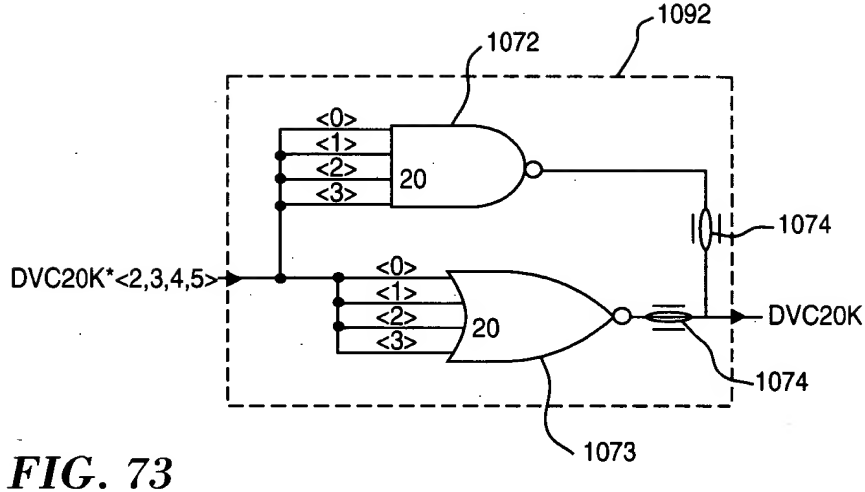


FIG. 73

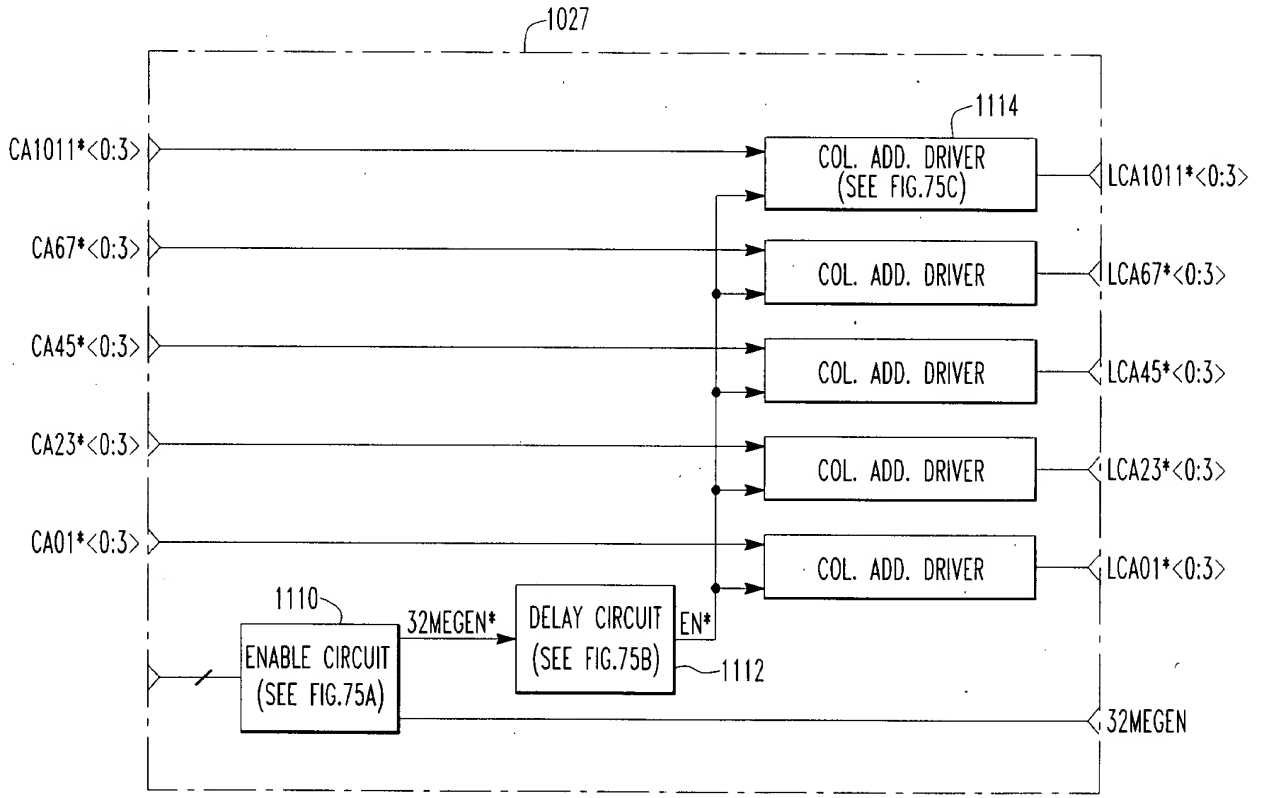

1027
1114
CA1011*<0:3>
CA67*<0:3>
CA45*<0:3>
CA23*<0:3>
CA01*<0:3>
COL. ADD. DRIVER (SEE FIG.75C)
COL. ADD. DRIVER
COL. ADD. DRIVER
COL. ADD. DRIVER
COL. ADD. DRIVER
LCA1011*<0:3>
LCA67*<0:3>
LCA45*<0:3>
LCA23*<0:3>
LCA01*<0:3>
1110
ENABLE CIRCUIT (SEE FIG.75A)
32MEGEN*
DELAY CIRCUIT (SEE FIG.75B)
EN*
1112
32MEGEN

FIG. 74

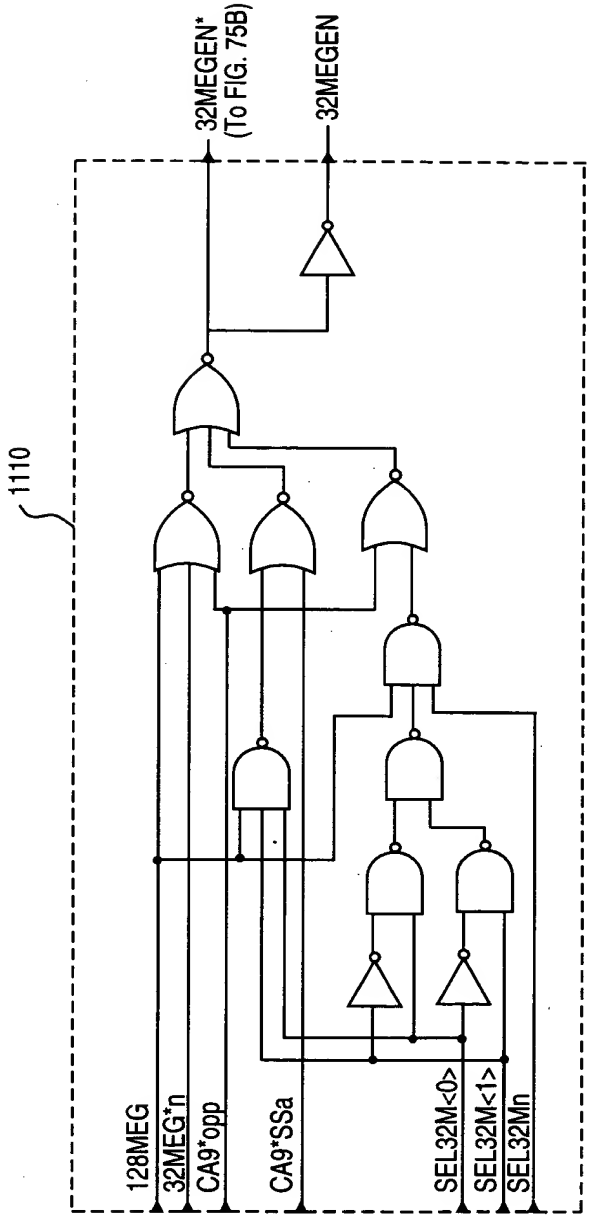

1110
32MEGEN*
(To FIG. 75B)
32MEGEN
128MEG
32MEG*n
CA9*opp
CA9*SSa
SEL32M<0>
SEL32M<1>
SEL32Mn

FIG. 75A

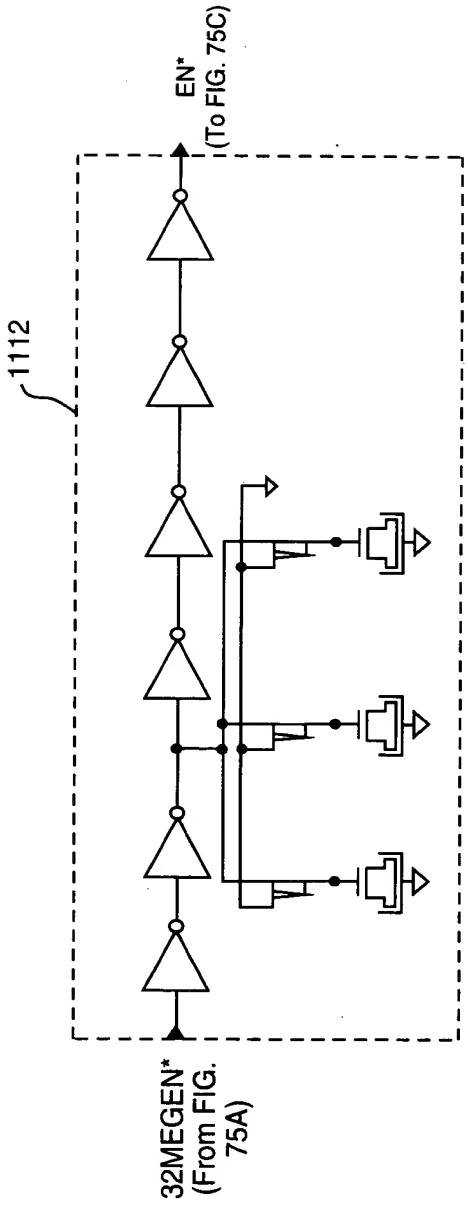


FIG. 75B

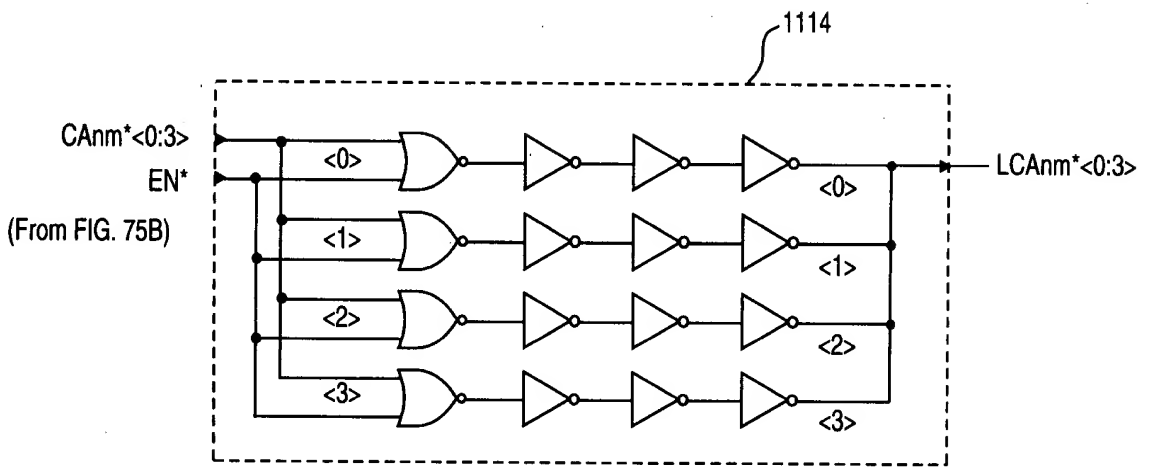


FIG. 75C

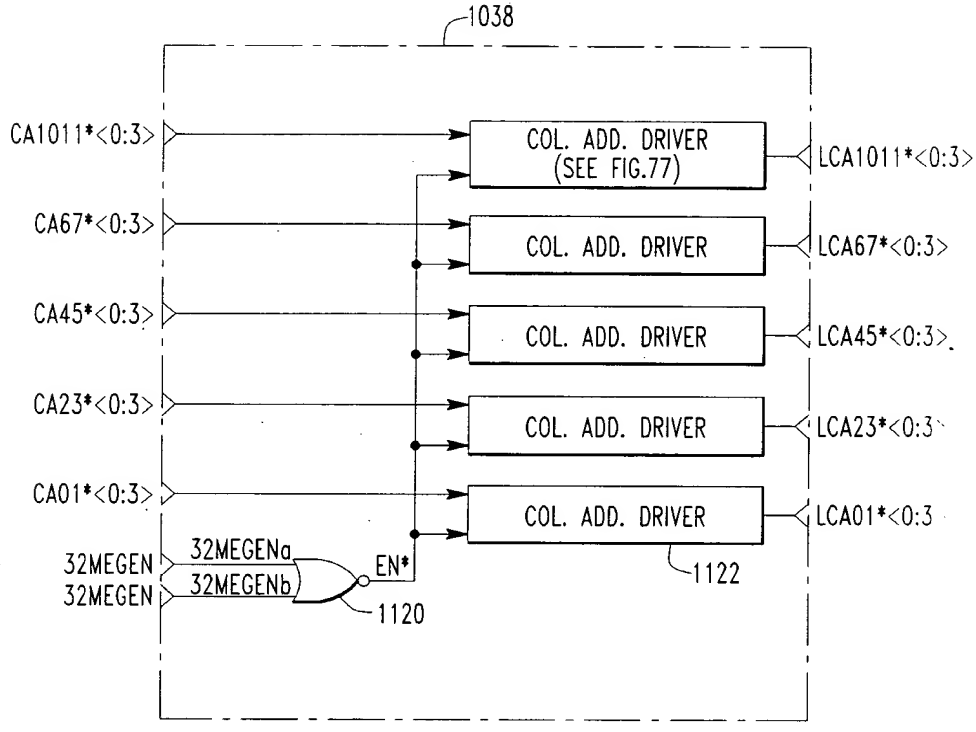

1038
CA1011*<0:3>
CA67*<0:3>
CA45*<0:3>
CA23*<0:3>
CA01*<0:3>
32MEGEN
32MEGEN
32MEGENa
32MEGENb
EN*
1120
COL. ADD. DRIVER
(SEE FIG.77)
COL. ADD. DRIVER
COL. ADD. DRIVER
COL. ADD. DRIVER
COL. ADD. DRIVER
1122
LCA1011*<0:3>
LCA67*<0:3>
LCA45*<0:3>
LCA23*<0:3
LCA01*<0:3

FIG. 76

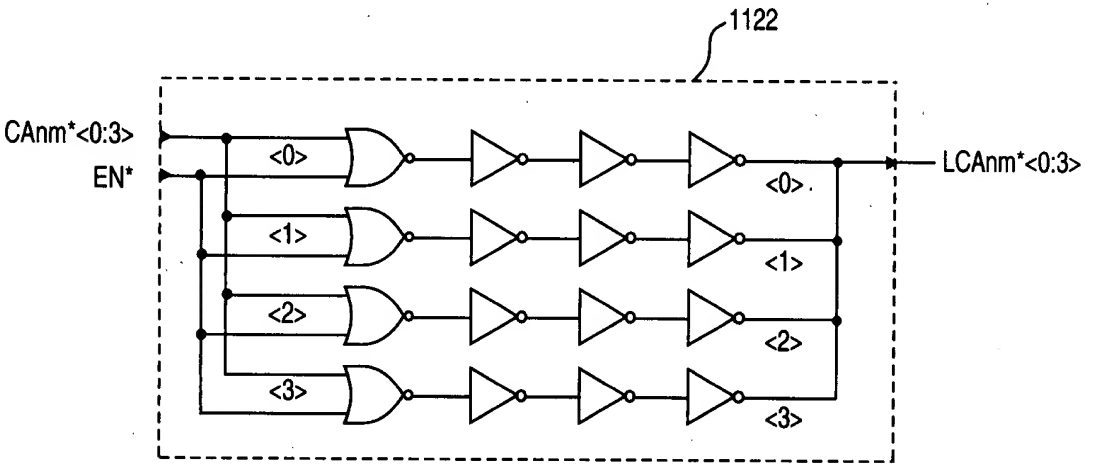


FIG. 77

09801638.030901

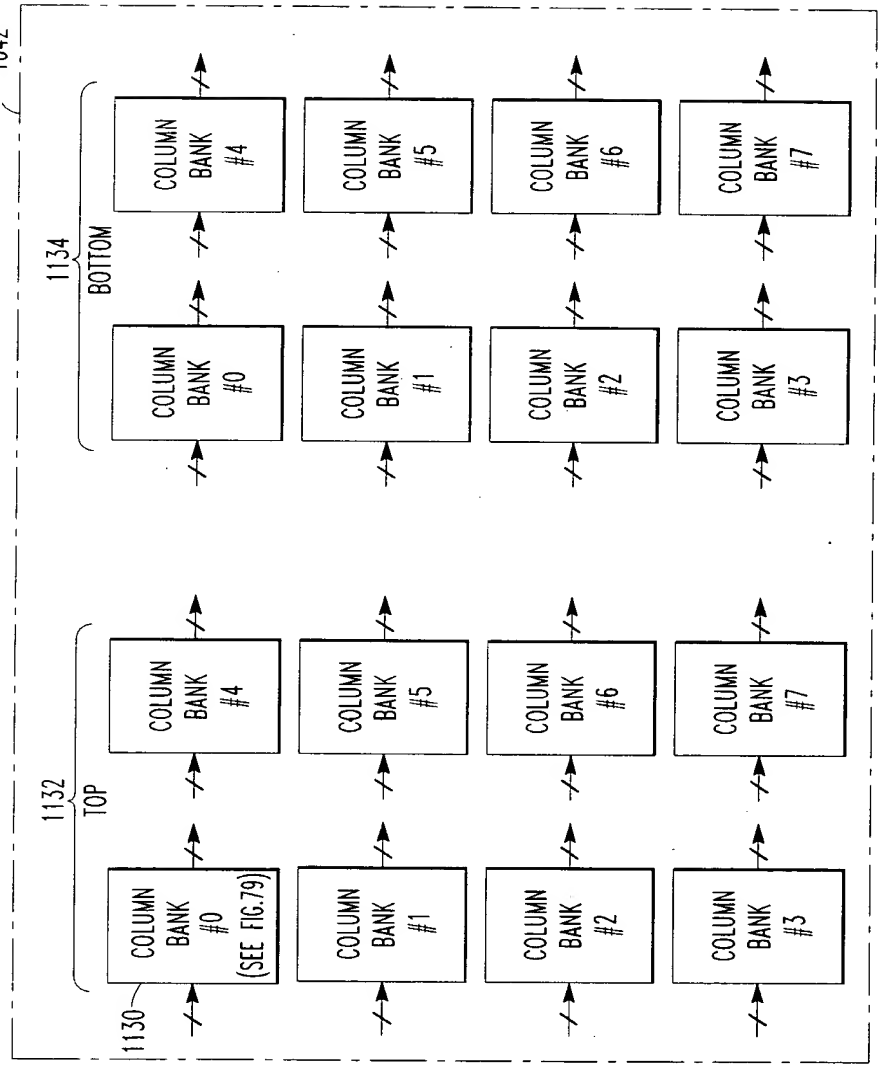

1042
1132
TOP
1134
BOTTOM
1130
COLUMN BANK #0 (SEE FIG.79)
COLUMN BANK #1
COLUMN BANK #2
COLUMN BANK #3
COLUMN BANK #4
COLUMN BANK #5
COLUMN BANK #6
COLUMN BANK #7
COLUMN BANK #0
COLUMN BANK #1
COLUMN BANK #2
COLUMN BANK #3
COLUMN BANK #4
COLUMN BANK #5
COLUMN BANK #6
COLUMN BANK #7

FIG. 78

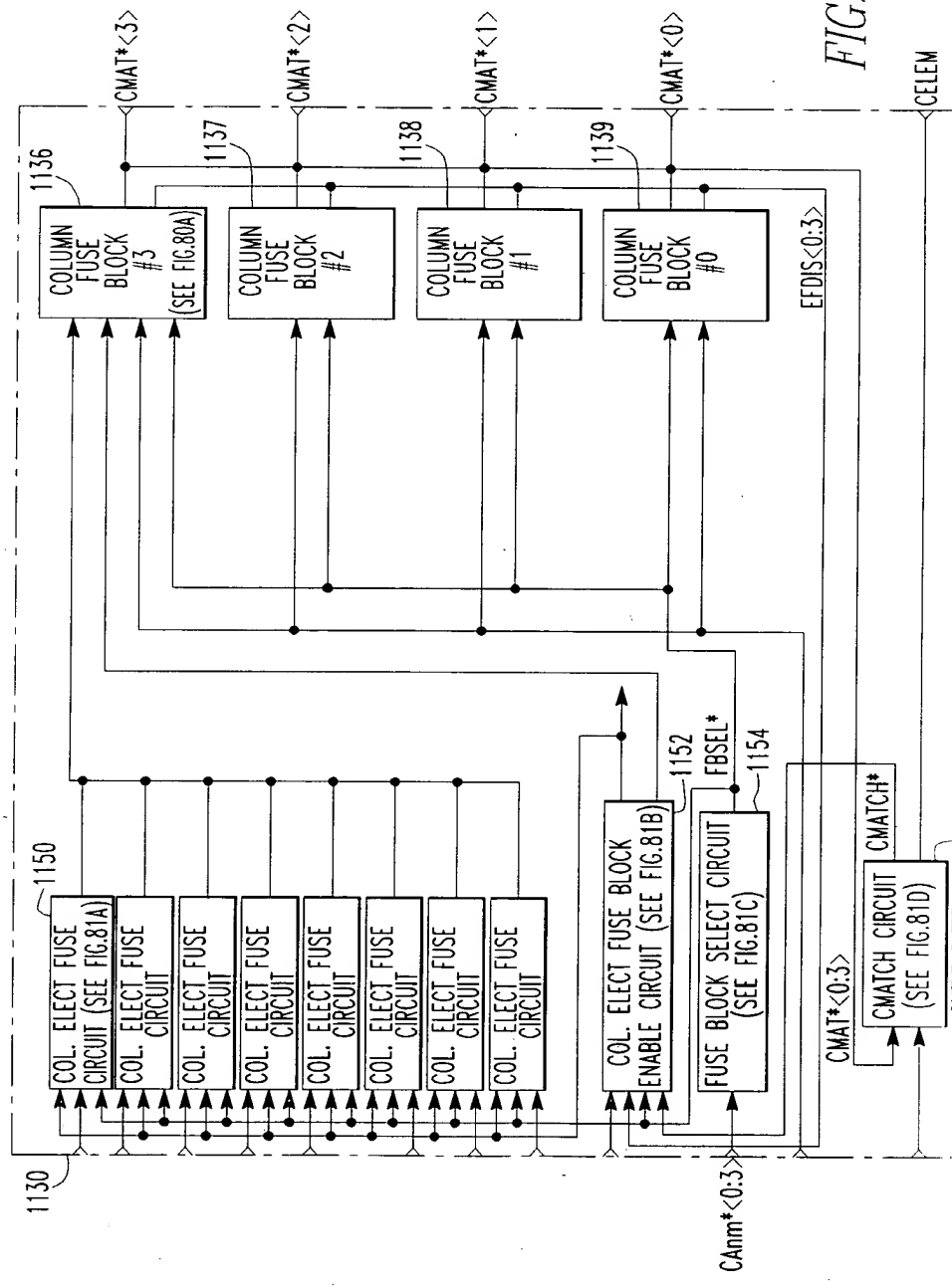

1130
1136
1137
1138
1139
1150
1152
1154
1156
CMAT*<3>
CMAT*<2>
CMAT*<1>
CMAT*<0>
CELEM
COLUMN FUSE BLOCK #3 (SEE FIG.80A)
COLUMN FUSE BLOCK #2
COLUMN FUSE BLOCK #1
COLUMN FUSE BLOCK #0
EFDIS<0:3>
COL. ELECT FUSE CIRCUIT (SEE FIG.81A)
COL. ELECT FUSE CIRCUIT
COL. ELECT FUSE BLOCK ENABLE CIRCUIT (SEE FIG.81B)
FBSEL*
FUSE BLOCK SELECT CIRCUIT (SEE FIG.81C)
CMAT*<0:3>
CMATCH CIRCUIT (SEE FIG.81D)
CMATCH*
CAnm*<0:3>

FIG. 79

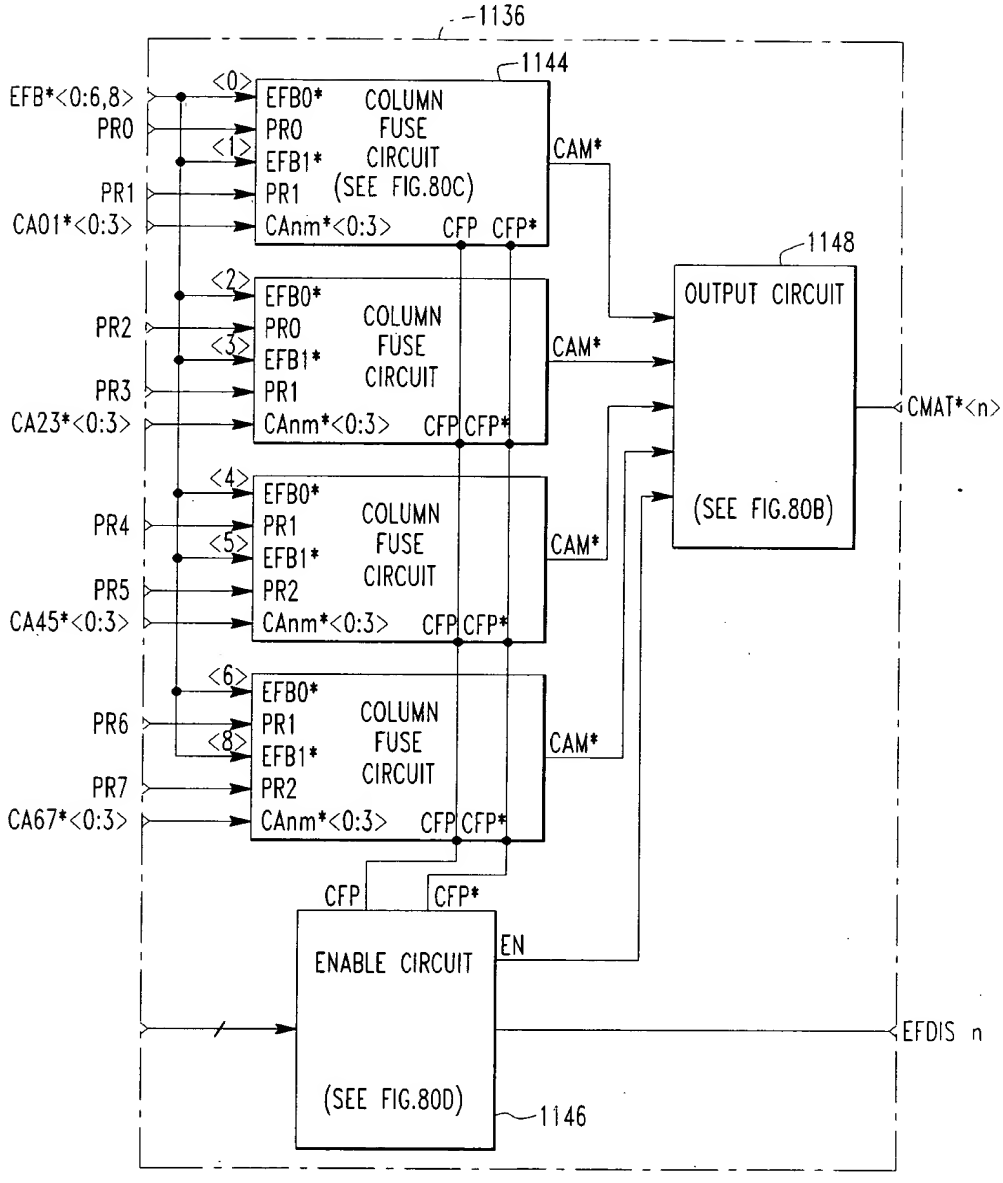

1136
1144
EFB*<0:6,8>
PR0
PR1
CA01*<0:3>
<0>
<1>
EFB0*
PR0
EFB1*
PR1
CAnm*<0:3>
COLUMN FUSE CIRCUIT
(SEE FIG.80C)
CFP CFP*
CAM*
1148
OUTPUT CIRCUIT
(SEE FIG.80B)
CMAT*<n>
PR2
PR3
CA23*<0:3>
<2>
<3>
PR4
PR5
CA45*<0:3>
<4>
<5>
PR6
PR7
CA67*<0:3>
<6>
<8>
CFP
CFP*
ENABLE CIRCUIT
(SEE FIG.80D)
1146
EN
EFDIS n

FIG. 80A

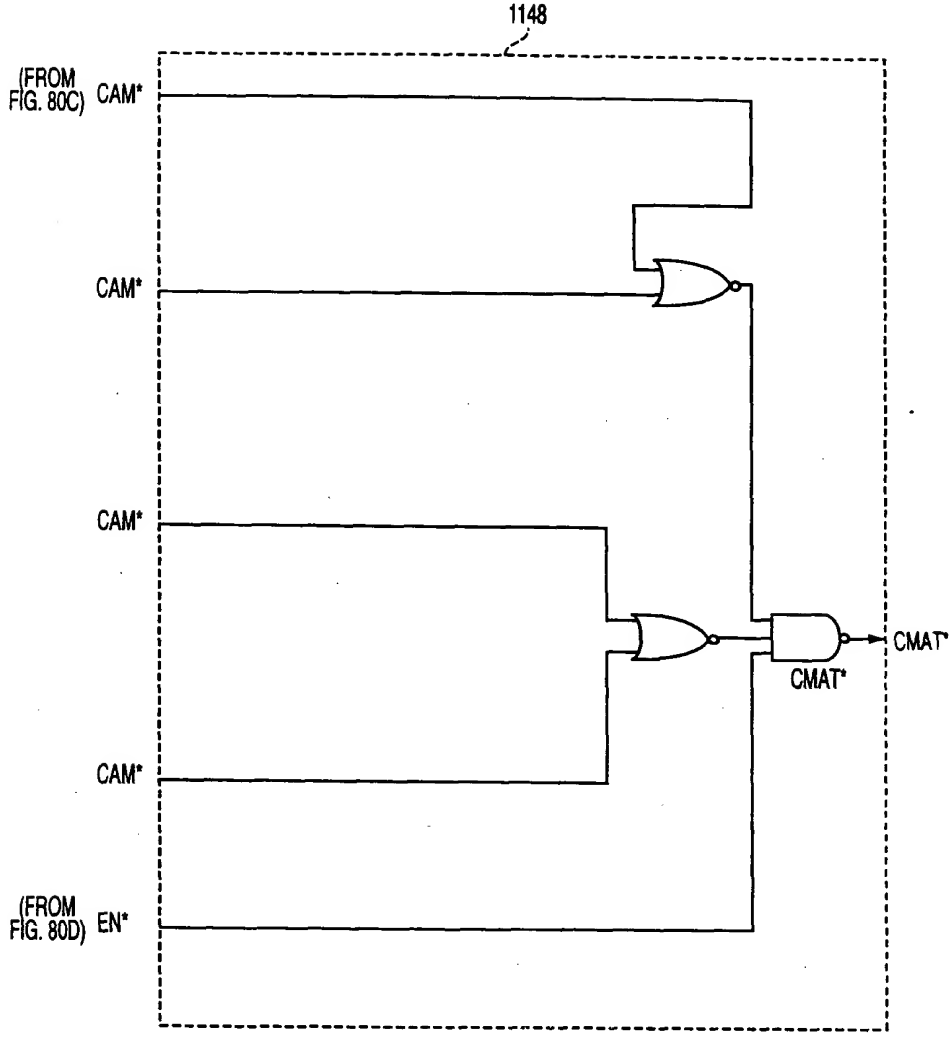


FIG. 80B

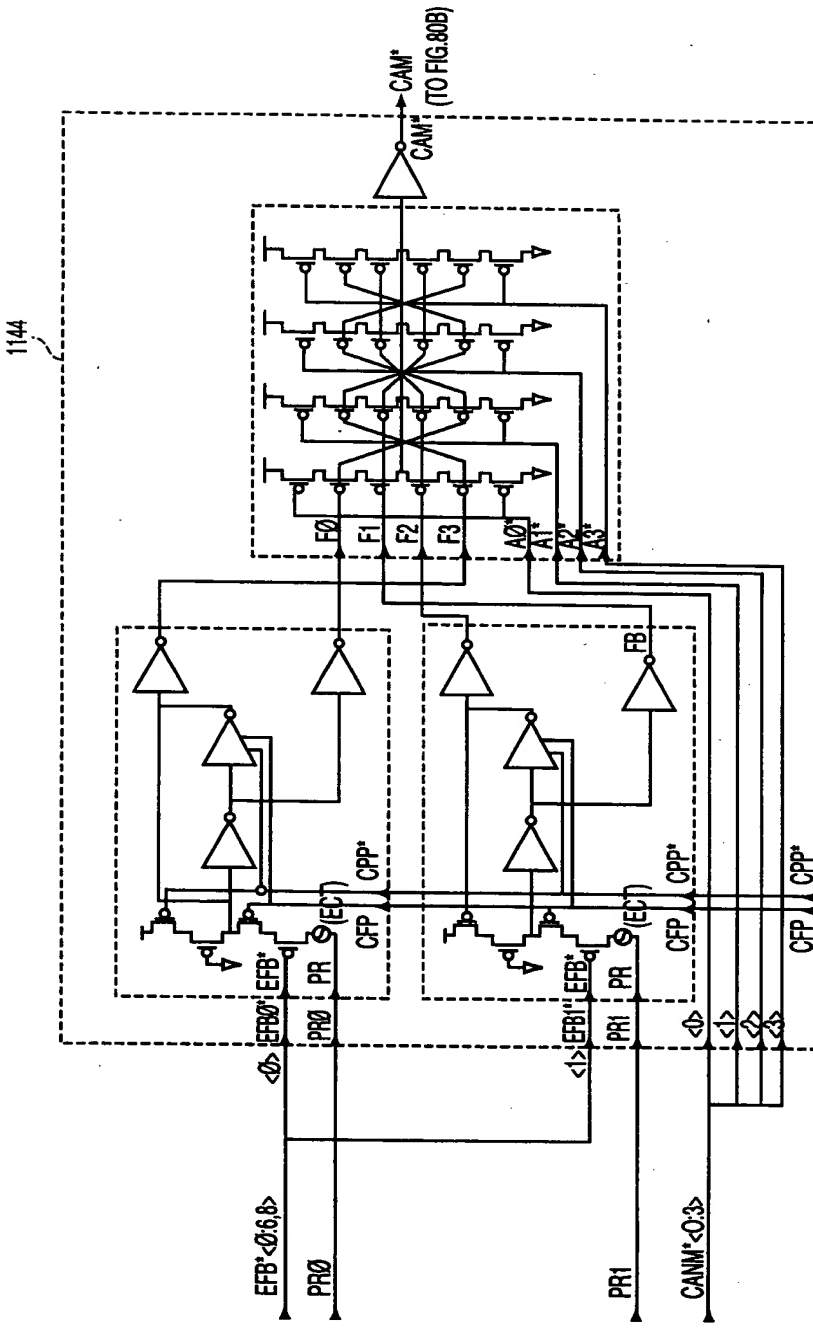
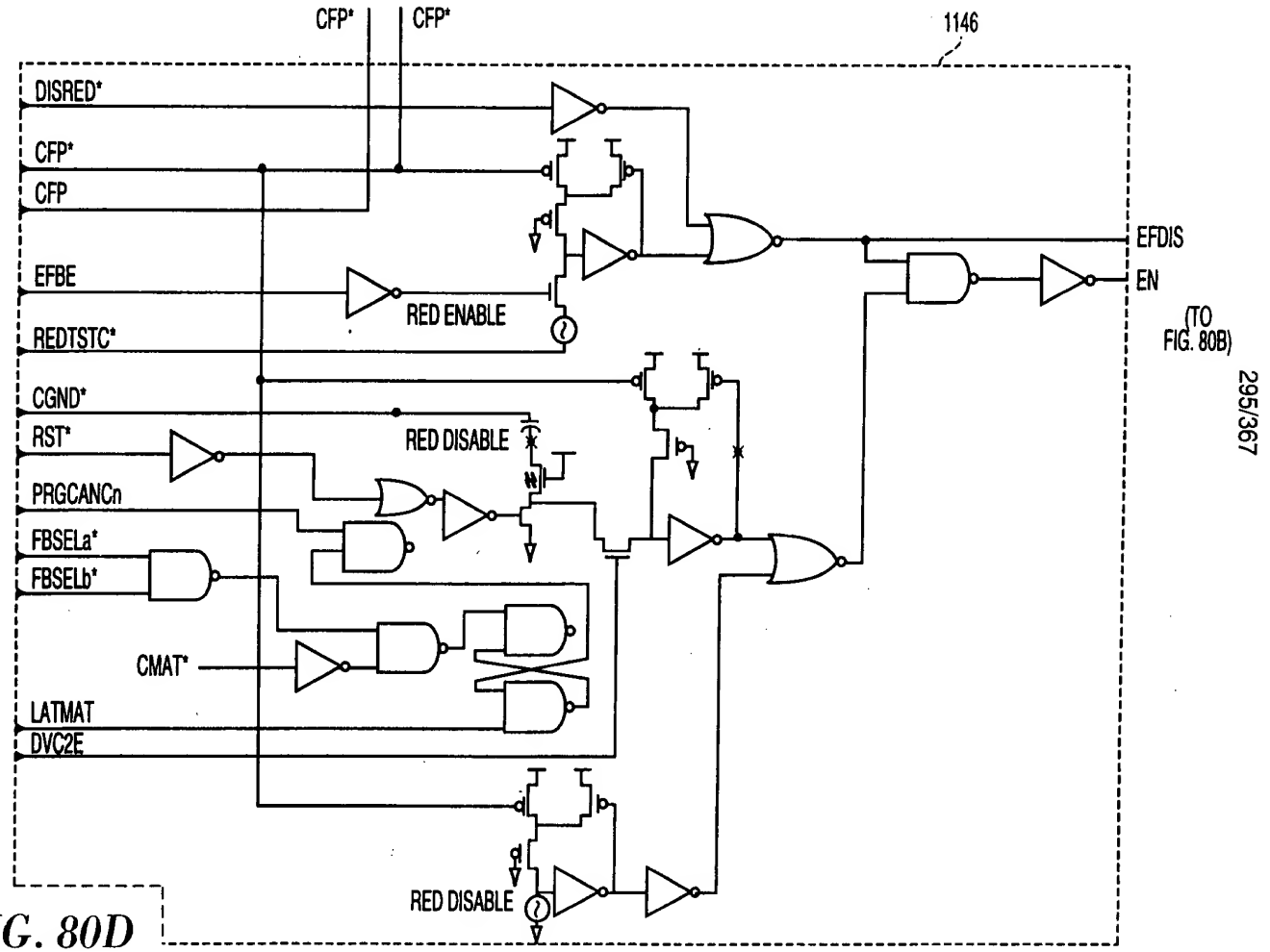

1144
CAM*
CAM*; (TO FIG.80B)
F0
F1
F2
F3
A0*
A1*
A2*
A3*
FB
CPP*
CFP
(EC1)
EFB*
PR
EFB0*
PR0
EFB1*
PR1
<0>
<1>
<2>
<3>
EFB*<0:6,8>
PR0
PR1
CANM*<0:3>

FIG. 80C



295/367

FIG. 80D

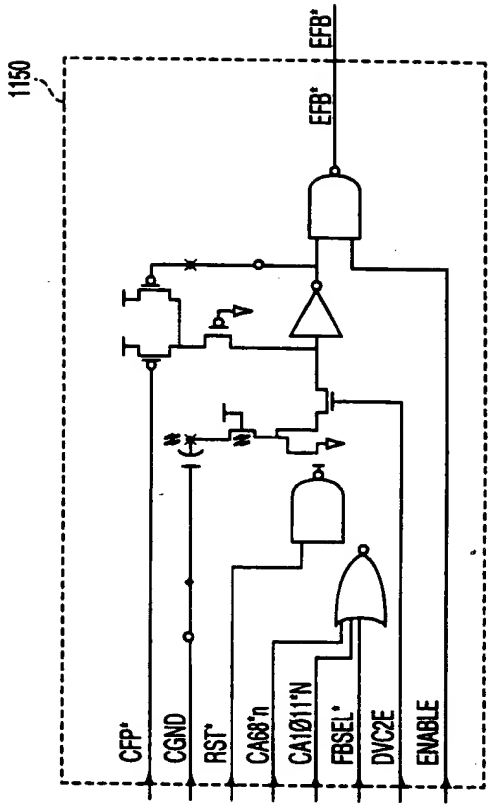


FIG. 81A

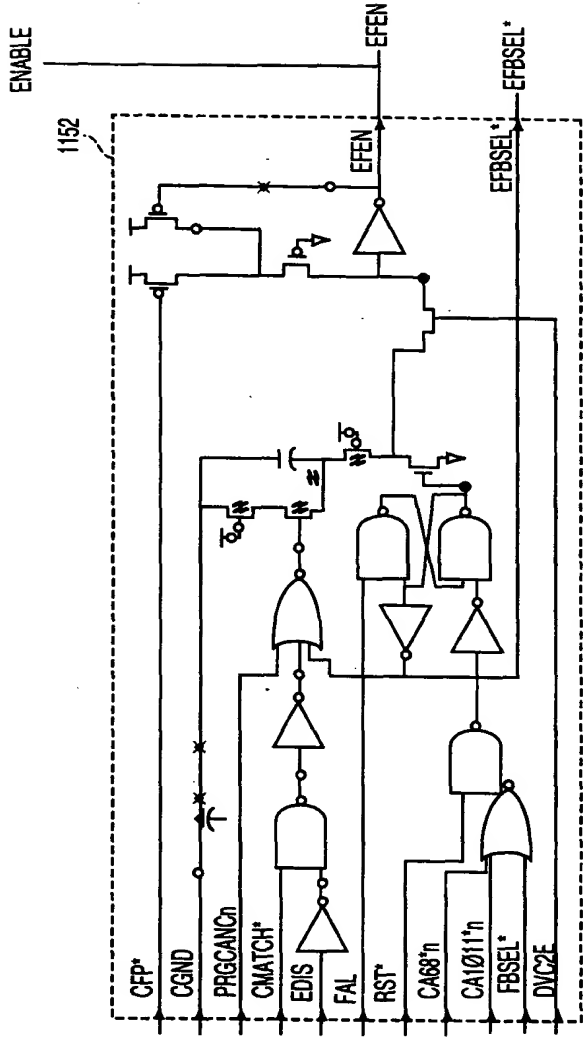

ENABLE
EFEN
EFBSEL*
1152
EFEN
EFBSEL*
CFP*
CGND
PRGCANCn
CMATCH*
EDIS
FAL
RST*
CA68*n
CA1Ø11*n
FBSEL*
DVC2E

FIG. 81B

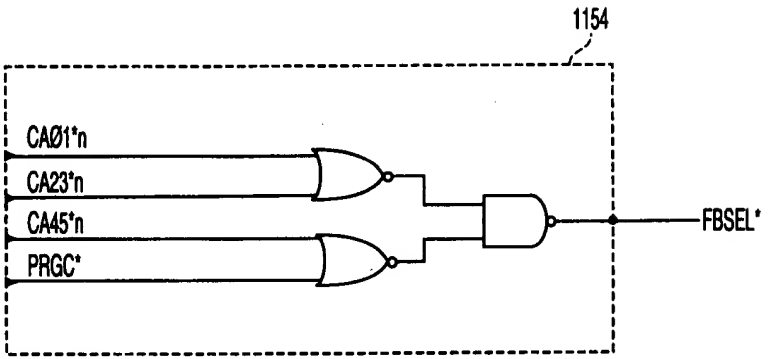


FIG. 81C

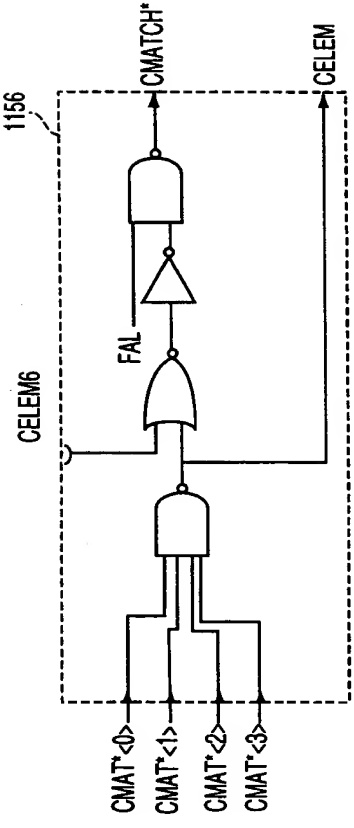


FIG. 81D

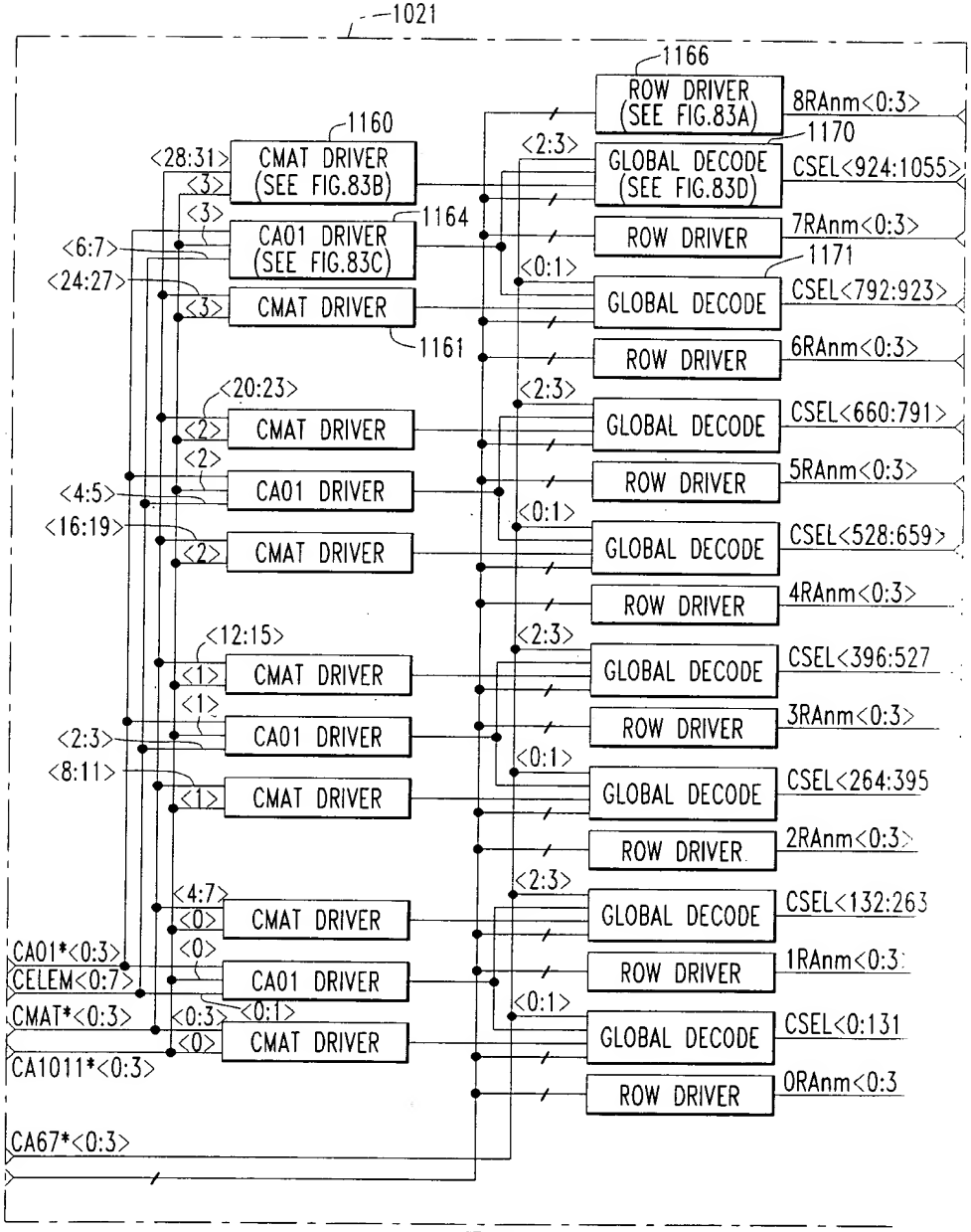

1021
1166
ROW DRIVER (SEE FIG.83A)
8RAnm<0:3>
1160
<28:31>
CMAT DRIVER (SEE FIG.83B)
<2:3>
1170
GLOBAL DECODE (SEE FIG.83D)
CSEL<924:1055>
<3>
<3>
1164
CA01 DRIVER (SEE FIG.83C)
ROW DRIVER
7RAnm<0:3>
<6:7>
<24:27>
<0:1>
1171
<3>
CMAT DRIVER
GLOBAL DECODE
CSEL<792:923>
1161
ROW DRIVER
6RAnm<0:3>
<20:23>
<2:3>
<2>
CMAT DRIVER
GLOBAL DECODE
CSEL<660:791>
<2>
ROW DRIVER
5RAnm<0:3>
<4:5>
CA01 DRIVER
<0:1>
<16:19>
<2>
CMAT DRIVER
GLOBAL DECODE
CSEL<528:659>
ROW DRIVER
4RAnm<0:3>
<12:15>
<2:3>
<1>
CMAT DRIVER
GLOBAL DECODE
CSEL<396:527
<1>
ROW DRIVER
3RAnm<0:3>
<2:3>
CA01 DRIVER
<0:1>
<8:11>
<1>
CMAT DRIVER
GLOBAL DECODE
CSEL<264:395
ROW DRIVER
2RAnm<0:3>
<4:7>
<2:3>
<0>
CMAT DRIVER
GLOBAL DECODE
CSEL<132:263
CA01*<0:3>
<0>
CELEM<0:7>
CA01 DRIVER
ROW DRIVER
1RAnm<0:3
<0:1>
CMAT*<0:3>
<0:3>
<0:1>
<0>
CMAT DRIVER
GLOBAL DECODE
CSEL<0:131
CA1011*<0:3>
ROW DRIVER
0RAnm<0:3
CA67*<0:3>

FIG. 82

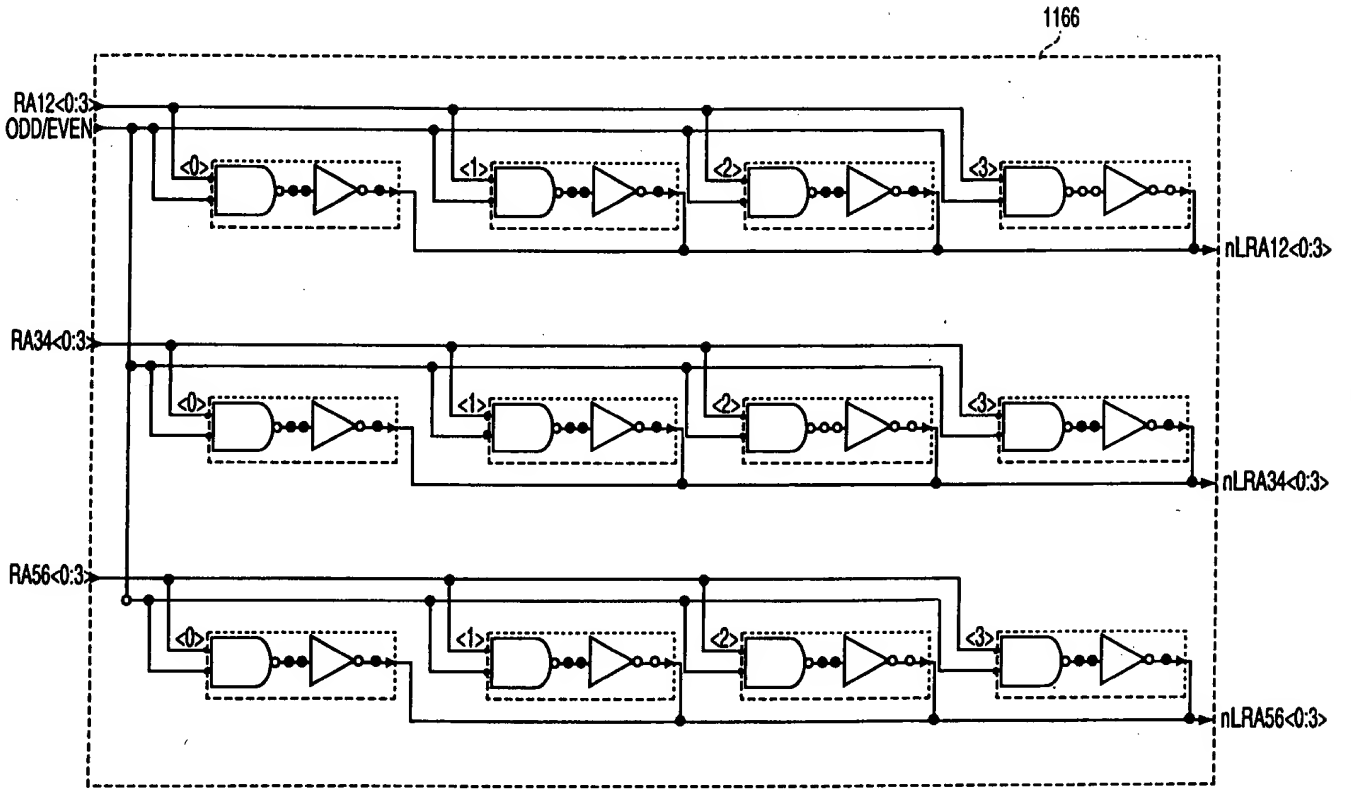

1166
RA12<0:3>
ODD/EVEN
<0>
<1>
<2>
<3>
nLRA12<0:3>
RA34<0:3>
<0>
<1>
<2>
<3>
nLRA34<0:3>
RA56<0:3>
<0>
<1>
<2>
<3>
nLRA56<0:3>

FIG. 83A

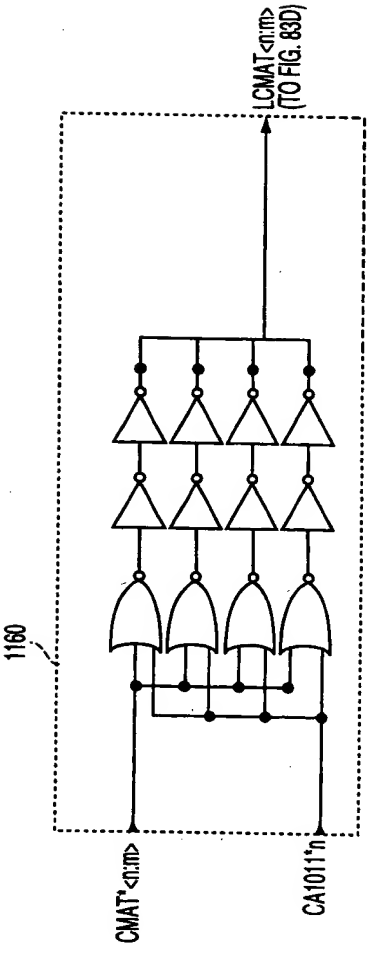


FIG. 83B

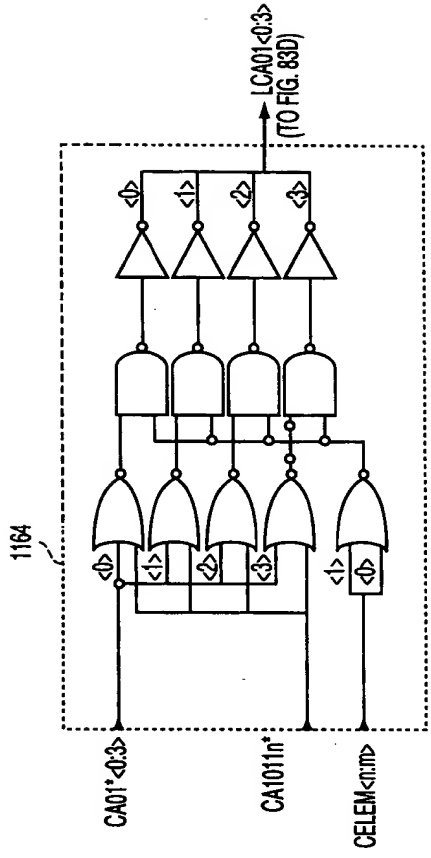


FIG. 83C

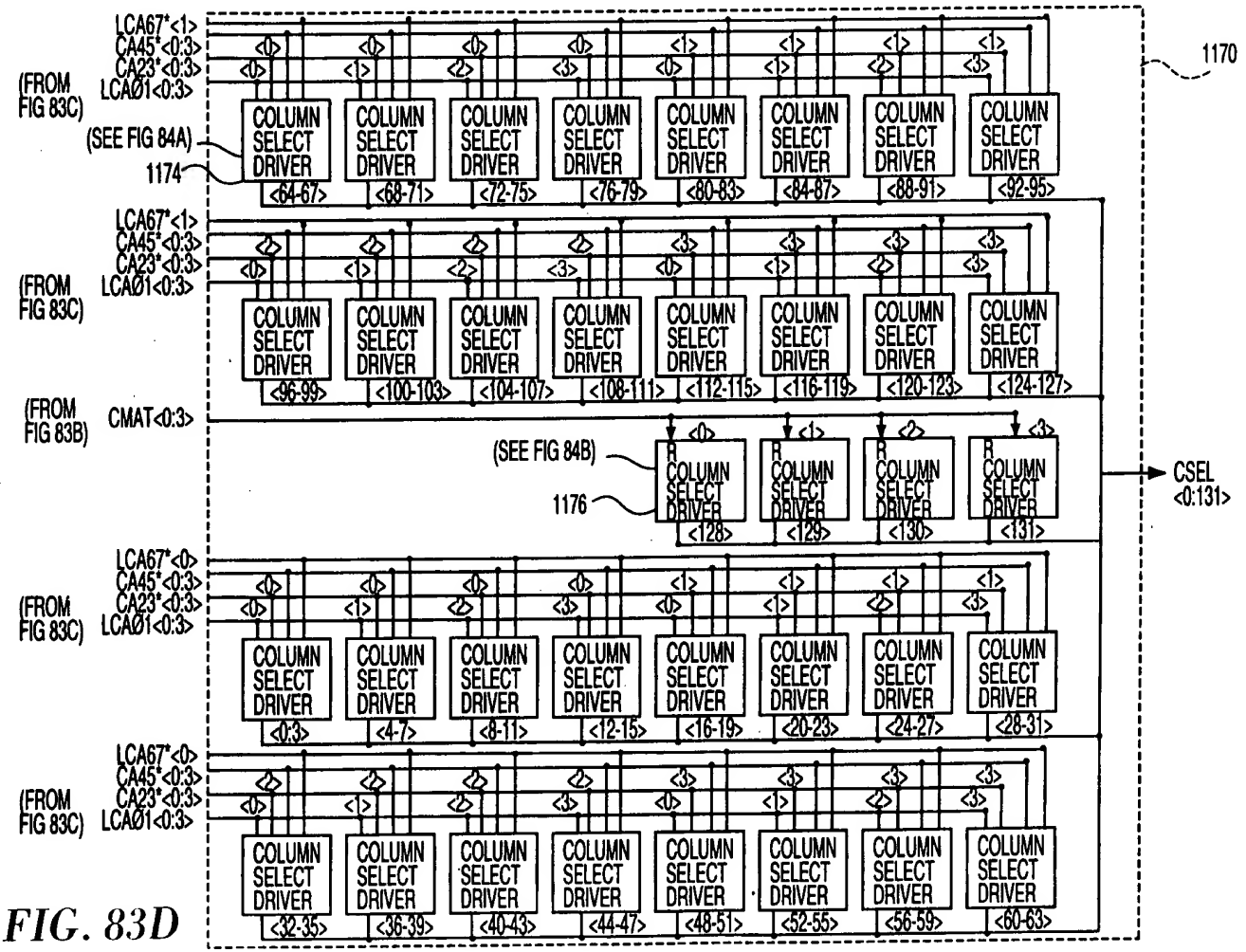

LCA67*<1>
CA45*<0:3>
CA23*<0:3>
(FROM FIG 83C) LCAØ1<0:3>
(SEE FIG 84A)
1174
COLUMN SELECT DRIVER
<64-67>
<68-71>
<72-75>
<76-79>
<80-83>
<84-87>
<88-91>
<92-95>
1170
<96-99>
<100-103>
<104-107>
<108-111>
<112-115>
<116-119>
<120-123>
<124-127>
(FROM FIG 83B) CMAT<0:3>
(SEE FIG 84B)
1176
R COLUMN SELECT DRIVER
<128>
<129>
<130>
<131>
CSEL <0:131>
LCA67*<0>
<0:3>
<4-7>
<8-11>
<12-15>
<16-19>
<20-23>
<24-27>
<28-31>
<32-35>
<36-39>
<40-43>
<44-47>
<48-51>
<52-55>
<56-59>
<60-63>

FIG. 83D

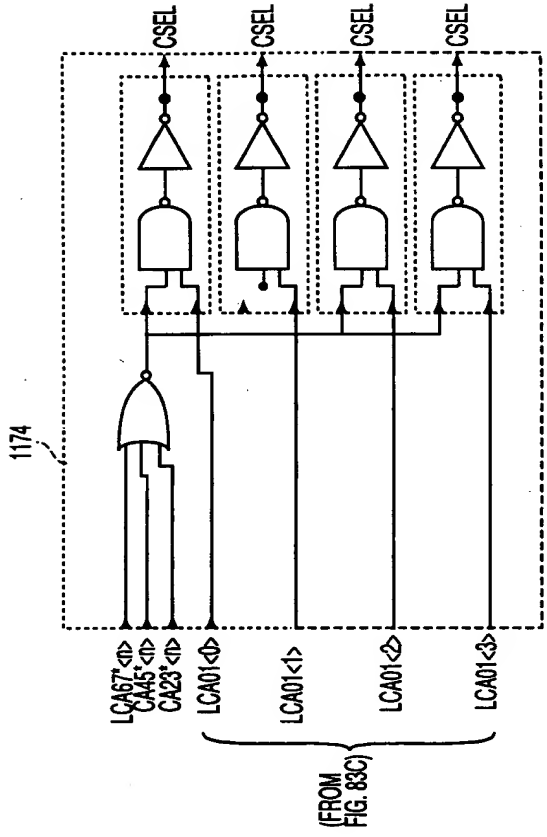

CSEL
CSEL
CSEL
CSEL
1174
LCA67<1>
CA45<1>
CA23<1>
LCA01<0>
LCA01<1>
LCA01<2>
LCA01<3>
(FROM FIG. 83C)

FIG. 84A

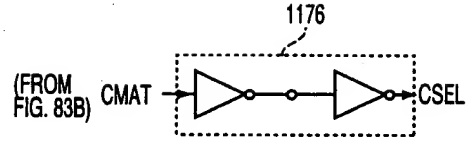


FIG. 84B

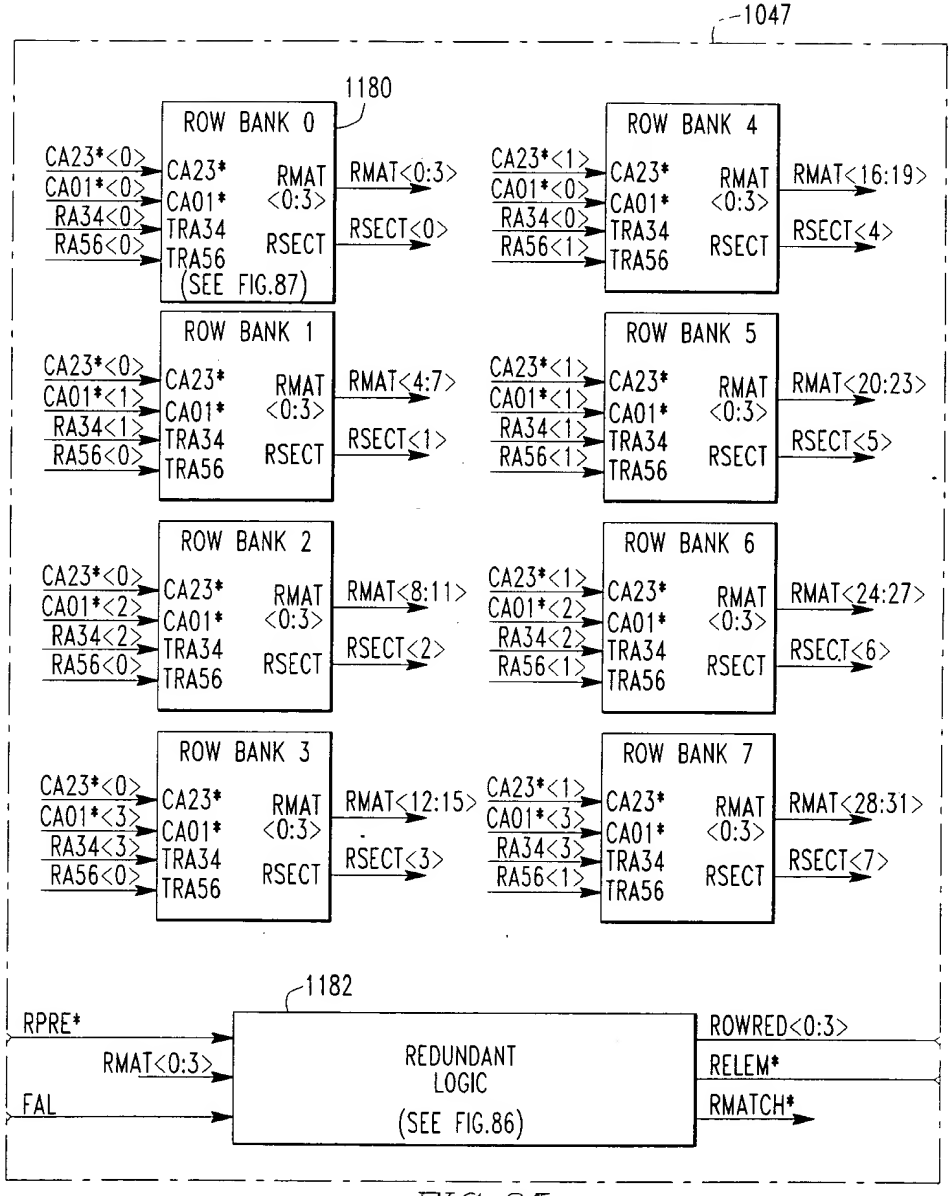

1047
1180
ROW BANK 0
CA23*<0>
CA01*<0>
RA34<0>
RA56<0>
CA23*
CA01*
TRA34
TRA56
RMAT <0:3>
RSECT
RMAT<0:3>
RSECT<0>
(SEE FIG.87)
ROW BANK 4
CA23*<1>
CA01*<0>
RA34<0>
RA56<1>
RMAT<16:19>
RSECT<4>
ROW BANK 1
CA23*<0>
CA01*<1>
RA34<1>
RA56<0>
RMAT<4:7>
RSECT<1>
ROW BANK 5
CA23*<1>
CA01*<1>
RA34<1>
RA56<1>
RMAT<20:23>
RSECT<5>
ROW BANK 2
CA23*<0>
CA01*<2>
RA34<2>
RA56<0>
RMAT<8:11>
RSECT<2>
ROW BANK 6
CA23*<1>
CA01*<2>
RA34<2>
RA56<1>
RMAT<24:27>
RSECT<6>
ROW BANK 3
CA23*<0>
CA01*<3>
RA34<3>
RA56<0>
RMAT<12:15>
RSECT<3>
ROW BANK 7
CA23*<1>
CA01*<3>
RA34<3>
RA56<1>
RMAT<28:31>
RSECT<7>
1182
RPRE*
RMAT<0:3>
FAL
REDUNDANT LOGIC
(SEE FIG.86)
ROWRED<0:3>
RELEM*
RMATCH*

FIG. 85

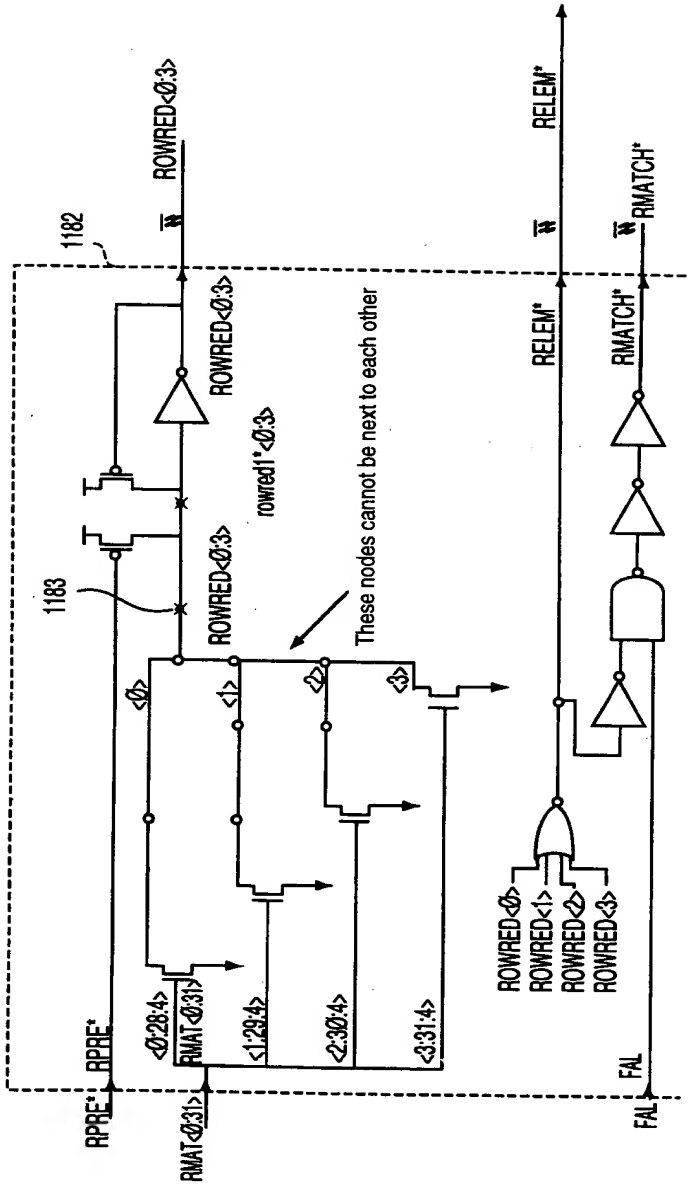

1182
1183
ROWRED<0:3>
ROWRED<0:3>
rowred1*<0:3>
ROWRED<0:3>
These nodes cannot be next to each other
RELEM*
RELEM*
RMATCH*
RMATCH*
RPRE*
RPRE*
RMAT<0:31>
<0:28:4>
RMAT<0:31>
<1:29:4>
<2:30:4>
<3:31:4>
ROWRED<0>
ROWRED<1>
ROWRED<2>
ROWRED<3>
FAL
FAL

FIG. 86

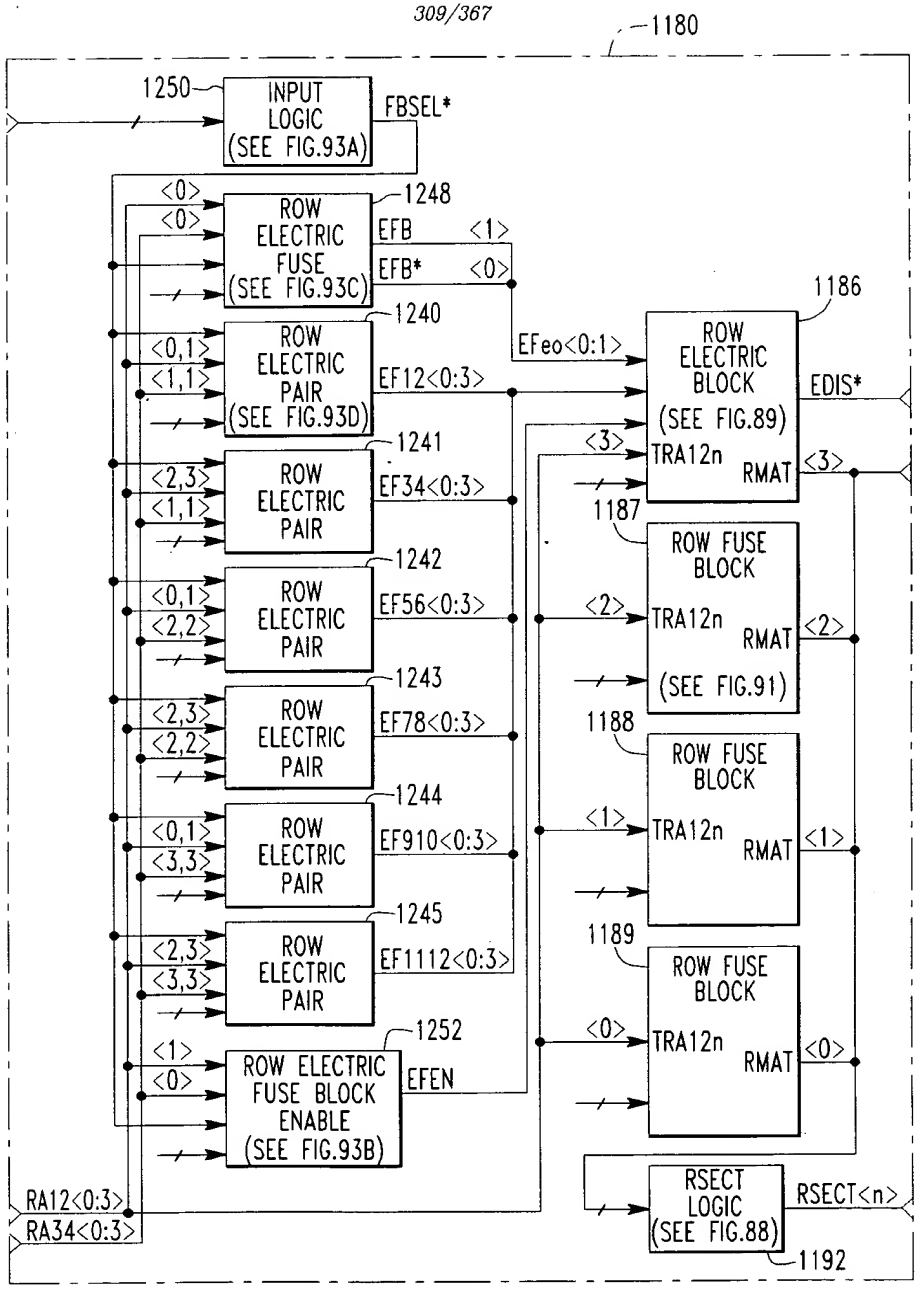

1180
1250
INPUT LOGIC (SEE FIG.93A)
FBSEL*
ROW ELECTRIC FUSE (SEE FIG.93C)
1248
EFB
EFB*
ROW ELECTRIC PAIR (SEE FIG.93D)
1240
EF12<0:3>
ROW ELECTRIC PAIR
1241
EF34<0:3>
ROW ELECTRIC PAIR
1242
EF56<0:3>
ROW ELECTRIC PAIR
1243
EF78<0:3>
ROW ELECTRIC PAIR
1244
EF910<0:3>
ROW ELECTRIC PAIR
1245
EF1112<0:3>
ROW ELECTRIC FUSE BLOCK ENABLE (SEE FIG.93B)
1252
EFEN
EFeo<0:1>
ROW ELECTRIC BLOCK (SEE FIG.89)
1186
EDIS*
TRA12n
RMAT
ROW FUSE BLOCK
1187
(SEE FIG.91)
1188
1189
RSECT LOGIC (SEE FIG.88)
RSECT<n>
1192
RA12<0:3>
RA34<0:3>

FIG. 87

Printed: 25.05.2004

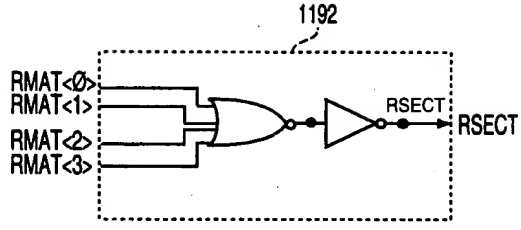


FIG. 88

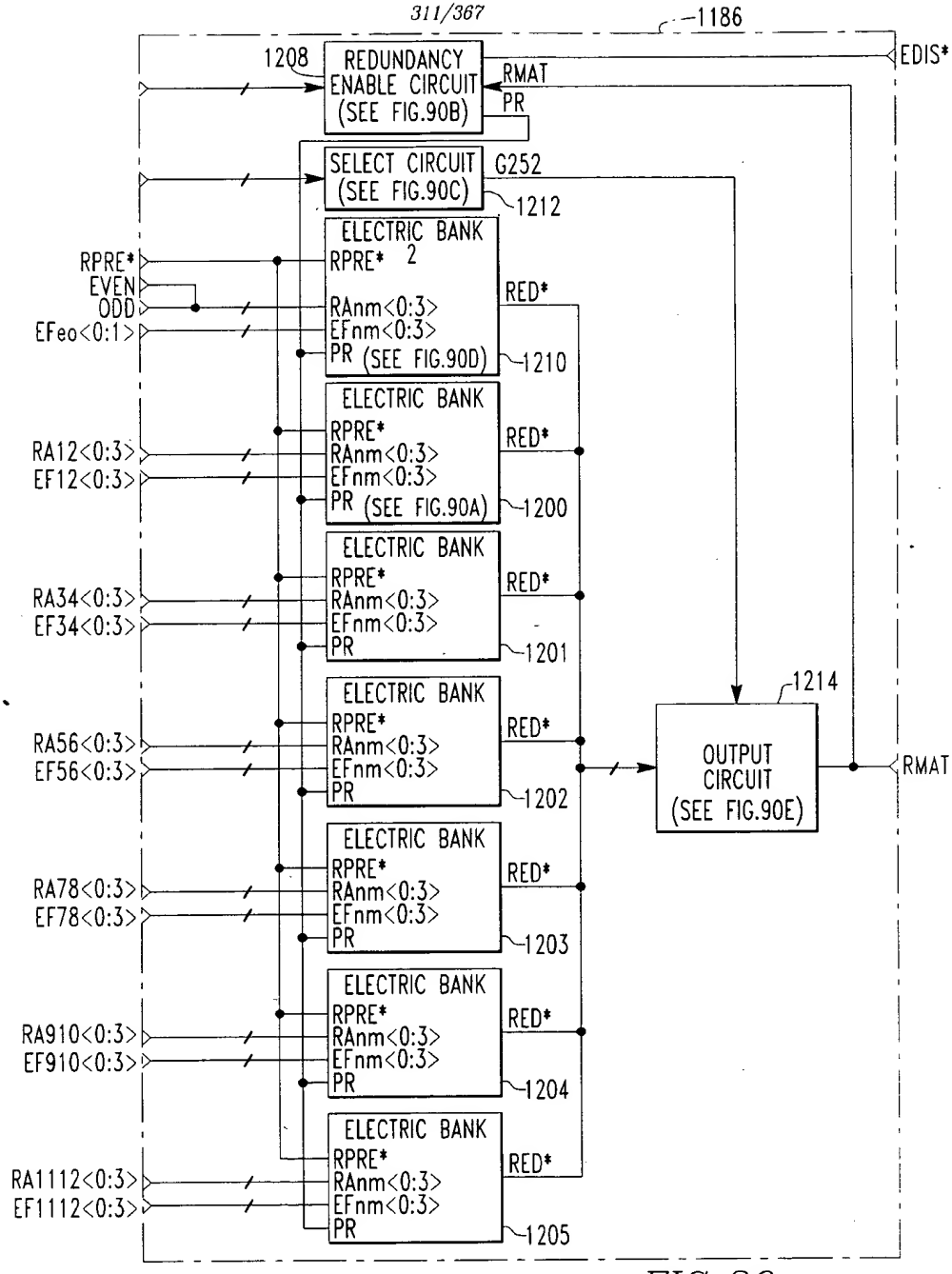

1186
1208
REDUNDANCY ENABLE CIRCUIT (SEE FIG.90B)
RMAT
PR
EDIS*
SELECT CIRCUIT (SEE FIG.90C)
G252
1212
ELECTRIC BANK 2
RPRE*
RAnm<0:3>
EFnm<0:3>
PR (SEE FIG.90D)
RED*
1210
ELECTRIC BANK
RPRE*
RAnm<0:3>
EFnm<0:3>
PR (SEE FIG.90A)
RED*
1200
ELECTRIC BANK
RPRE*
RAnm<0:3>
EFnm<0:3>
PR
RED*
1201
ELECTRIC BANK
RPRE*
RAnm<0:3>
EFnm<0:3>
PR
RED*
1202
ELECTRIC BANK
RPRE*
RAnm<0:3>
EFnm<0:3>
PR
RED*
1203
ELECTRIC BANK
RPRE*
RAnm<0:3>
EFnm<0:3>
PR
RED*
1204
ELECTRIC BANK
RPRE*
RAnm<0:3>
EFnm<0:3>
PR
RED*
1205
1214
OUTPUT CIRCUIT (SEE FIG.90E)
RMAT
RPRE*
EVEN
ODD
EFeo<0:1>
RA12<0:3>
EF12<0:3>
RA34<0:3>
EF34<0:3>
RA56<0:3>
EF56<0:3>
RA78<0:3>
EF78<0:3>
RA910<0:3>
EF910<0:3>
RA1112<0:3>
EF1112<0:3>

FIG. 89

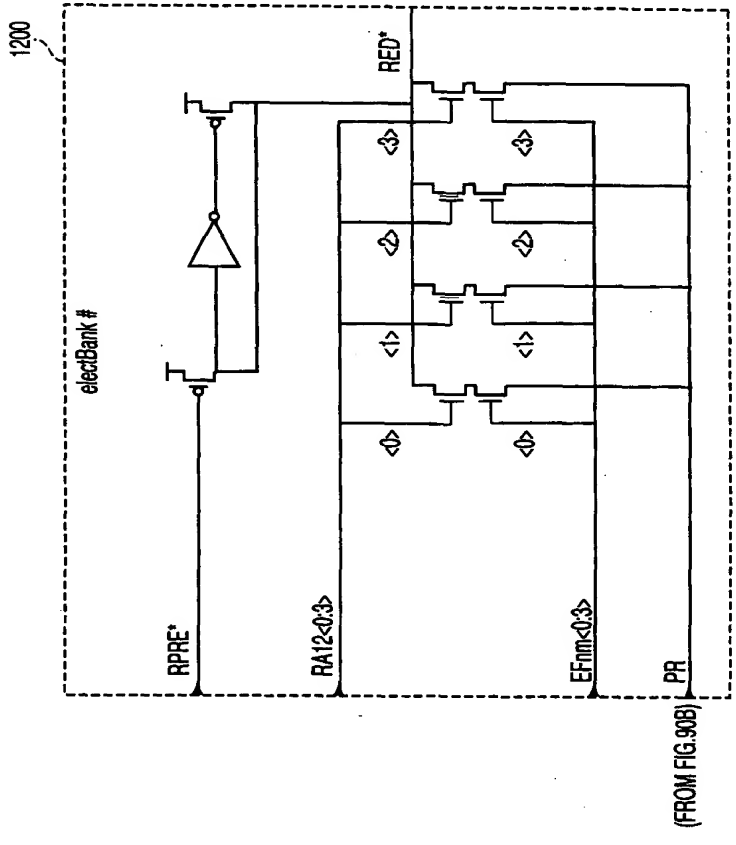


FIG. 90A

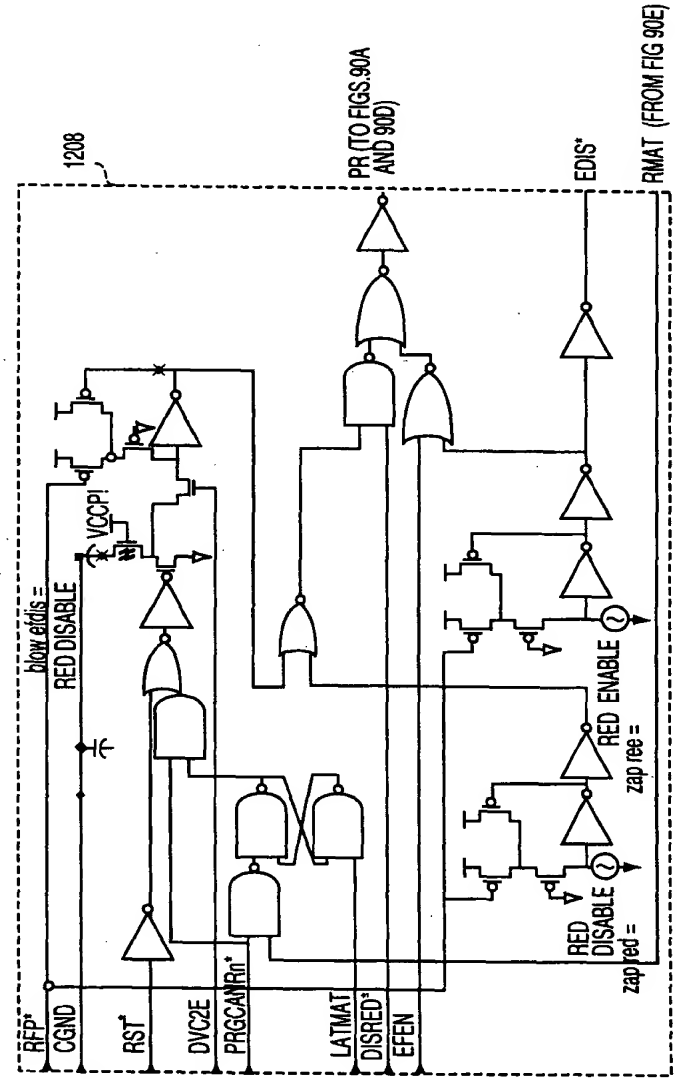

1208
PR (TO FIGS.90A AND 90D)
EDIS'
RMAT (FROM FIG 90E)
blow efdis =
RED DISABLE
VCCP1
RFP'
CGND
RST'
DVC2E
PRGCAMRn'
LATMAT
DISRED'
EFEN
RED ENABLE
zap ree =
RED DISABLE
zap red =

FIG. 90B

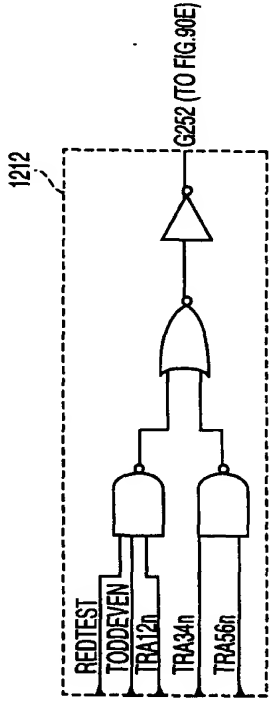


FIG. 90C

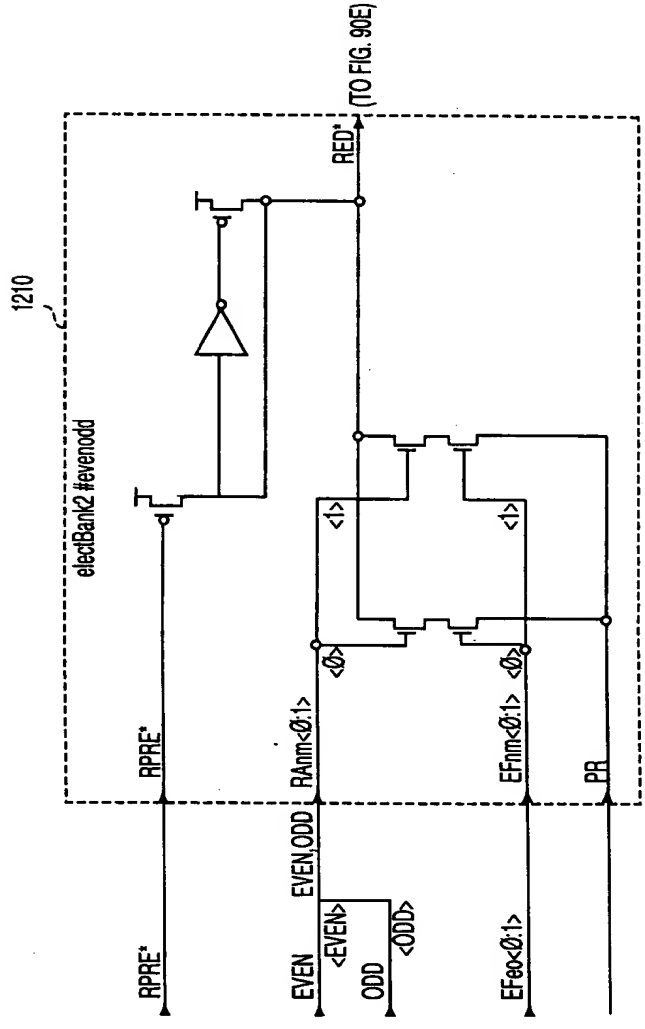

1210
electBank2 #evenodd
RPRE*
RAnm<Ø:1>
EFnm<Ø:1>
PR
RED*
(TO FIG. 90E)
<Ø>
<1>
EVEN,ODD
EVEN
<EVEN>
ODD
<ODD>
EFec<Ø:1>

FIG. 90D

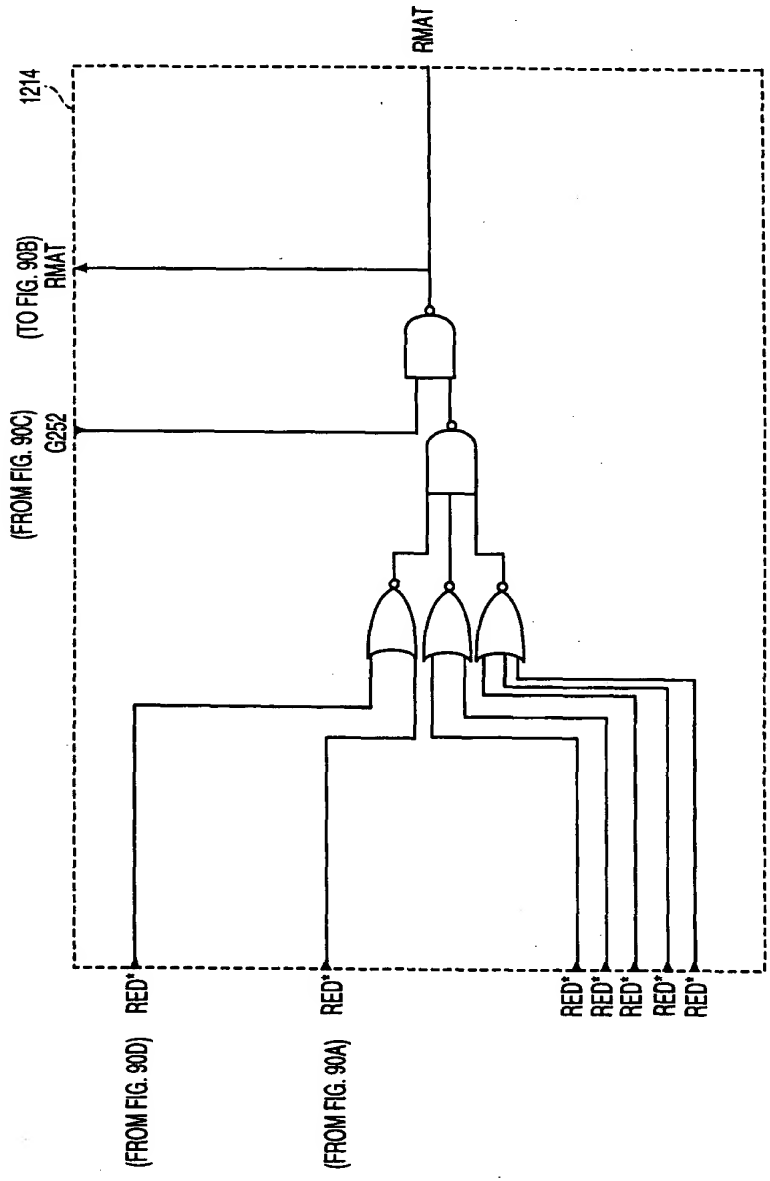

RMAT
1214
(TO FIG. 90B)
RMAT
(FROM FIG. 90C)
G252
(FROM FIG. 90D)
RED*
(FROM FIG. 90A)
RED*
RED*
RED*
RED*
RED*

FIG. 90E

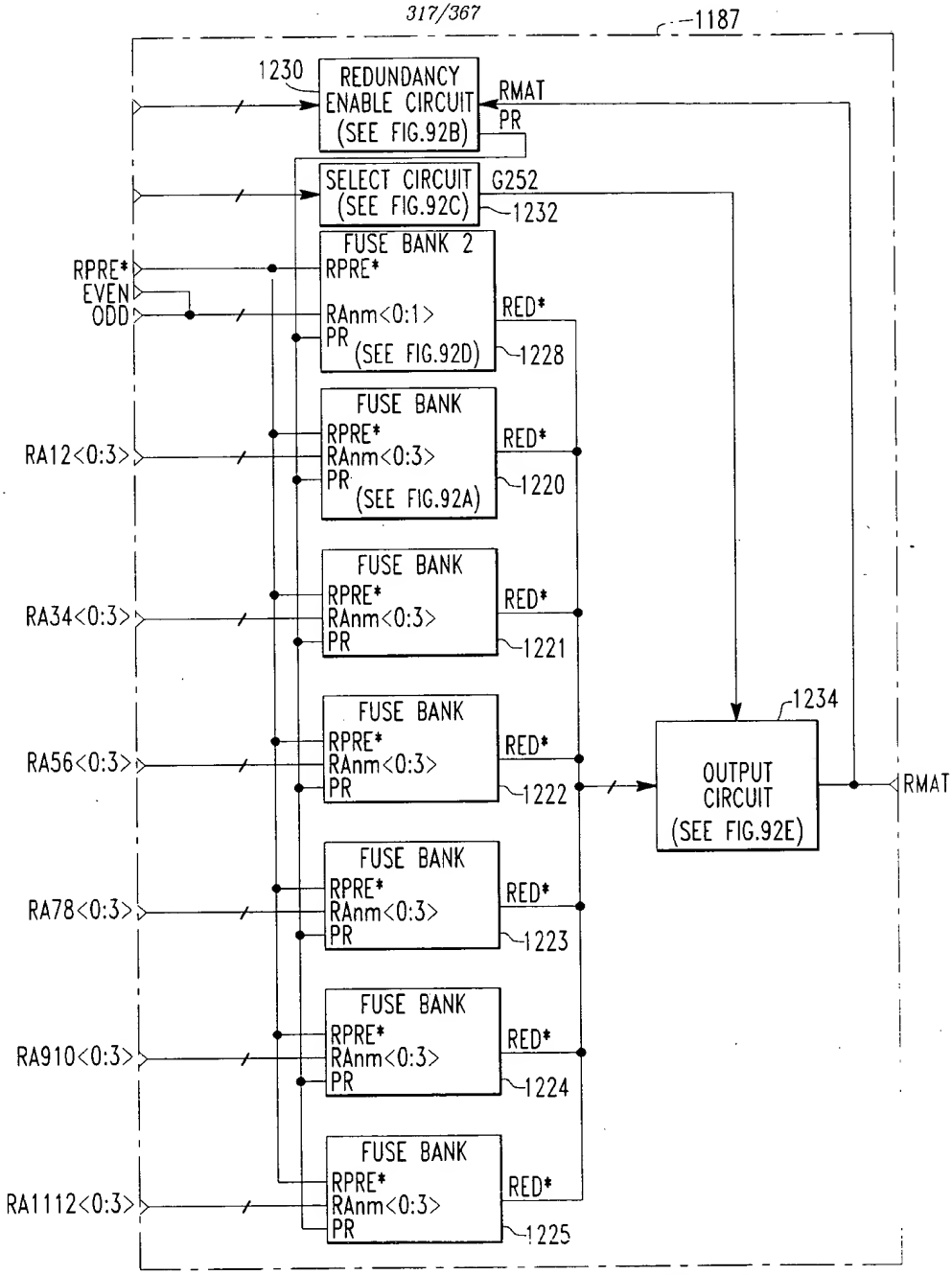


FIG. 91

09/08/2003, 3:30:01

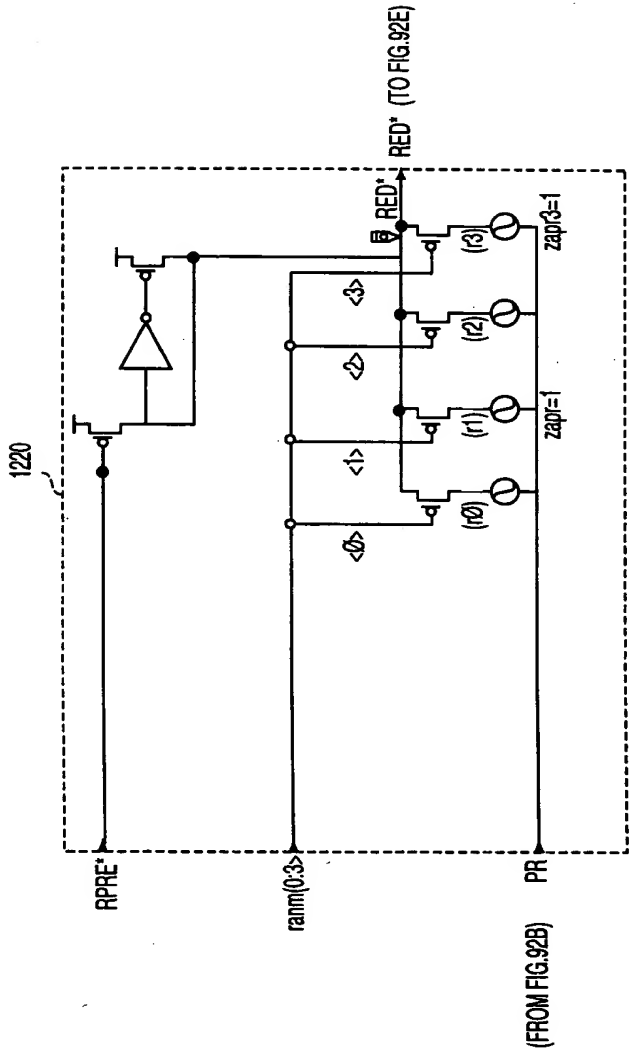

1220
RPRE*
ranm(0:3)
(FROM FIG.92B)
PR
RED*
RED* (TO FIG.92E)
<3>
<2>
<1>
<0>
(r3)
(r2)
(r1)
(r0)
zap<3>=1
zap<1>=1

FIG. 92A

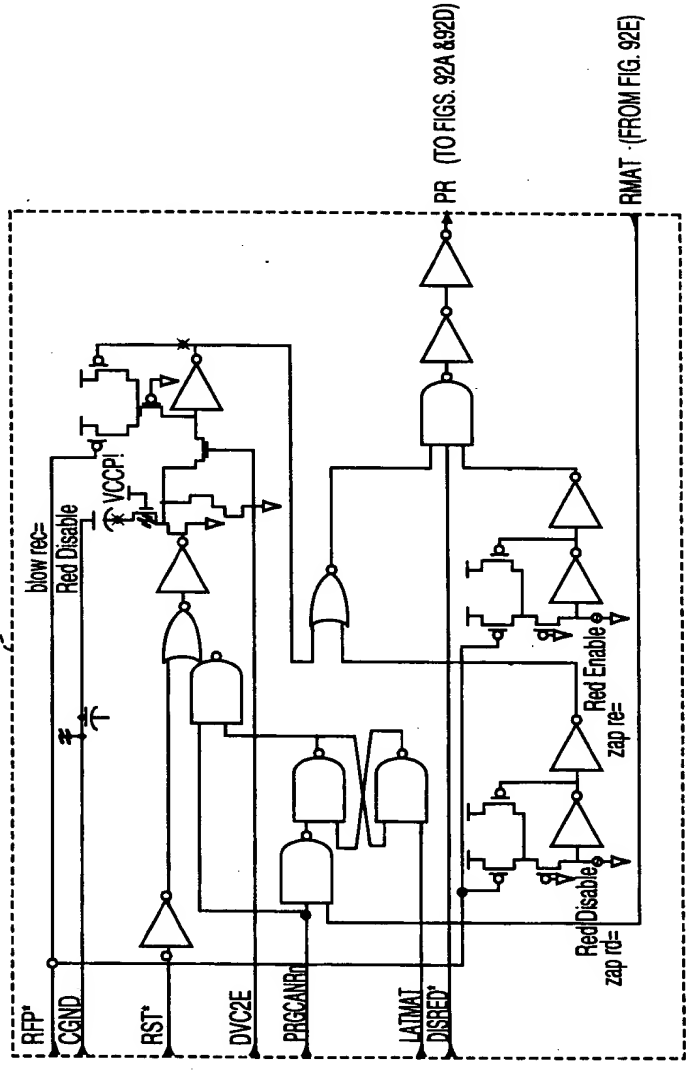

1230
RFP*
CGND
RST*
DVC2E
PRGCANRo
LATMAT
DISRED*
blow rec=
Red Disable
VCCP!
Red Enable
zap re=
Red Disable
zap rd=
PR (TO FIGS. 92A &92D)
RMAT (FROM FIG. 92E)

FIG. 92B

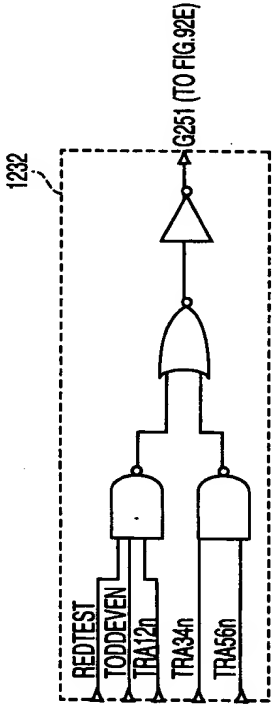


FIG. 92C

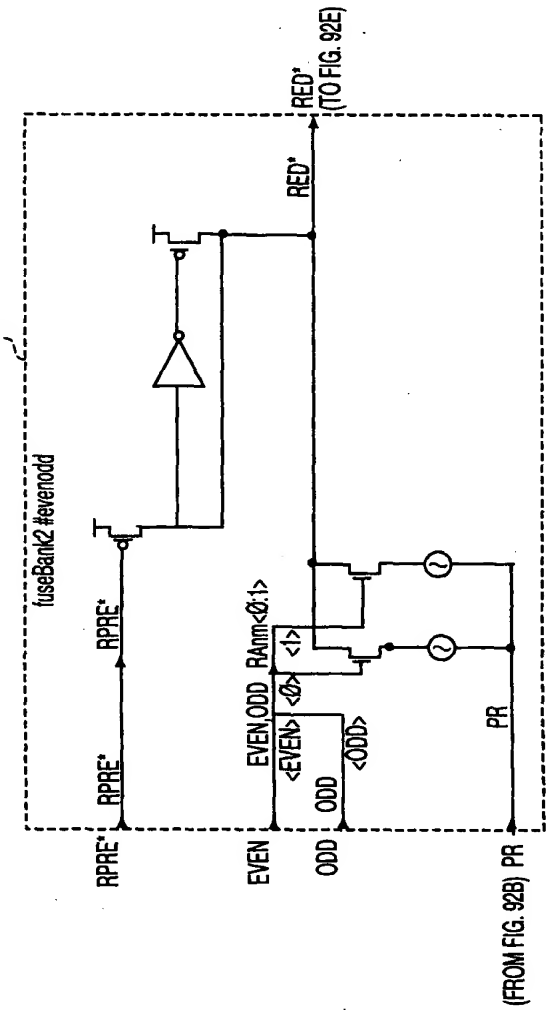

1228
fuseBank2 #evenodd
RPRE'
RPRE'
RPRE'
EVEN
ODD
EVEN ODD RAnm<0:1>
<EVEN>
<0>
<1>
<ODD>
ODD
PR
(FROM FIG. 92B) PR
RED'
RED'
(TO FIG. 92E)

FIG. 92D

TARGET 8370860

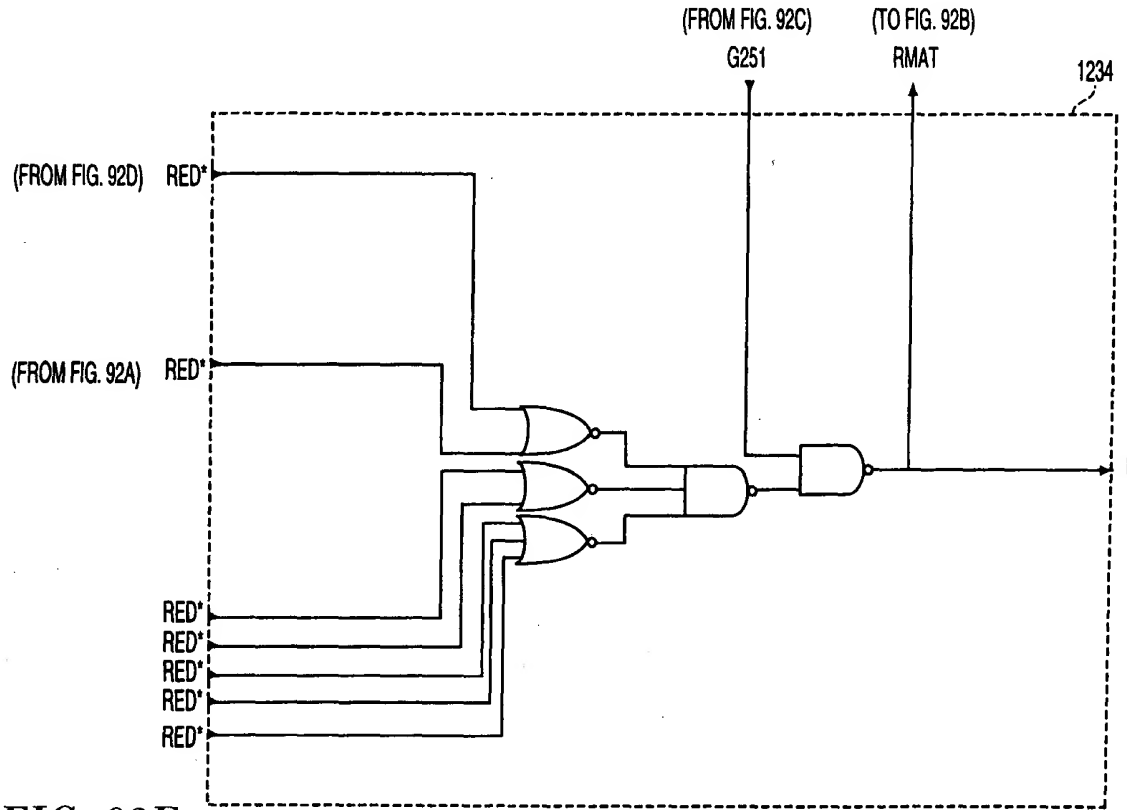


FIG. 92E

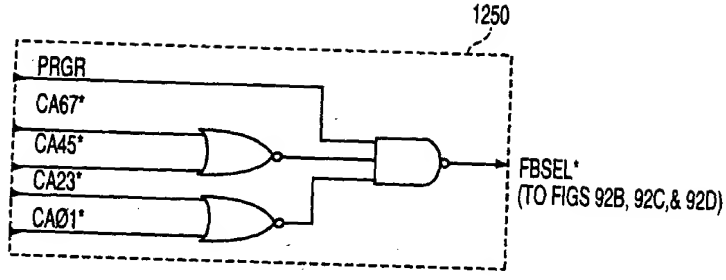


FIG. 93A

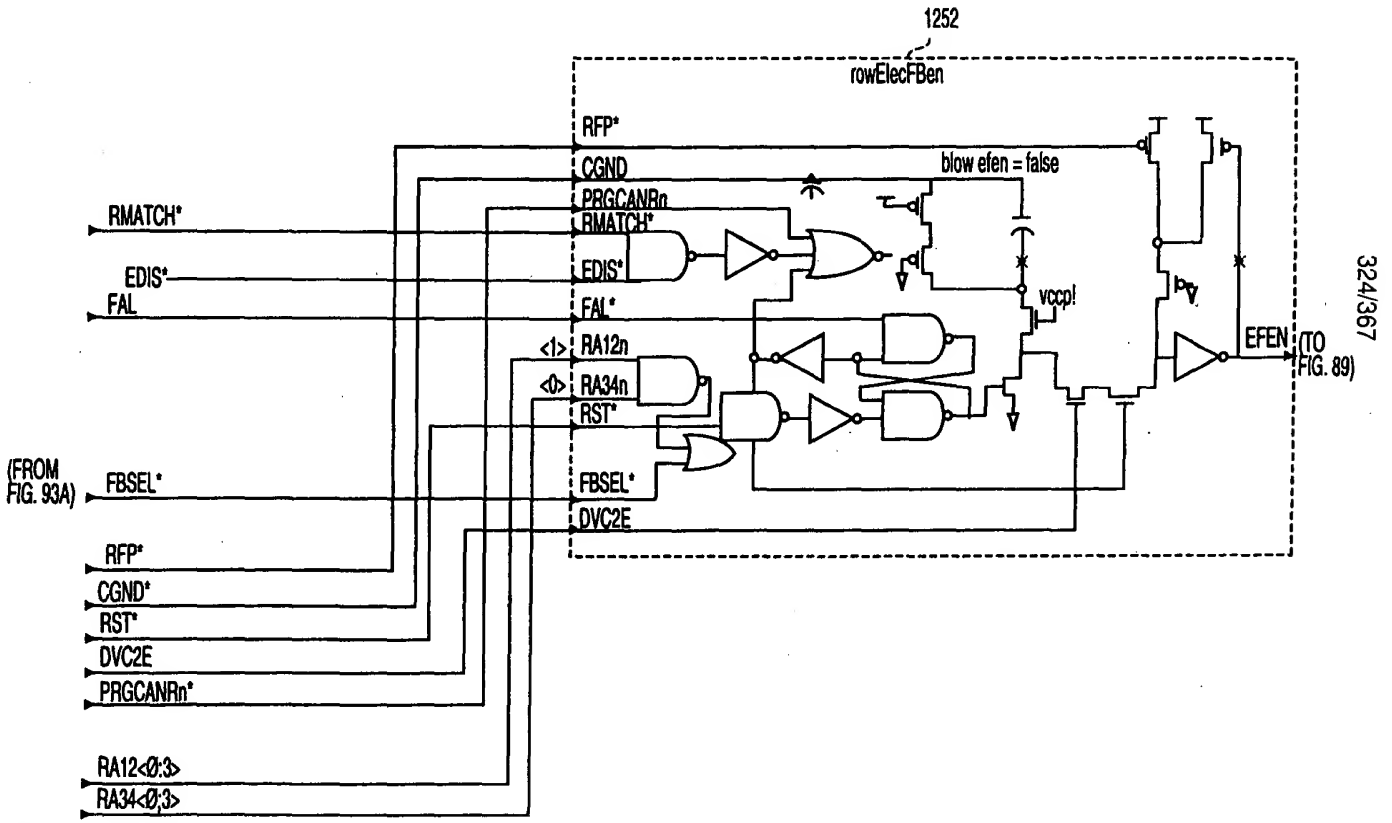

1252
rowElecFBen
RFP*
CGND
PRGCANRn
RMATCH*
EDIS*
FAL*
<1> RA12n
<0> RA34n
RST*
FBSEL*
DVC2E
blow efen = false
vccp!
EFEN
(TO FIG. 89)
RMATCH*
EDIS*
FAL
(FROM FIG. 93A)
FBSEL*
RFP*
CGND*
RST*
DVC2E
PRGCANRn*
RA12<0:3>
RA34<0:3>

FIG. 93B

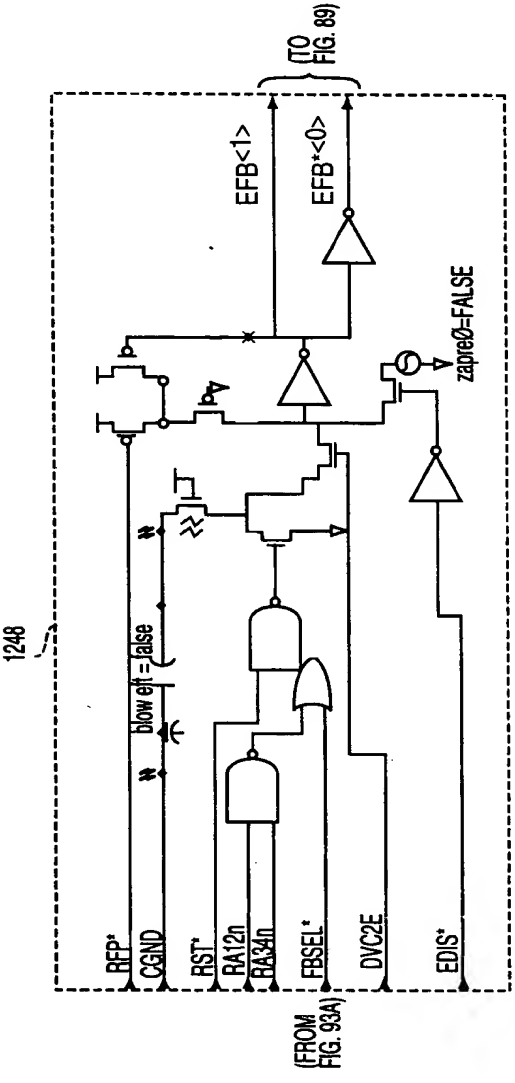

(TO FIG. 89)
EFB<1>
EFB*<0>
zapre0=FALSE
1248
blow eft=false
REP*
CGND
RST*
RA12n
RA34n
FBSEL*
DVC2E
EDIS*
(FROM FIG. 93A)

FIG. 93C

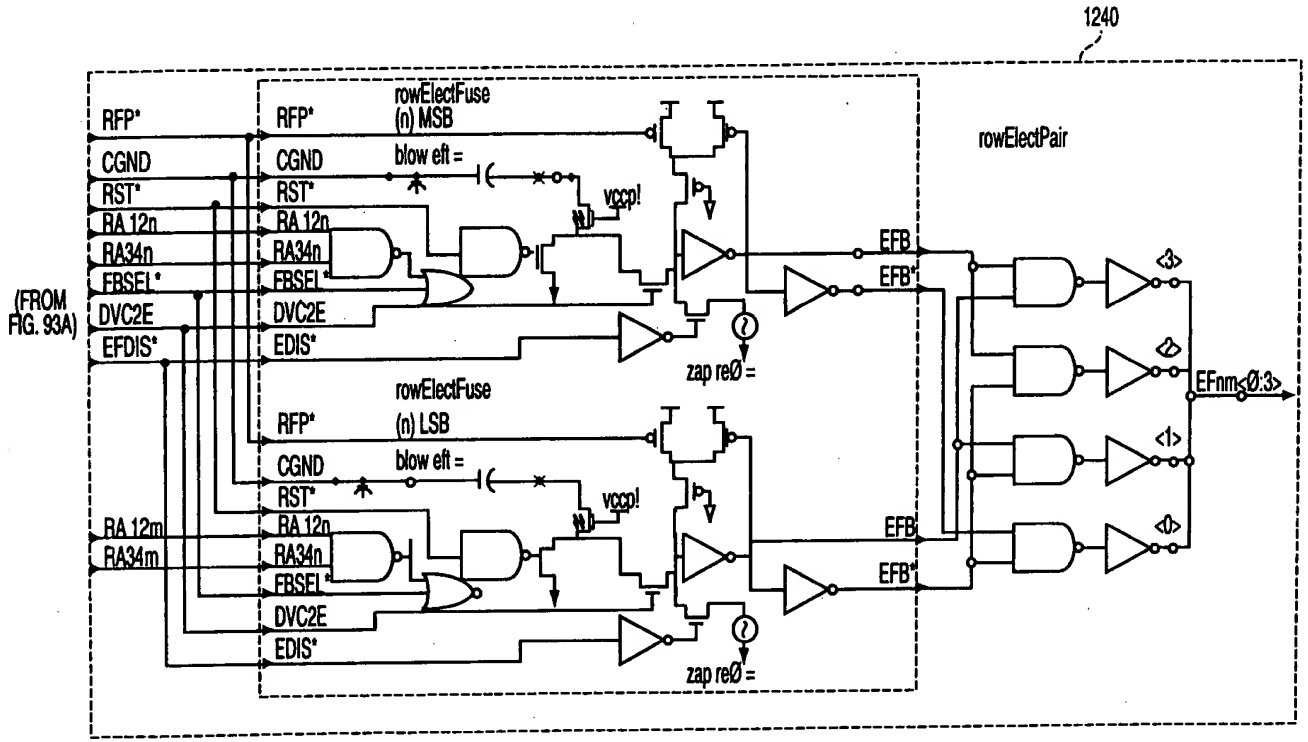

1240
rowElectFuse
(n) MSB
rowElectPair
RFP*
CGND
RST*
RA12n
RA34n
FBSEL*
DVC2E
EFDIS*
(FROM FIG. 93A)
blow eft =
vccp!
EFB
EFB*
zap reØ =
rowElectFuse
(n) LSB
RA12m
RA34m
EDIS*
<3>
<2>
<1>
<0>
EFnm<Ø:3>
(TO FIG. 89)

FIG. 93D

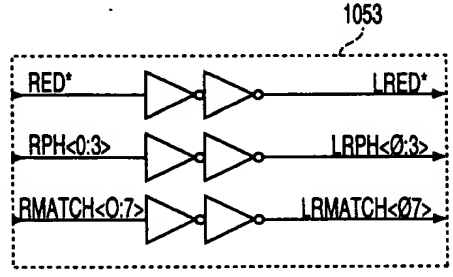


FIG. 94

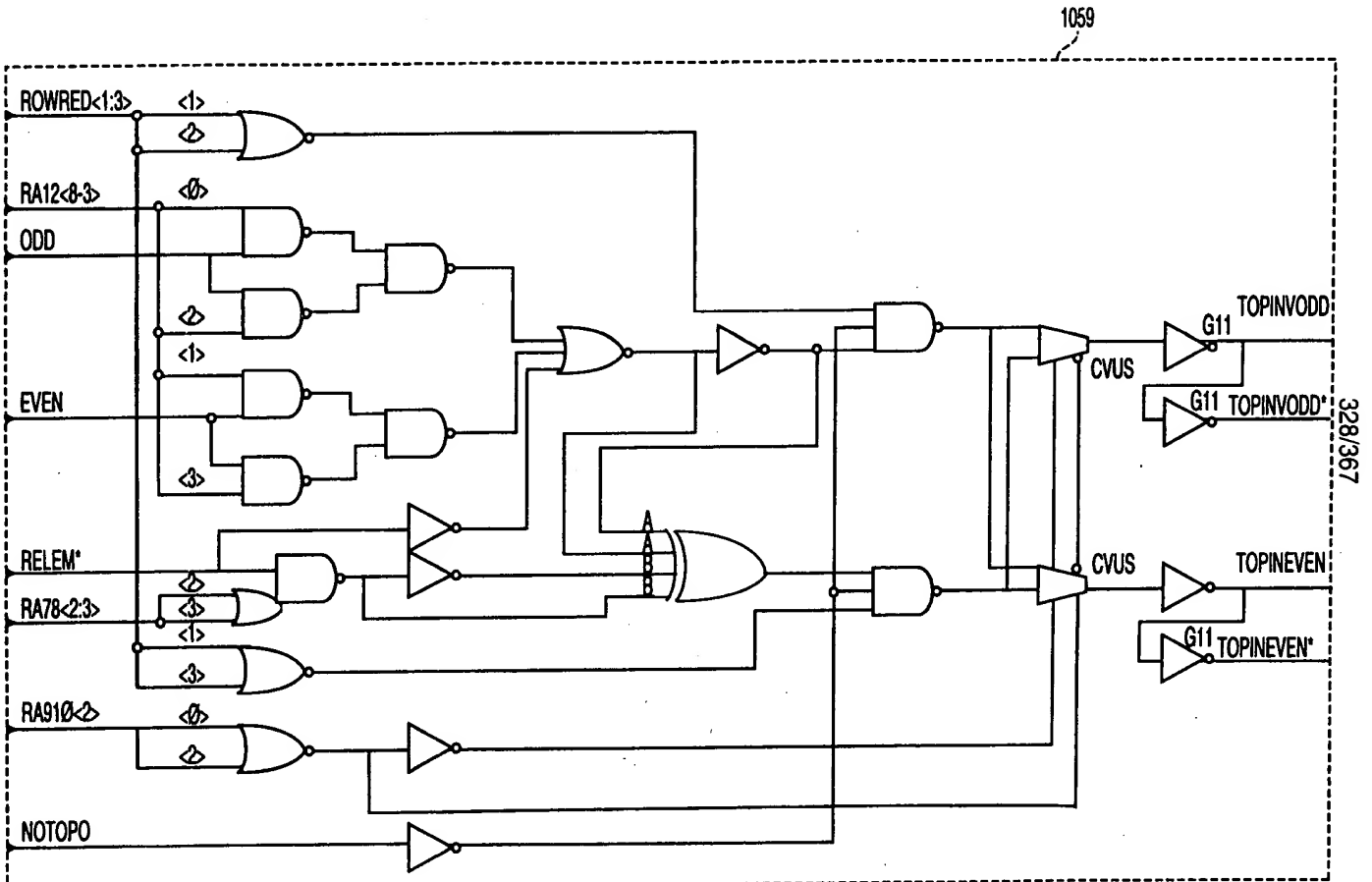

1059
ROWRED<1:3>
RA12<8-3>
ODD
EVEN
RELEM*
RA78<2:3>
RA91Ø<2>
NOTOPO
CVUS
CVUS
G11
G11
G11
TOPINVODD
TOPINVODD*
TOPINEVEN
TOPINEVEN*
328/367

FIG. 95

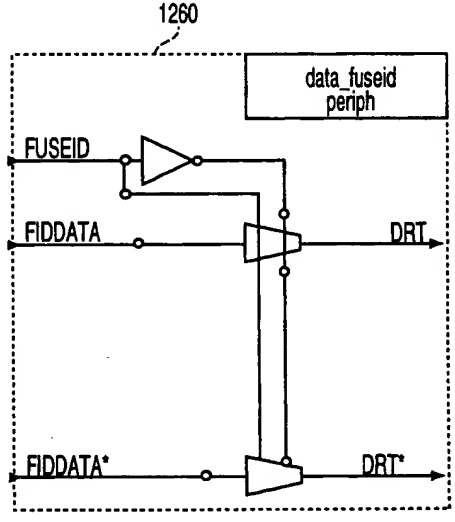


FIG. 96

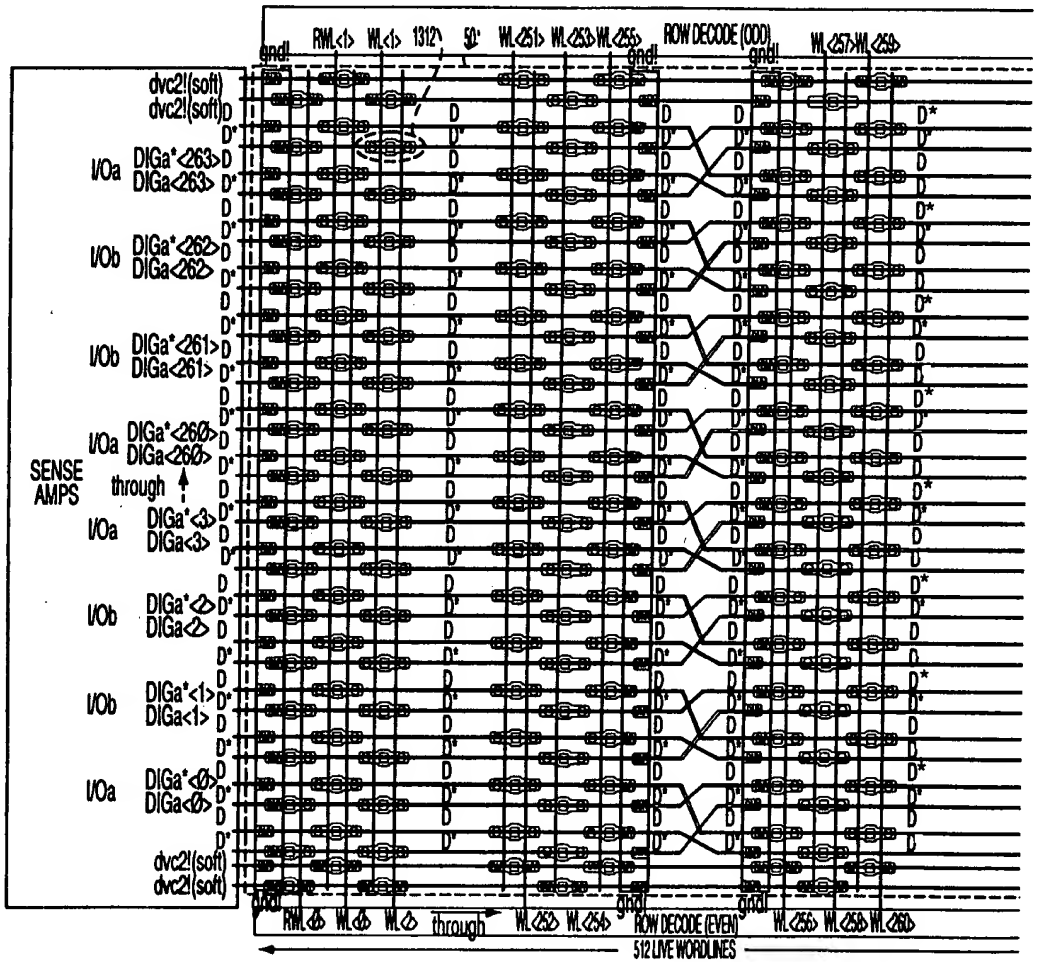


FIG. 97-1 | FIG. 97-2

FIG. 97-1

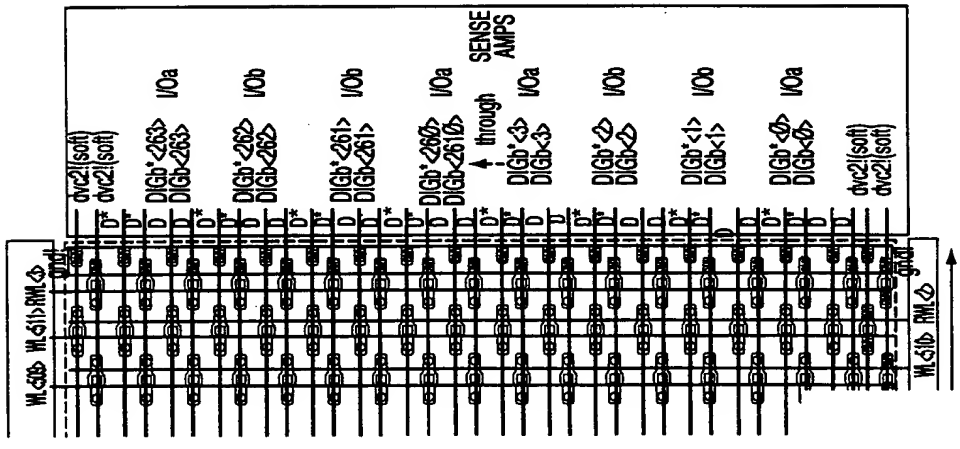


FIG. 97-1	FIG. 97-2

FIG. 97-2

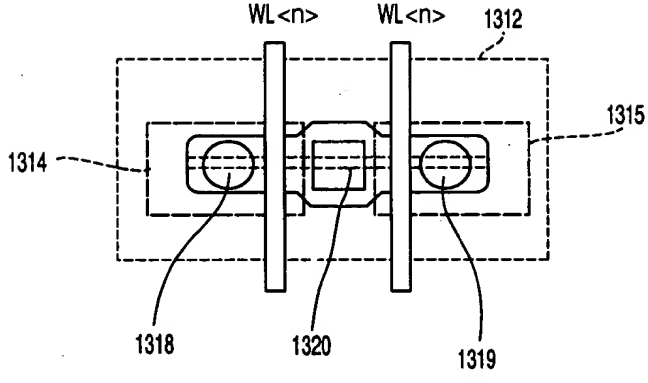


FIG. 98

US 2009/0168525 A1

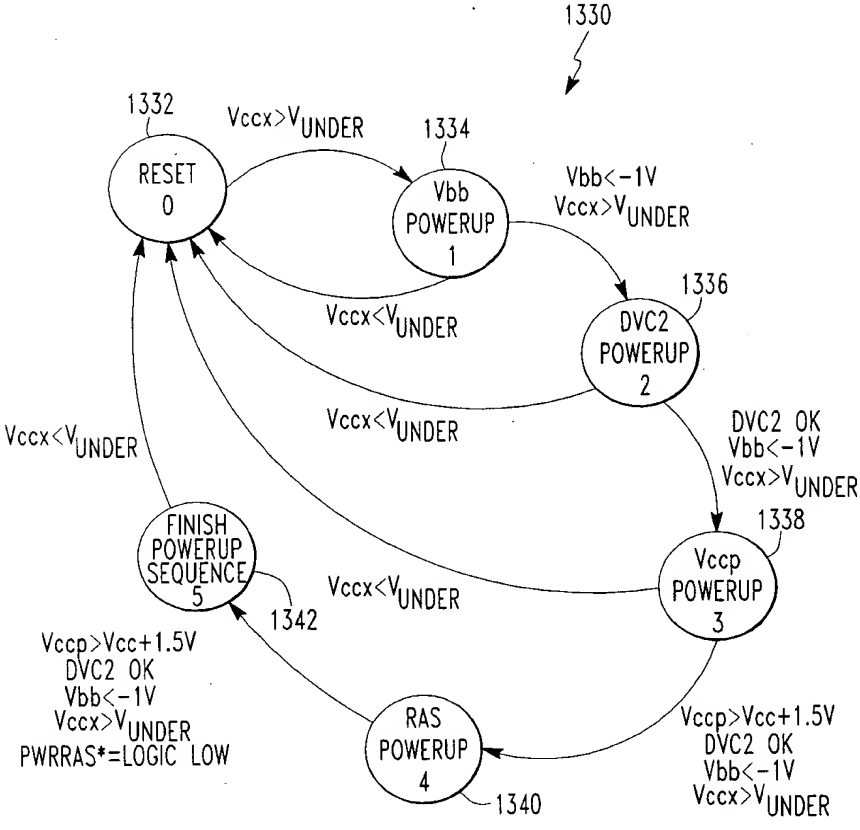

1330
1332
RESET
0
Vccx>V_UNDER
1334
Vbb
POWERUP
1
Vbb<-1V
Vccx>V_UNDER
Vccx<V_UNDER
1336
DVC2
POWERUP
2
Vccx<V_UNDER
Vccx<V_UNDER
DVC2 OK
Vbb<-1V
Vccx>V_UNDER
1338
Vccp
POWERUP
3
Vccx<V_UNDER
FINISH
POWERUP
SEQUENCE
5
1342
Vccp>Vcc+1.5V
DVC2 OK
Vbb<-1V
Vccx>V_UNDER
PWRRAS*=LOGIC LOW
RAS
POWERUP
4
1340
Vccp>Vcc+1.5V
DVC2 OK
Vbb<-1V
Vccx>V_UNDER

FIG. 99

Tobacco Settlement

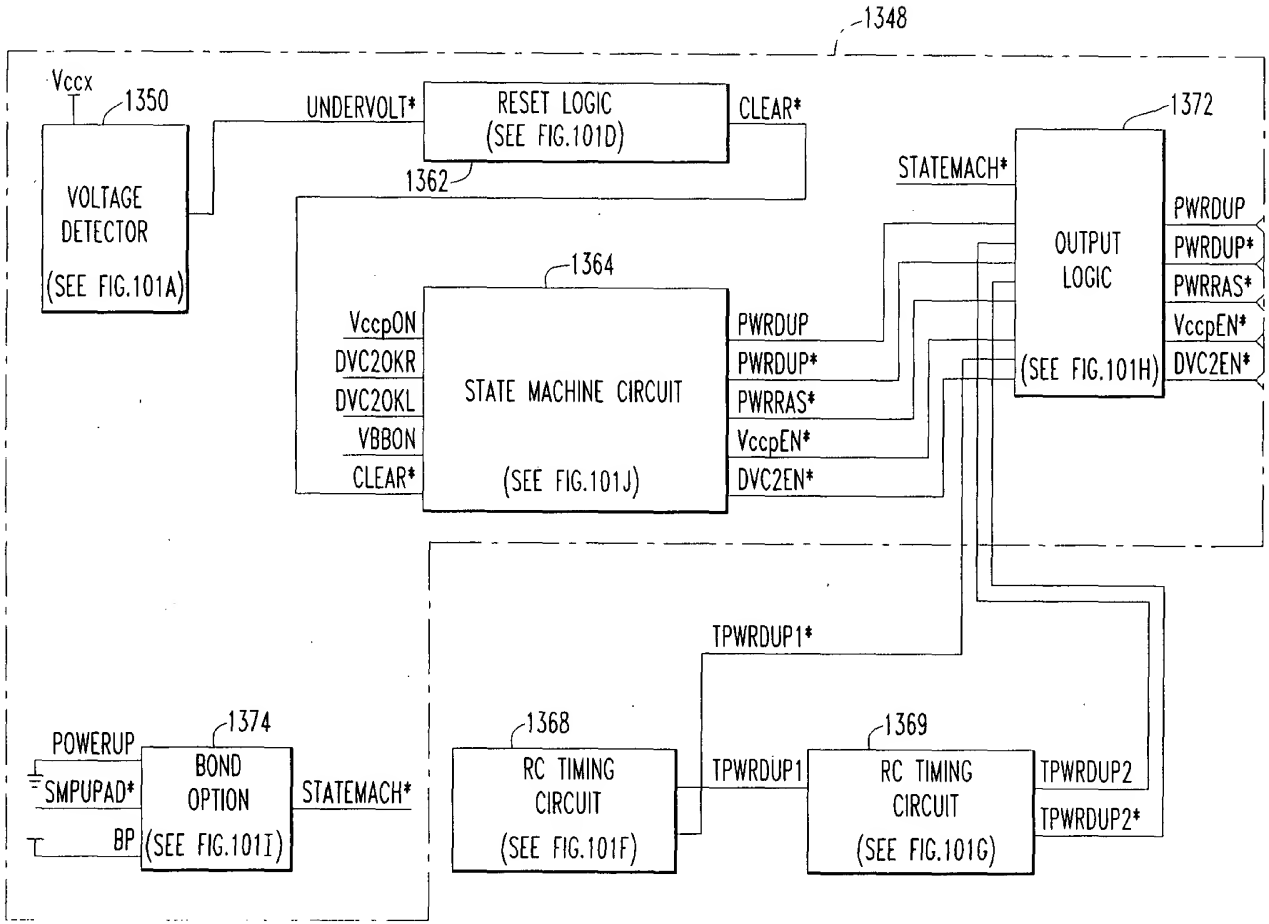


FIG.100

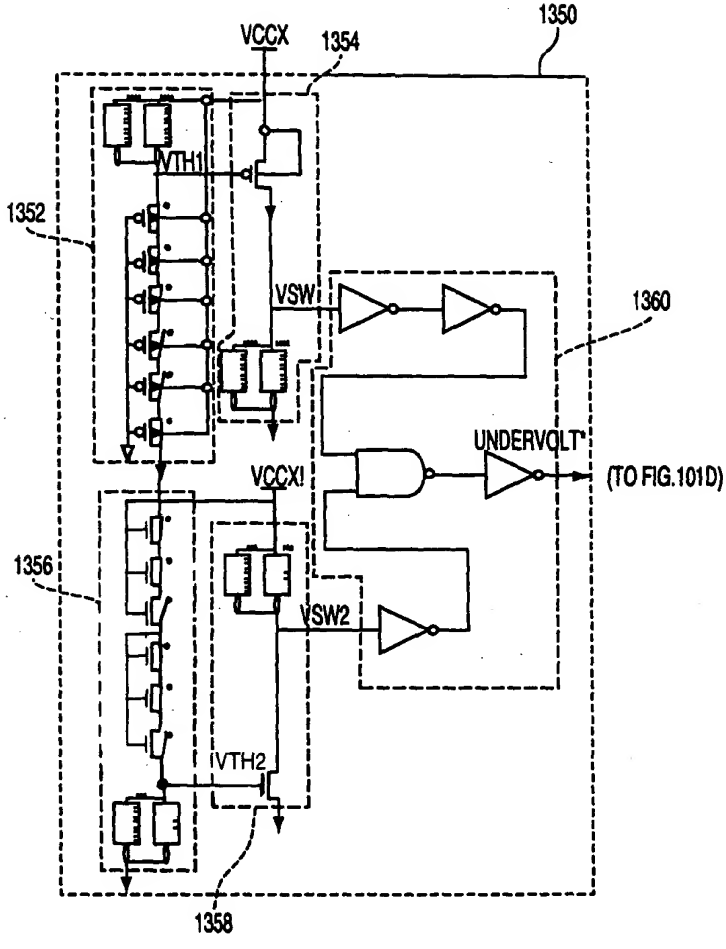

1350
VCCX
1354
VTH1
1352
VSW
1360
UNDERVOLT
(TO FIG.101D)
VCCXI
1356
VSW2
VTH2
1358

FIG. 101A

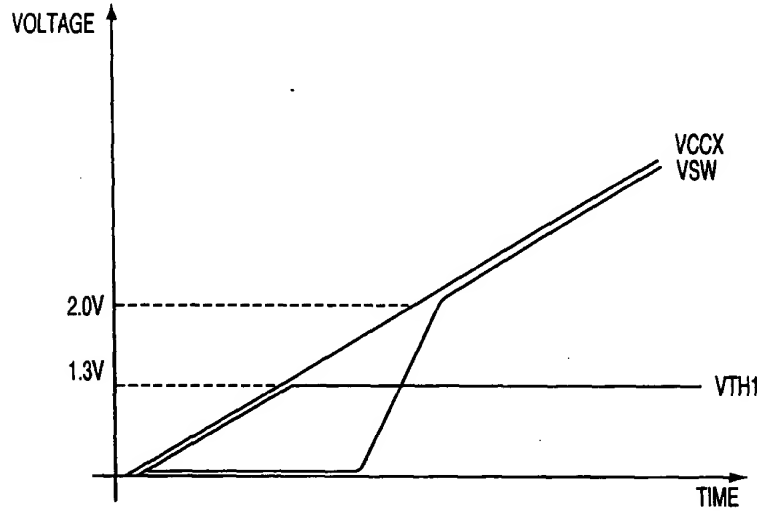


FIG. 101B

EP 3 503 369 A1 2019-06-26

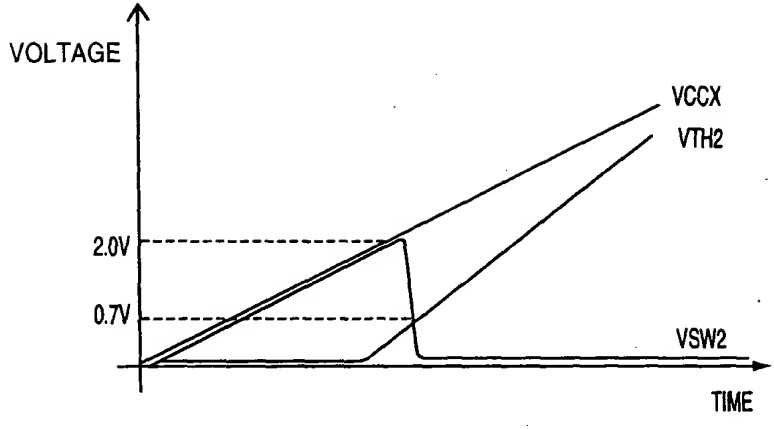


FIG. 101C

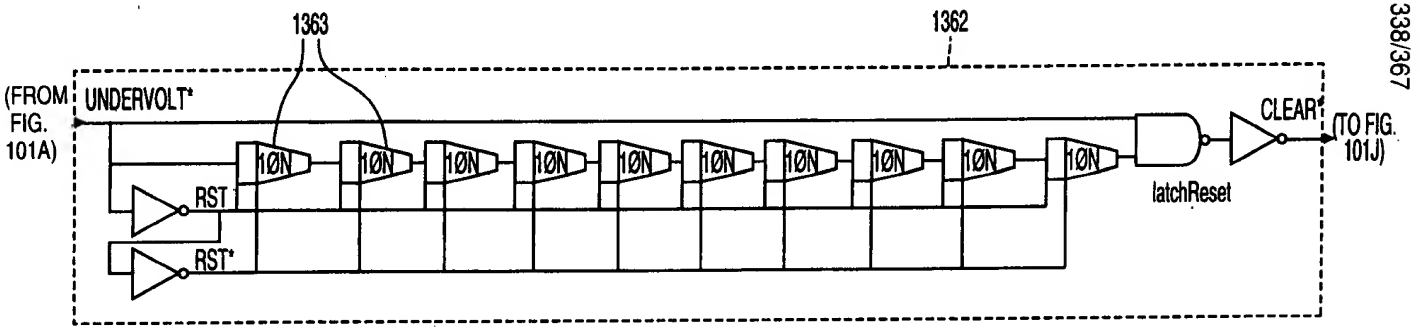

1363
1362
(FROM FIG. 101A)
UNDERVOLT*
1ØN
RST
RST*
latchReset
CLEAR*
(TO FIG. 101J)

FIG. 101D

Translated Submitted

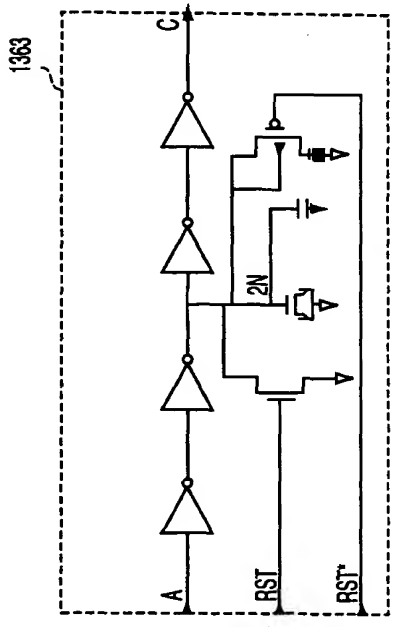


FIG. 101E

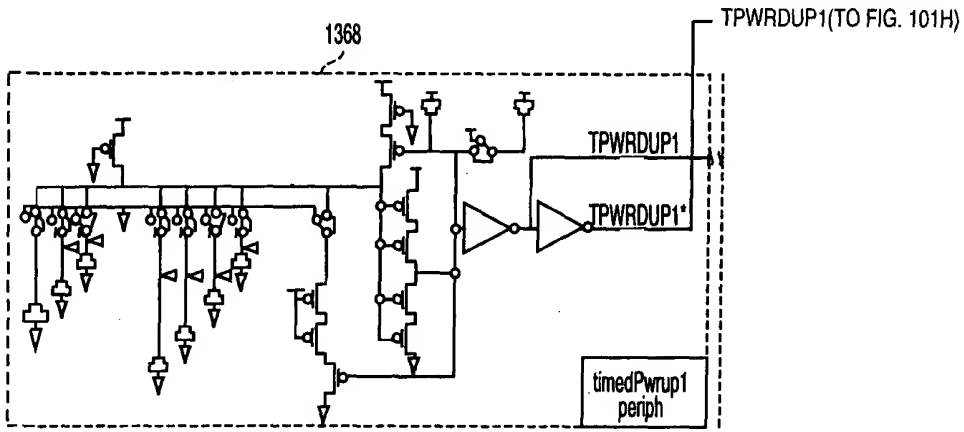

1368
TPWRDUP1(TO FIG. 101H)
TPWRDUP1
TPWRDUP1*
timedPwrup1
periph

FIG. 101F

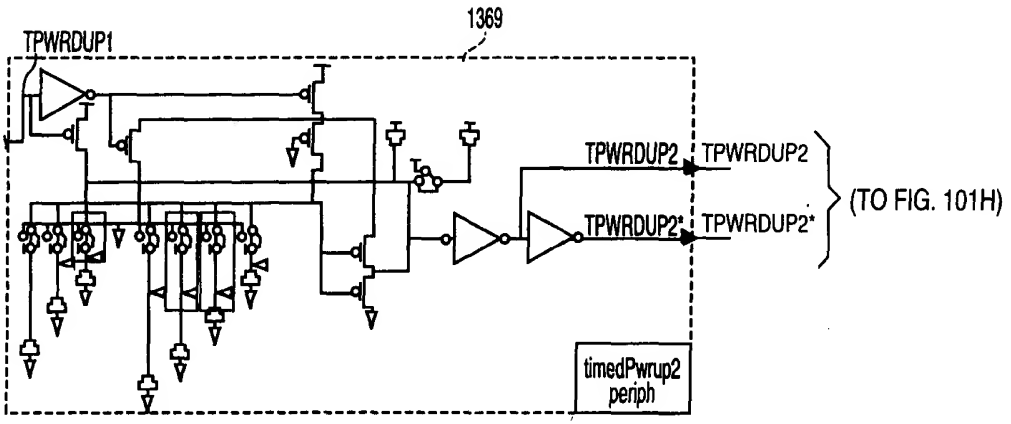

1369
TPWRDUP1
TPWRDUP2
TPWRDUP2
TPWRDUP2*
TPWRDUP2*
(TO FIG. 101H)
timedPwrup2
periph

FIG. 101G

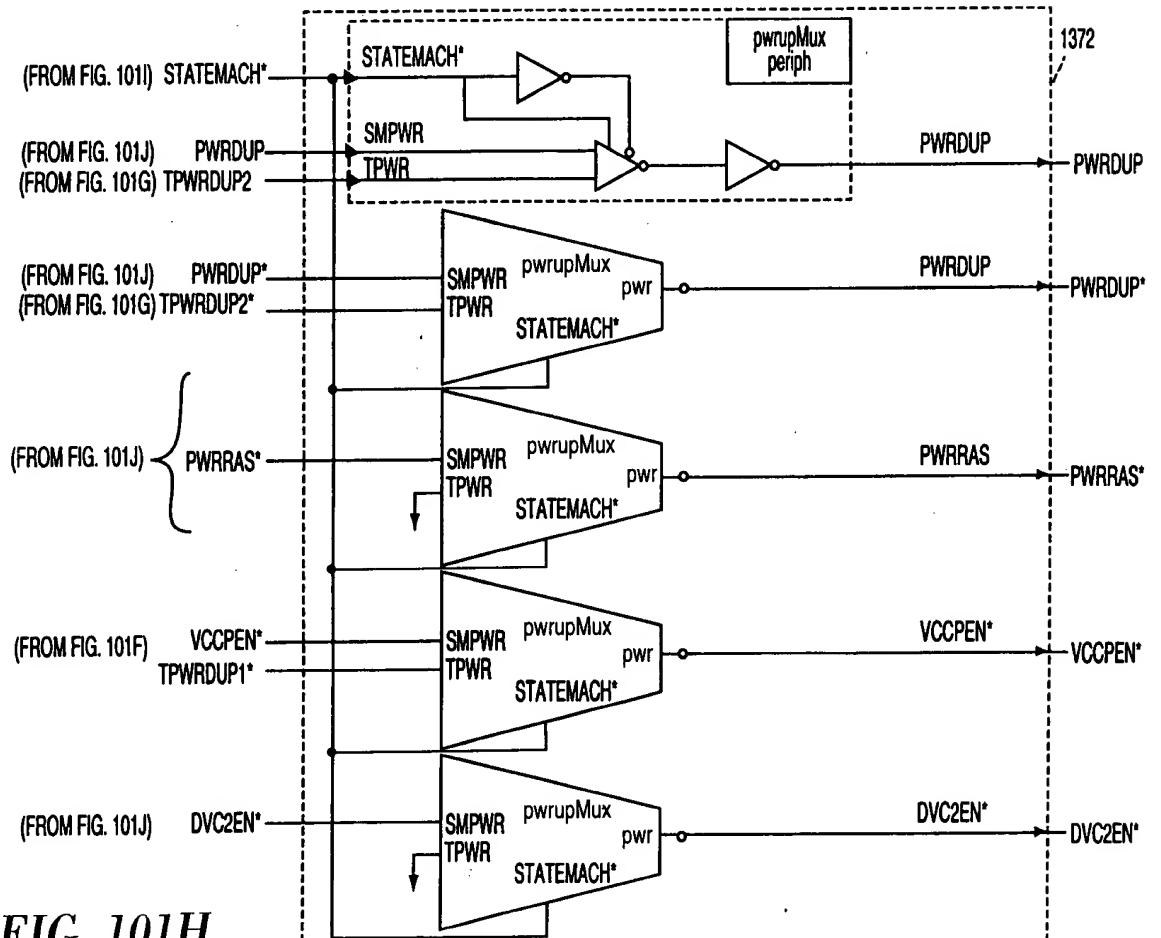

(FROM FIG. 101I) STATEMACH*
(FROM FIG. 101J) PWRDUP
(FROM FIG. 101G) TPWRDUP2
STATEMACH*
SMPWR
TPWR
pwrupMux periph
PWRDUP
PWRDUP
1372
(FROM FIG. 101J) PWRDUP*
(FROM FIG. 101G) TPWRDUP2*
SMPWR
TPWR
pwrupMux
pwr
STATEMACH*
PWRDUP
PWRDUP*
(FROM FIG. 101J) PWRRAS*
SMPWR
TPWR
pwrupMux
pwr
STATEMACH*
PWRRAS
PWRRAS*
(FROM FIG. 101F) VCCPEN*
TPWRDUP1*
SMPWR
TPWR
pwrupMux
pwr
STATEMACH*
VCCPEN*
VCCPEN*
(FROM FIG. 101J) DVC2EN*
SMPWR
TPWR
pwrupMux
pwr
STATEMACH*
DVC2EN*
DVC2EN*

FIG. 101H

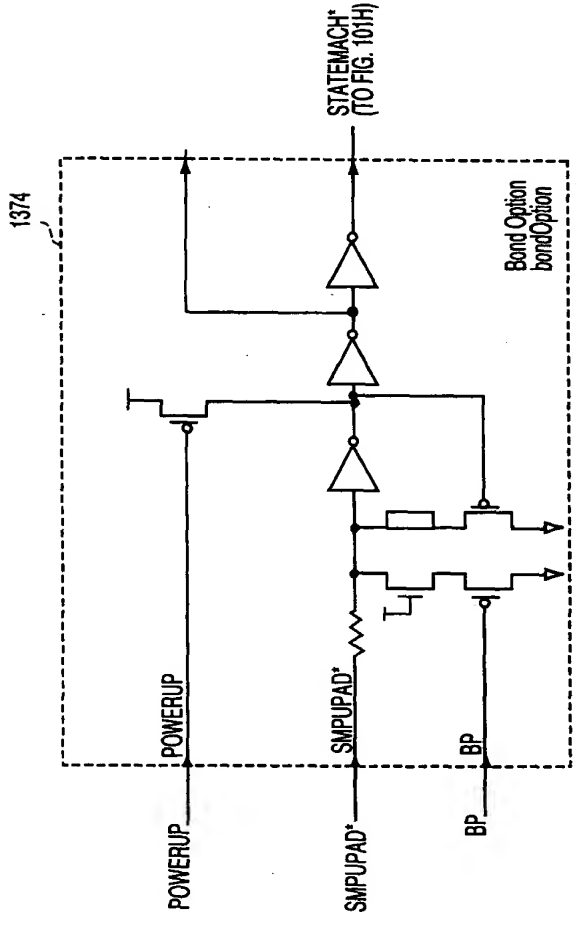

1374
STATEMACH*
(TO FIG. 101H)
Bond Option
bondOption
POWERUP
SMPUPAD*
BP
POWERUP
SMPUPAD*
BP

FIG. 1011

Tosoco 02570660

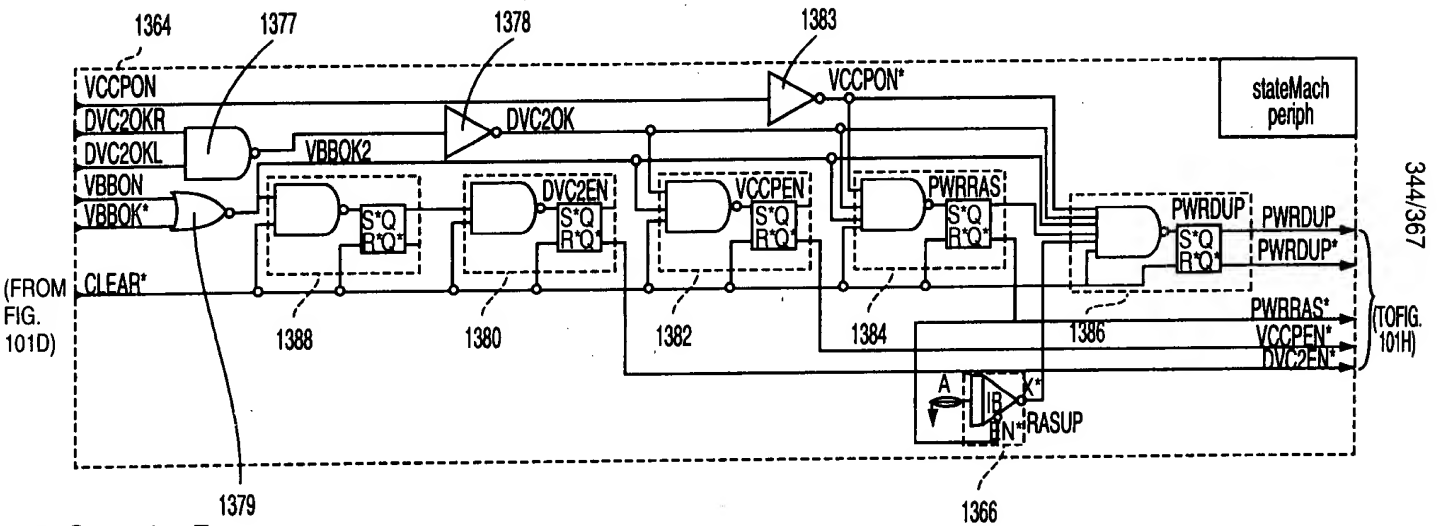


FIG. 101J

TOSHIBA 325360

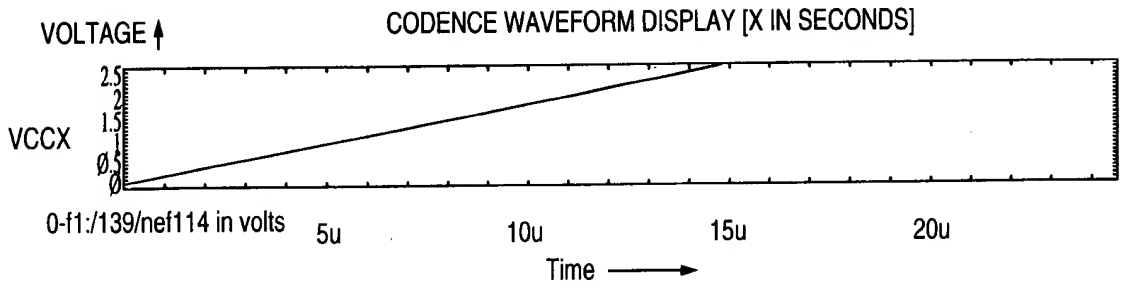


FIG. 102A

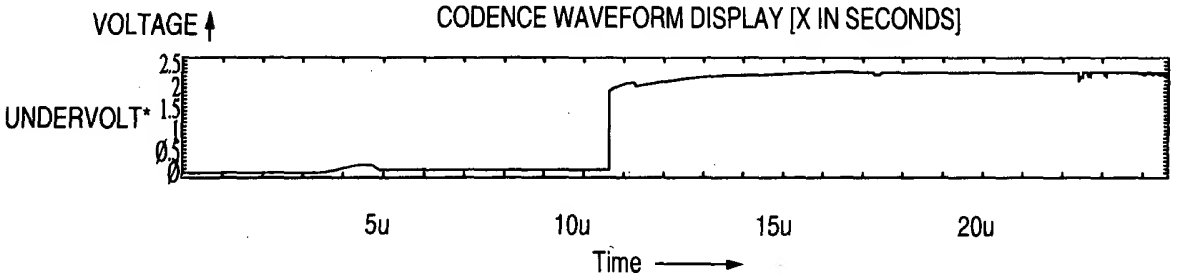

VOLTAGE
CODENCE WAVEFORM DISPLAY [X IN SECONDS]
UNDERVOLT*
2.5
2
1.5
Ø.5
Ø
5u
10u
15u
20u
Time
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102B

TOSHIBA 257A960

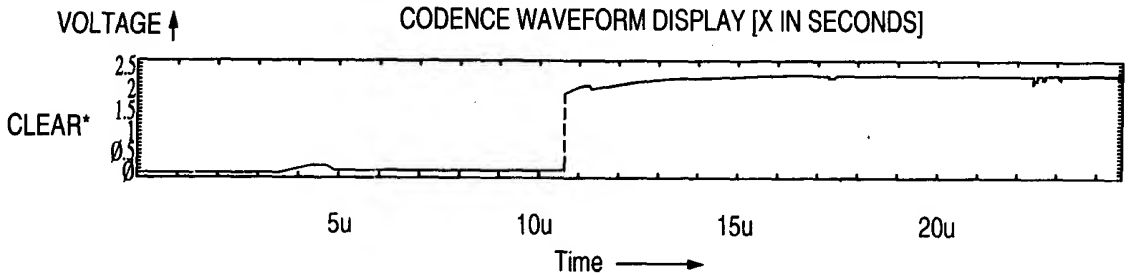


FIG. 102C

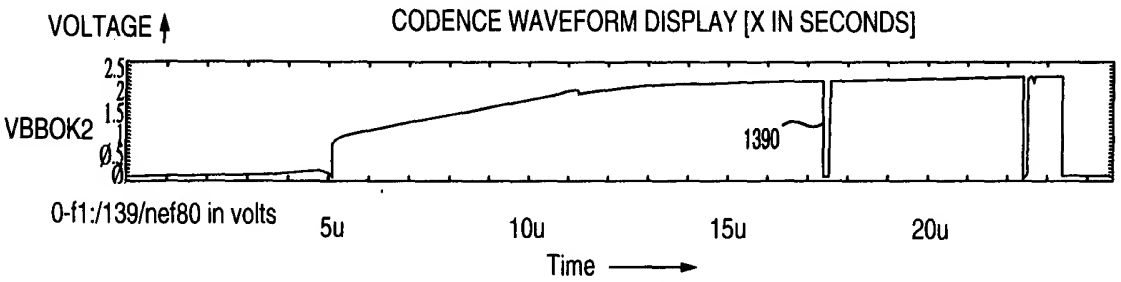
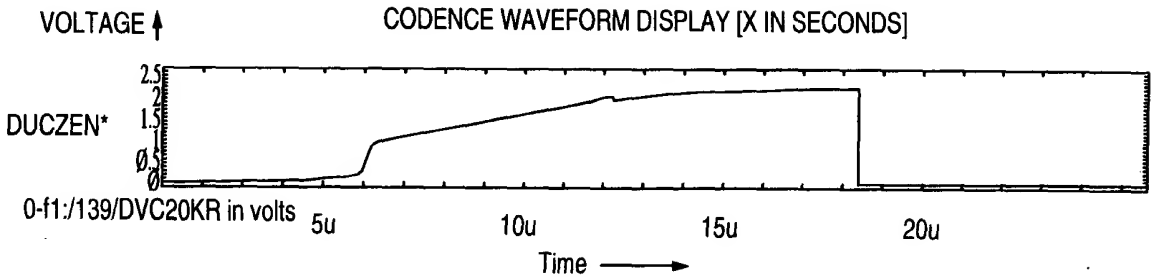

VOLTAGE
CODENCE WAVEFORM DISPLAY [X IN SECONDS]
VBBOK2
2.5
2
1.5
1
Ø.5
Ø
1390
0-f1:/139/nef80 in volts
5u
10u
15u
20u
Time
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102D

Tosoco 6297860



NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102E

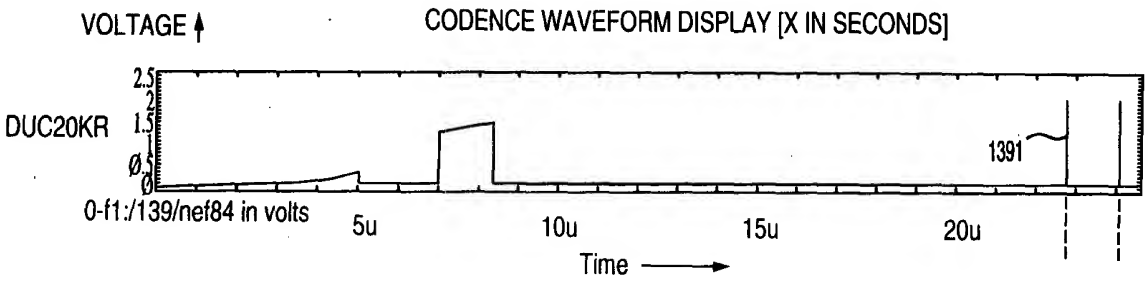

VOLTAGE
CODENCE WAVEFORM DISPLAY [X IN SECONDS]
DUC20KR
2.5
2
1.5
1
0.5
0
1391
0-f1:/139/nef84 in volts
5u
10u
15u
20u
Time
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102F

T08020 "8970860

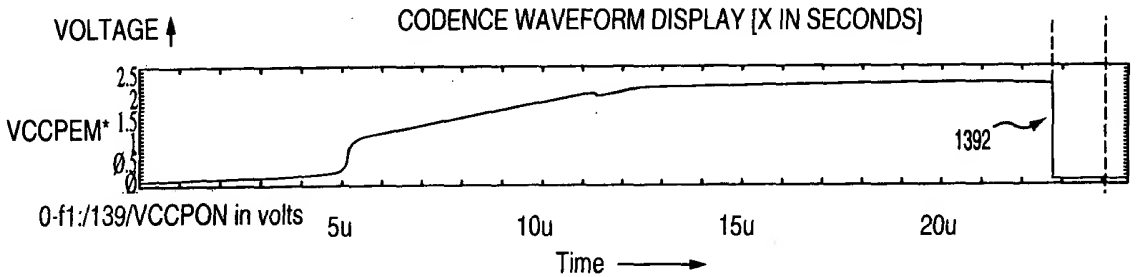


FIG. 102G

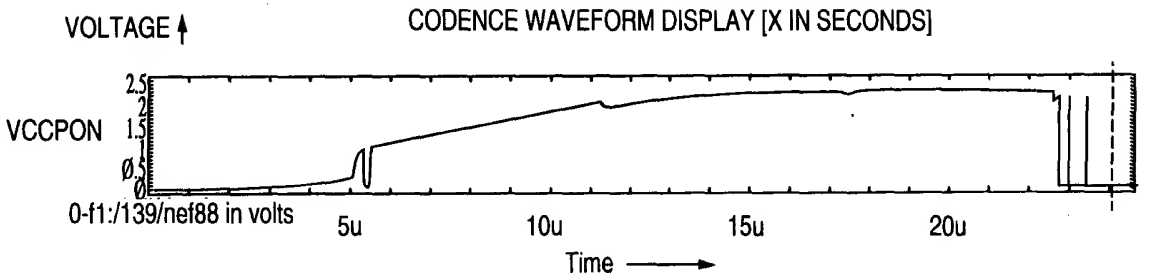

VOLTAGE
CODENCE WAVEFORM DISPLAY [X IN SECONDS]
VCCPON
2.5
2
1.5
1
0.5
0
0-f1:/139/nef88 in volts
5u
10u
15u
20u
Time
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102H

T0802D" 02570860

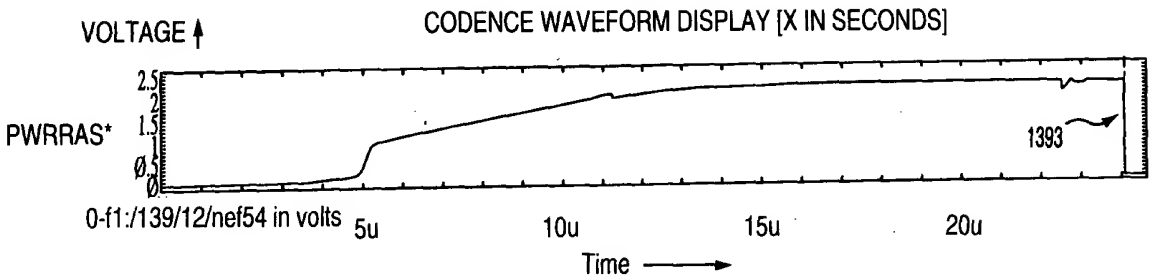


FIG. 102I

TOSHIBA 0297060

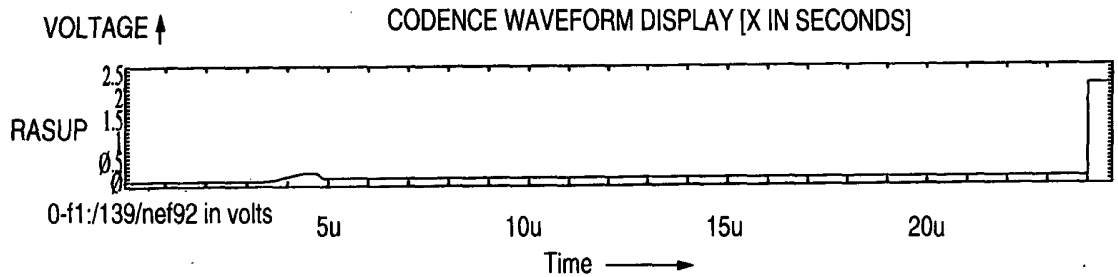
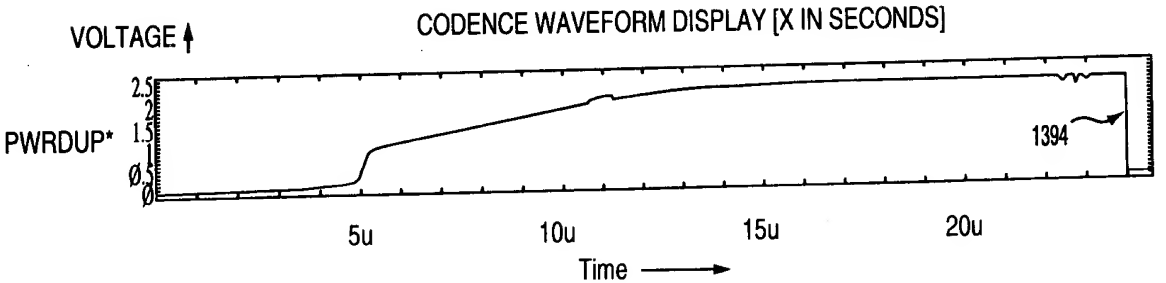


FIG. 102J



NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102K

T08020 8370860

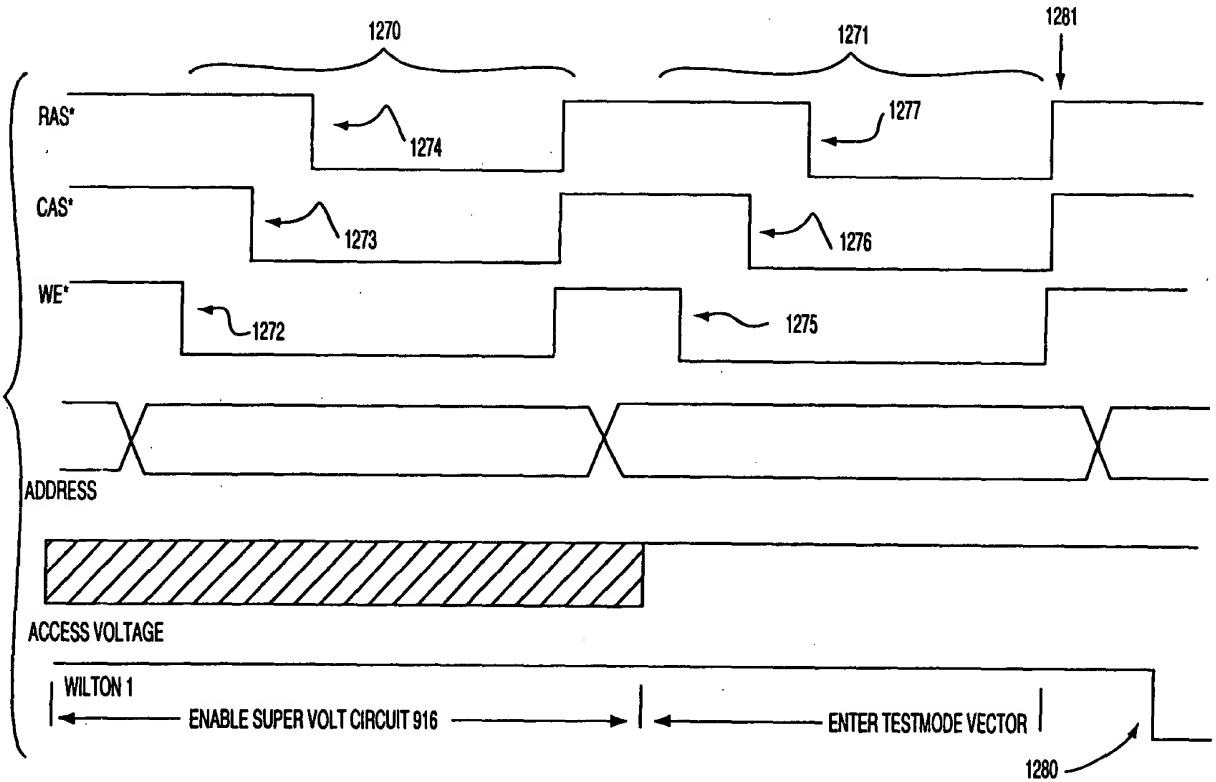


FIG. 103

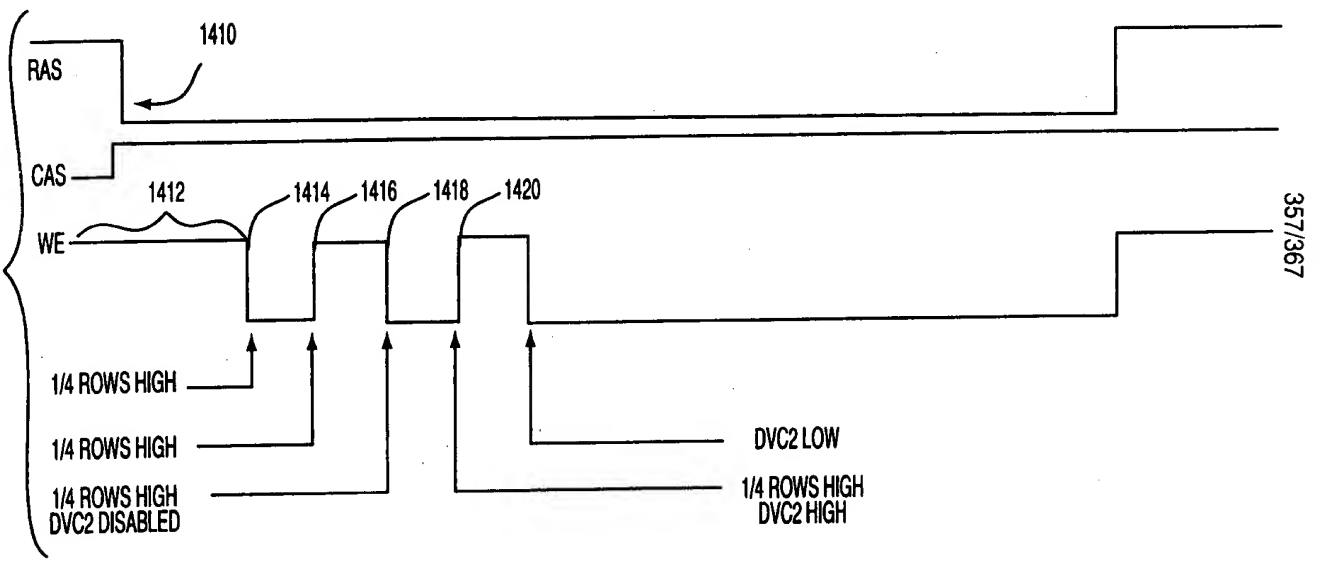

1410
RAS
CAS
1412
1414
1416
1418
1420
WE
357/367
1/4 ROWS HIGH
1/4 ROWS HIGH
1/4 ROWS HIGH
DVC2 DISABLED
DVC2 LOW
1/4 ROWS HIGH
DVC2 HIGH

FIG. 104

FOGGED BY SYSTRAN

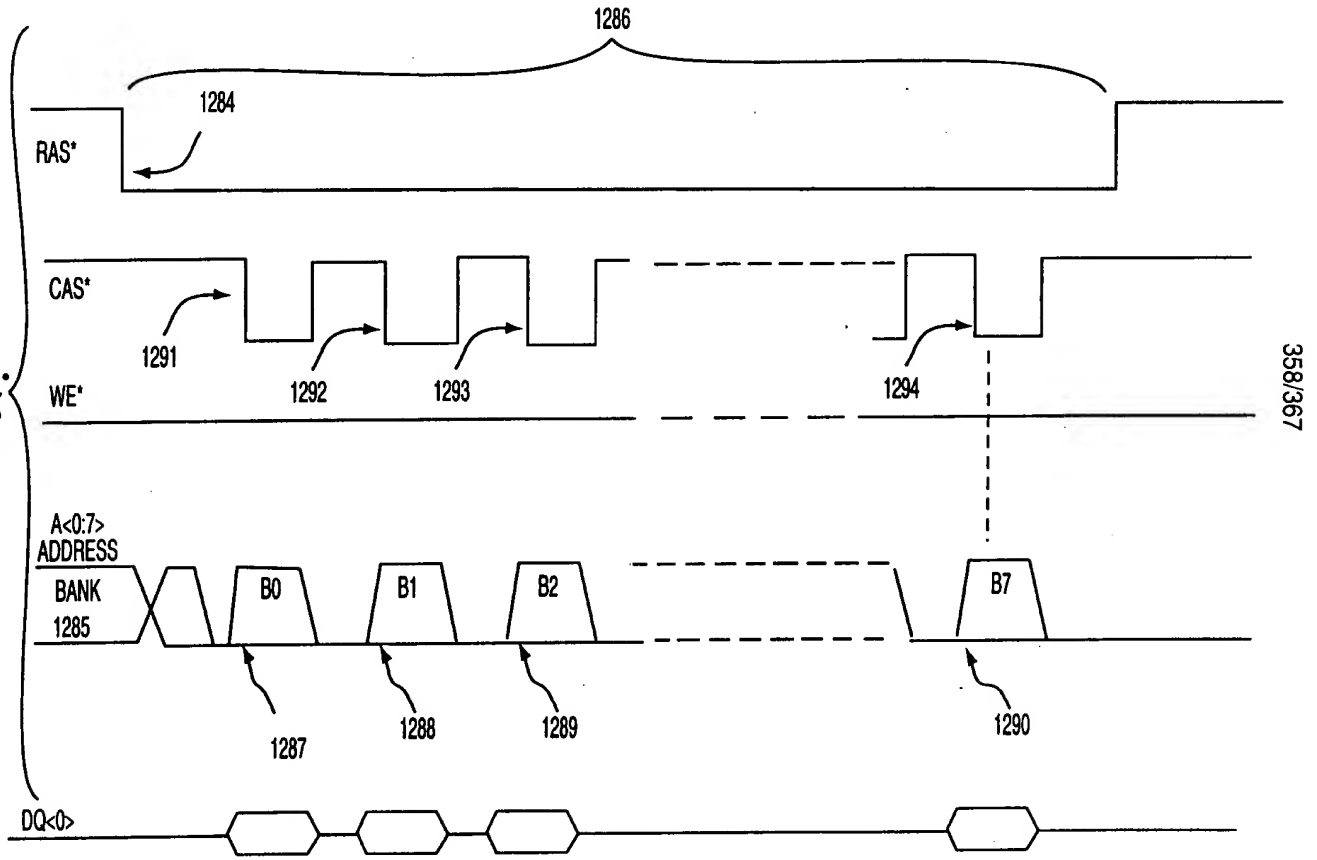


FIG. 105

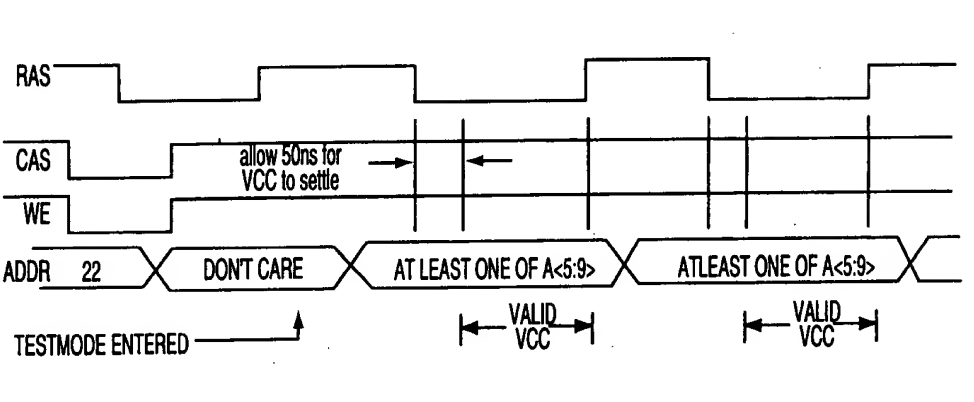
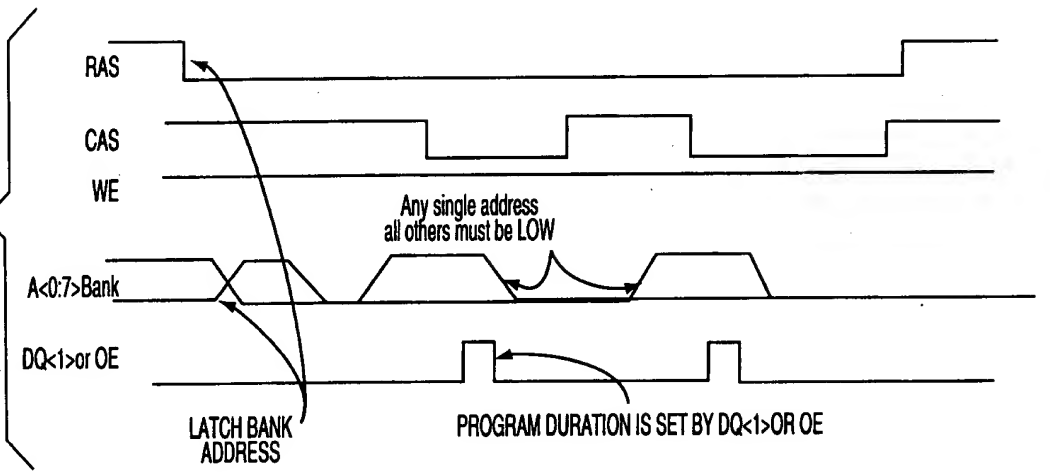

RAS
CAS
WE
ADDR
22
DON'T CARE
AT LEAST ONE OF A<5:9>
ATLEAST ONE OF A<5:9>
allow 50ns for
VCC to settle
TESTMODE ENTERED
VALID
VCC
VALID
VCC

FIG. 106

FORCED 0237 0860

FIG. 107



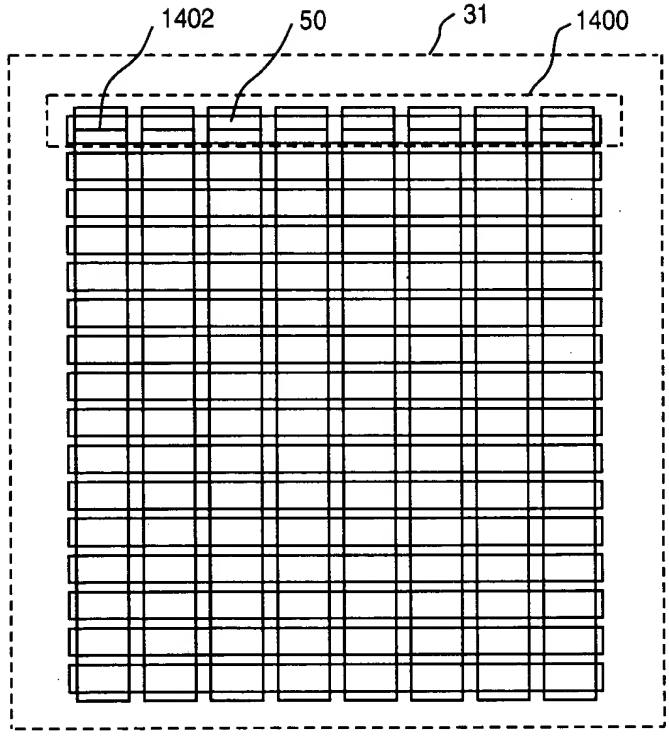


FIG. 108

FIG. 109-1

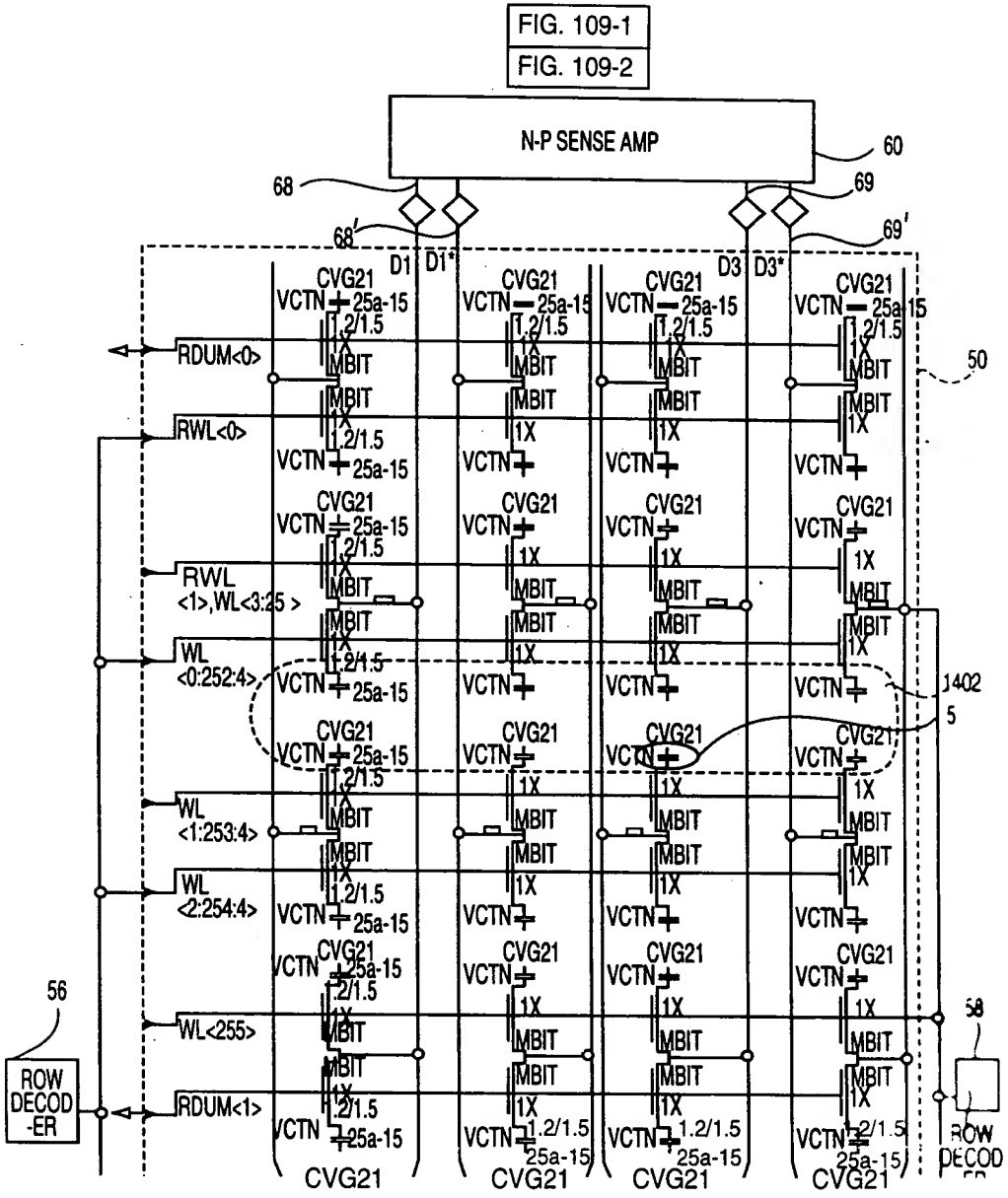


FIG. 109-1
FIG. 109-2
N-P SENSE AMP
60
68
68'
69
69'
D1
D1*
D3
D3*
CVG21
VCTN
25a-15
1.2/1.5
1X
MBIT
RDUM<0>
RWL<0>
RWL <1>,WL<3:25 >
WL <0:252:4>
WL <1:253:4>
WL <2:254:4>
WL<255>
RDUM<1>
50
1402
5
56
ROW DECOD -ER
58
ROW DECOD

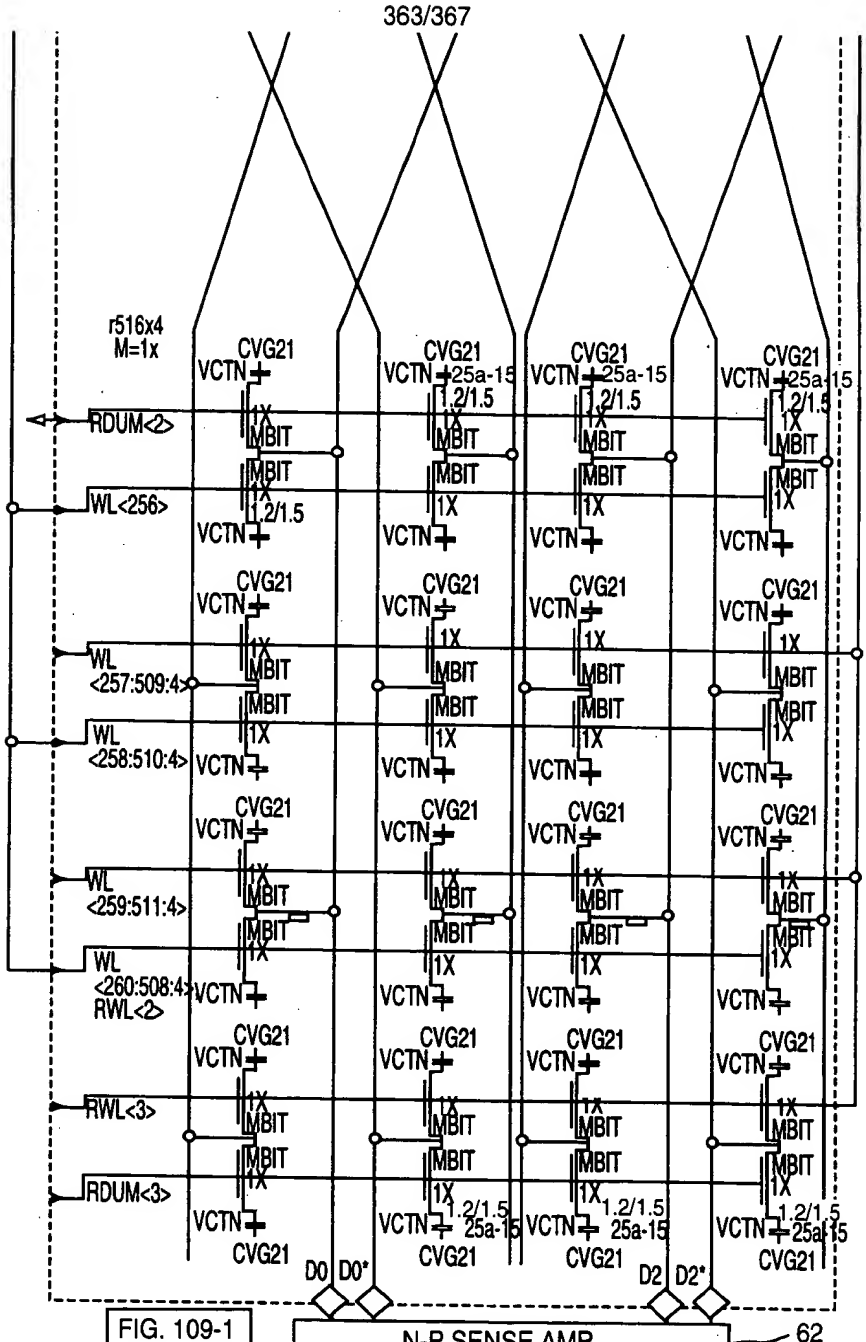


FIG. 109-1
FIG. 109-2

FIG. 109-2

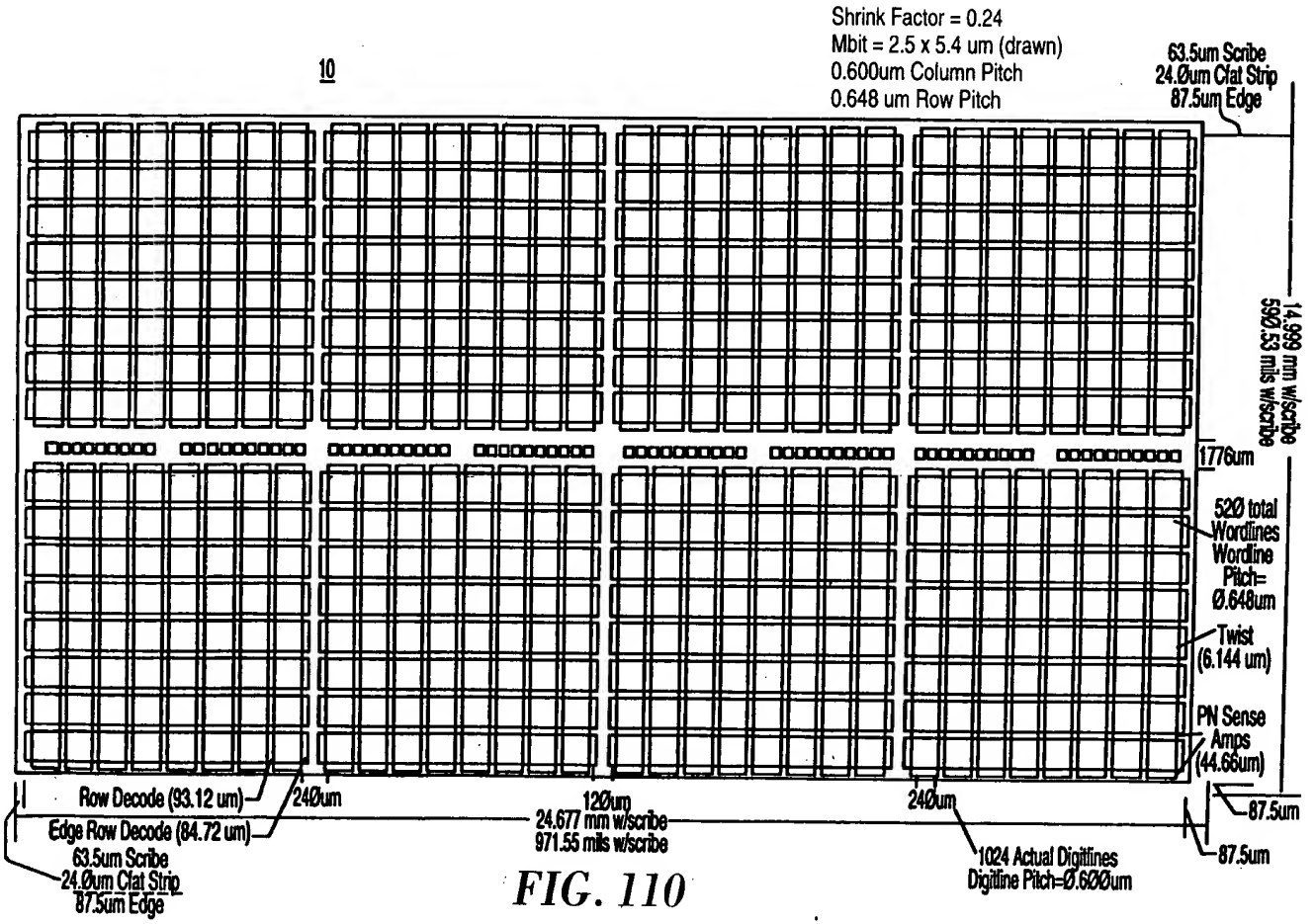

10
Shrink Factor = 0.24
Mbit = 2.5 x 5.4 um (drawn)
0.600um Column Pitch
0.648 um Row Pitch
63.5um Scribe
24.Øum Cfat Strip
87.5um Edge
14.999 mm w/scribe
590.53 mils w/scribe
1776um
52Ø total Wordlines
Wordline Pitch= Ø.648um
Twist (6.144 um)
PN Sense Amps (44.66um)
Row Decode (93.12 um)
Edge Row Decode (84.72 um)
63.5um Scribe
24.Øum Cfat Strip
87.5um Edge
24Øum
12Øum
24.677 mm w/scribe
971.55 mils w/scribe
24Øum
1024 Actual Digitlines
Digitline Pitch=Ø.6ØØum
87.5um
87.5um

FIG. 110

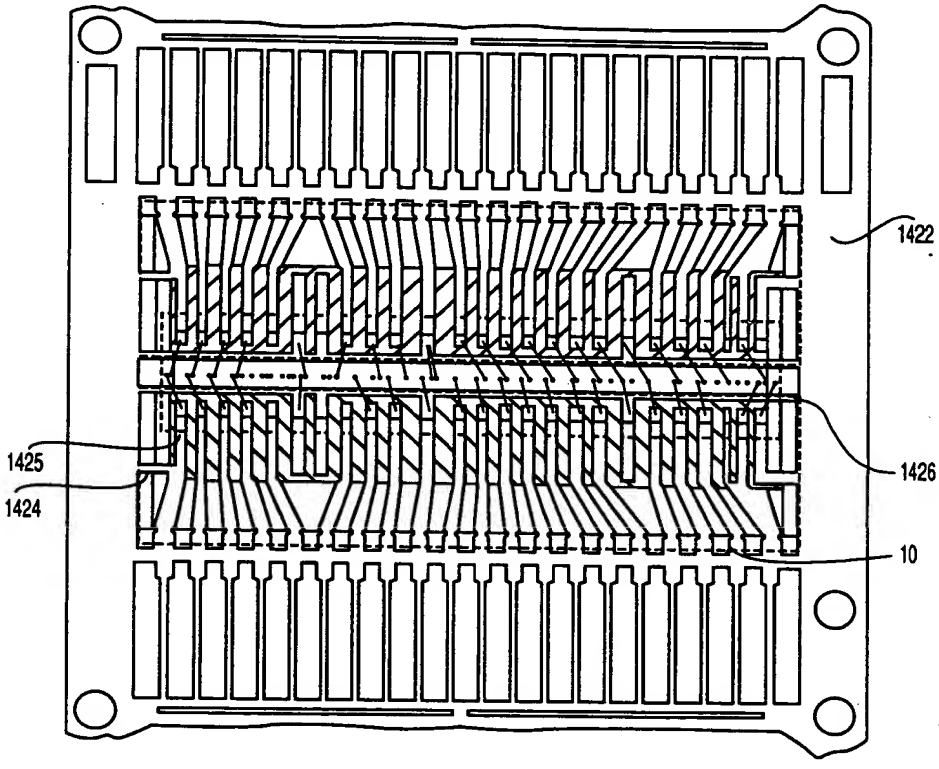


FIG. 111

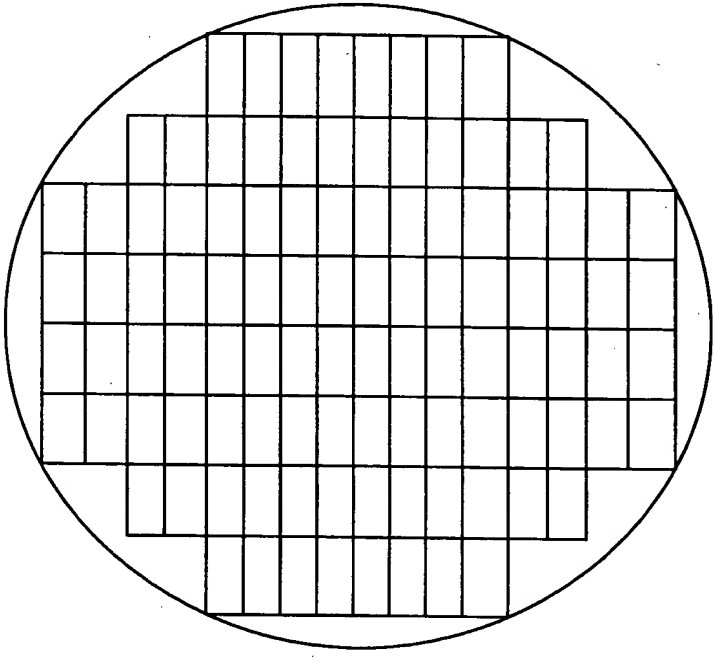


FIG. 112

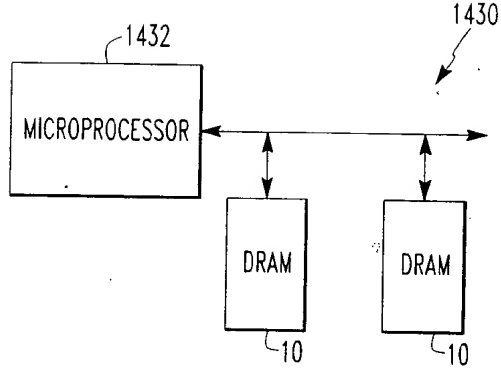


FIG. 113